HDL Simulation using Questa Intel FPGA Edition

Installation Instructions

Simulator Options and Licensing

Quartus Prime and Questa Intel FPGA Edition Version Support

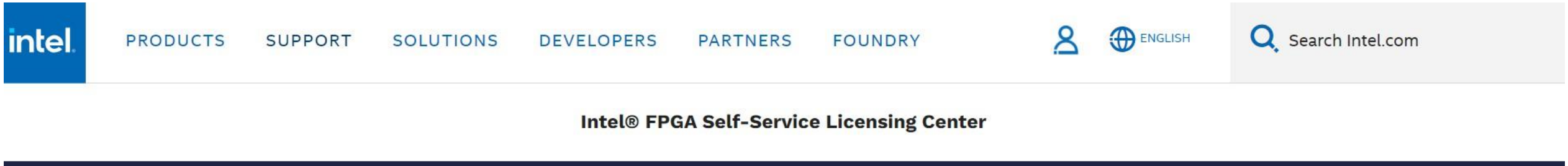
Questa Intel FPGA Edition Version	Licensing	Supported Quartus Prime Version	Performance Difference
Questa Intel FPGA Edition version 2023.3	Licenses are required and must be purchased. Each edition supports the same user interface commands, GUI options, and behavior as the Siemens EDA Questa* Core simulator.	Quartus Prime Pro Edition version 23.4 (Windows, Linux)	Reduced speed and instance count(1) capacity limits in comparison with Siemens EDA Questa* Core.
Questa Intel FPGA Starter Edition 2023.3	Licenses are required but are free. Each edition supports the same user interface commands, GUI options, behavior, and number of module instances as the Siemens EDA Questa* Core simulator.	Quartus Prime Pro Edition version 23.4 (Windows, Linux)	Reduced speed and instance count capacity limits in comparison with Siemens EDA Questa* Core. The Starter Edition has further reduced performance levels.
Questa Intel FPGA Edition version 2023.3	Licenses are required and must be purchased. Each edition supports the same user interface commands, GUI options, and behavior as the Siemens EDA Questa* Core simulator.	Quartus Prime Standard Edition version 23.1 (Windows, Linux)	Reduced speed and instance count capacity limits in comparison with Siemens EDA Questa* Core.
Questa Intel FPGA Starter Edition 2023.3	Licenses are required but are free. Each edition supports the same user interface commands, GUI options, behavior, and number of module instances as the Siemens EDA Questa* Core simulator	Quartus Prime Standard Edition version 23.1 (Windows, Linux)	Reduced speed and instance count capacity limits in comparison with Siemens EDA Questa* Core. The Starter Edition has further reduced performance levels.

Simulator Options and Licensing

Quartus Prime Pro Edition Supported Simulators

Vendor	Simulator	Version	Platform	Supports Siemens EDA Verification IP
Aldec	Active-HDL*	13.0	Windows* 64-bit	No
Aldec	Riviera-PRO*	2023.04	Windows, Linux, 64-bit	No
Cadence	Xcelium* Parallel Simulator	22.09.001	Linux 64-bit	Yes
Siemens EDA	QuestaSim* Simulator(2)	2022.4	Windows, Linux, 64-bit	Yes
Synopsys*	VCS*, VCS MX	T-2022.06-SP2-3	Linux 64-bit	Yes

Obtaining Questa Intel License



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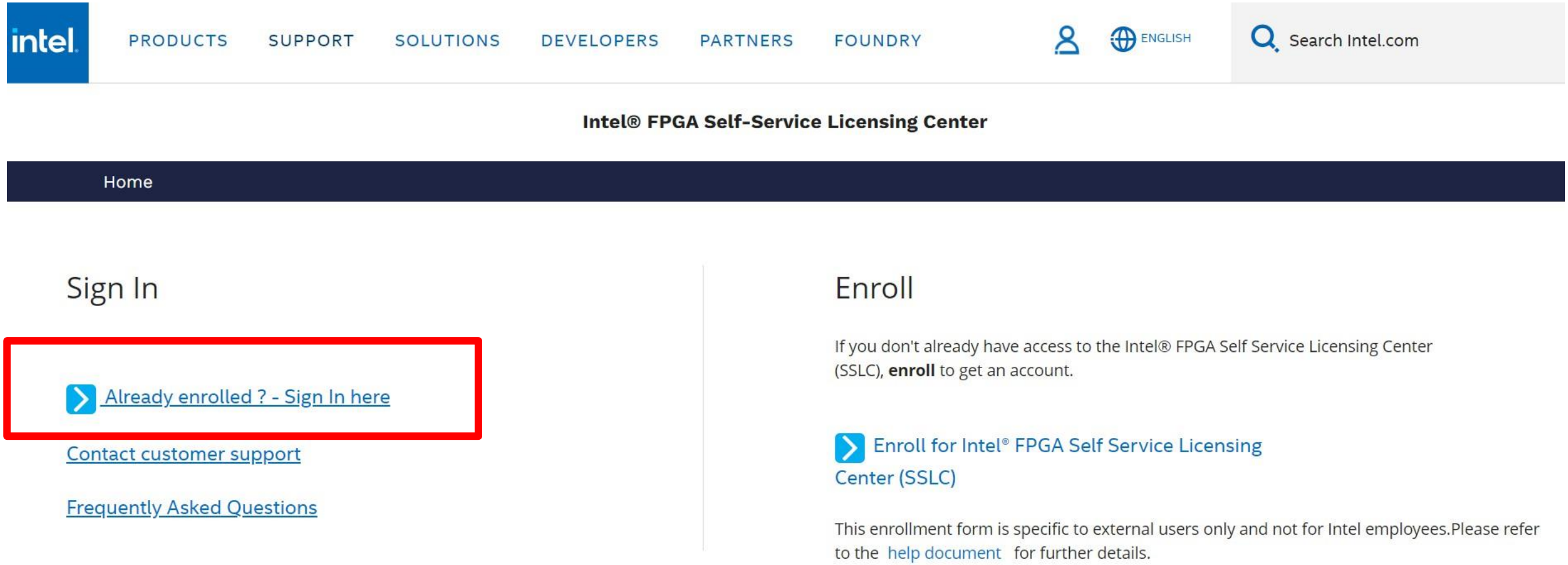
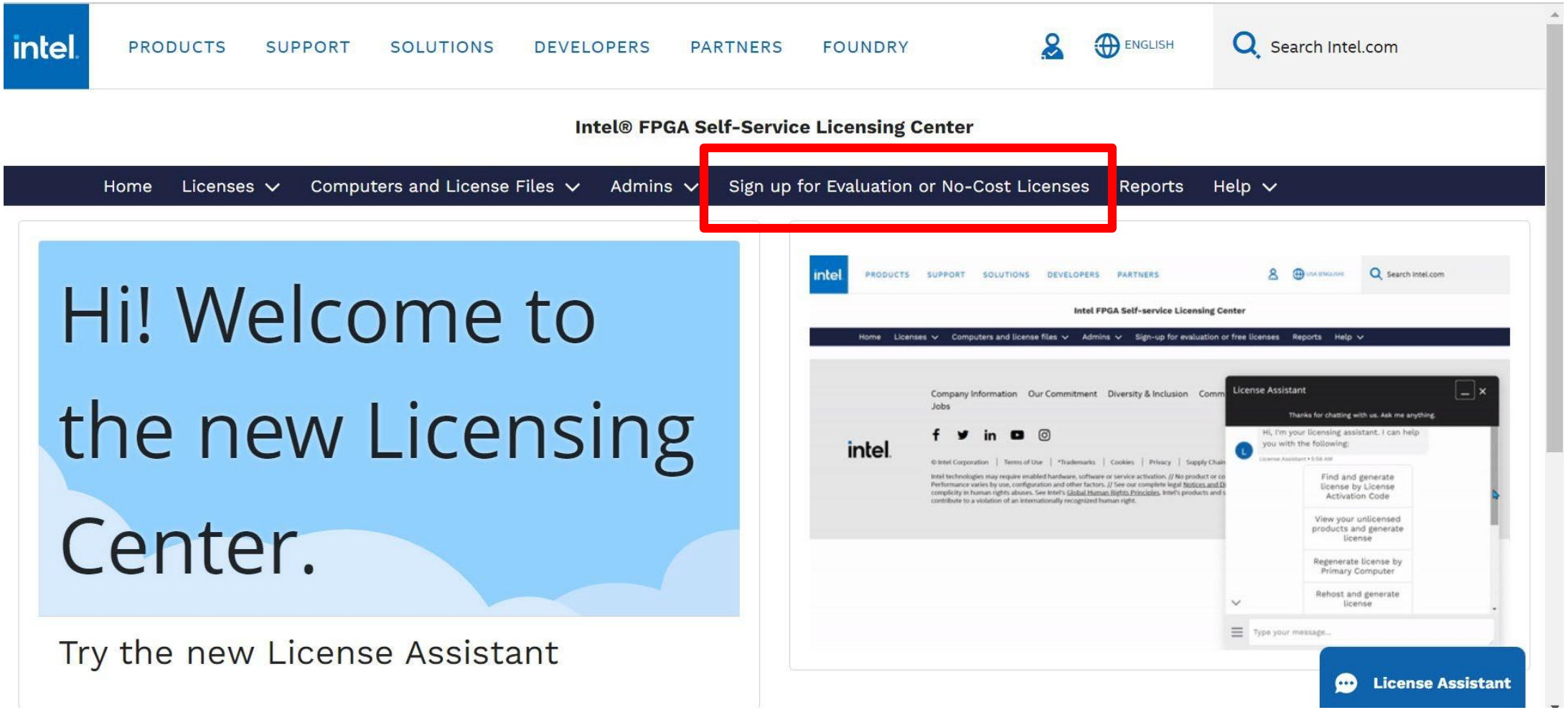


Obtaining Questa Intel



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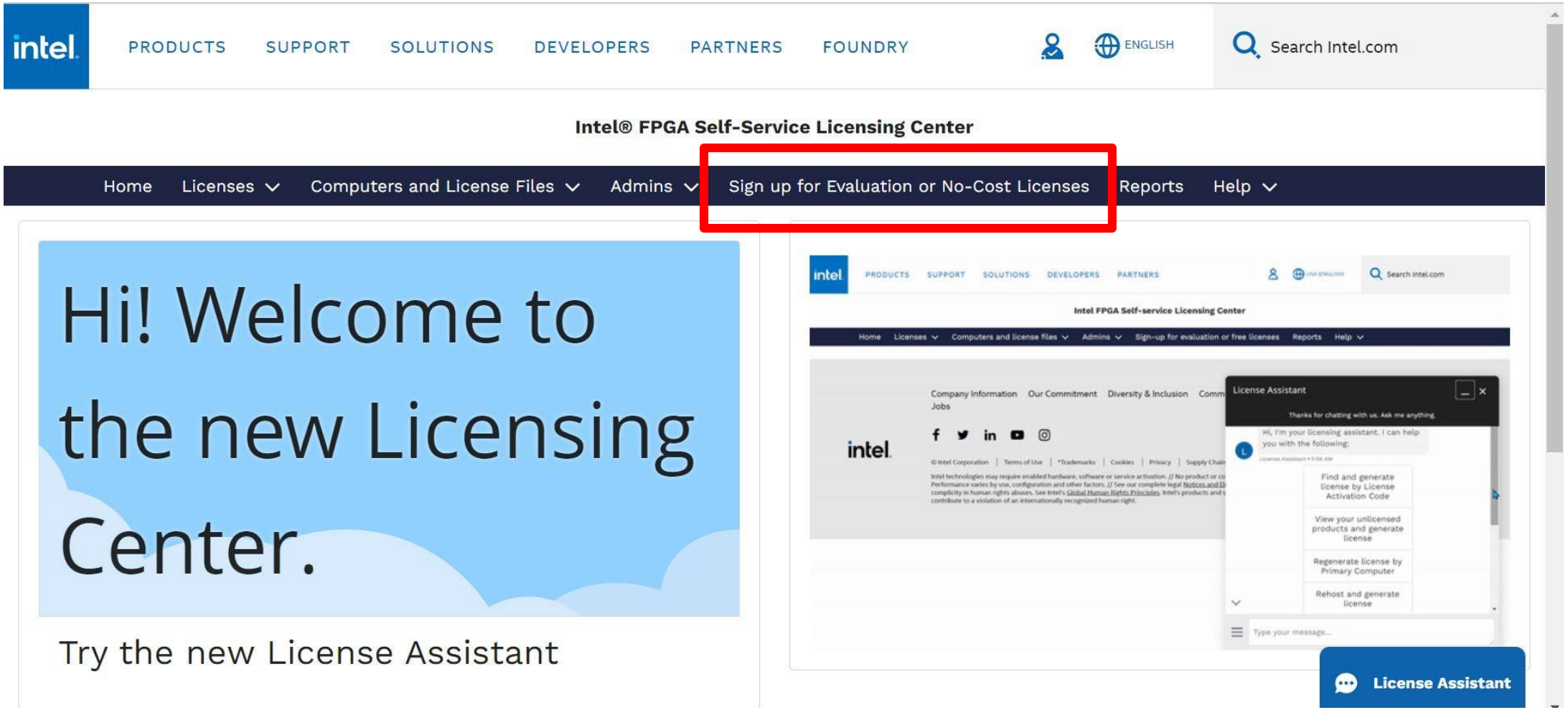
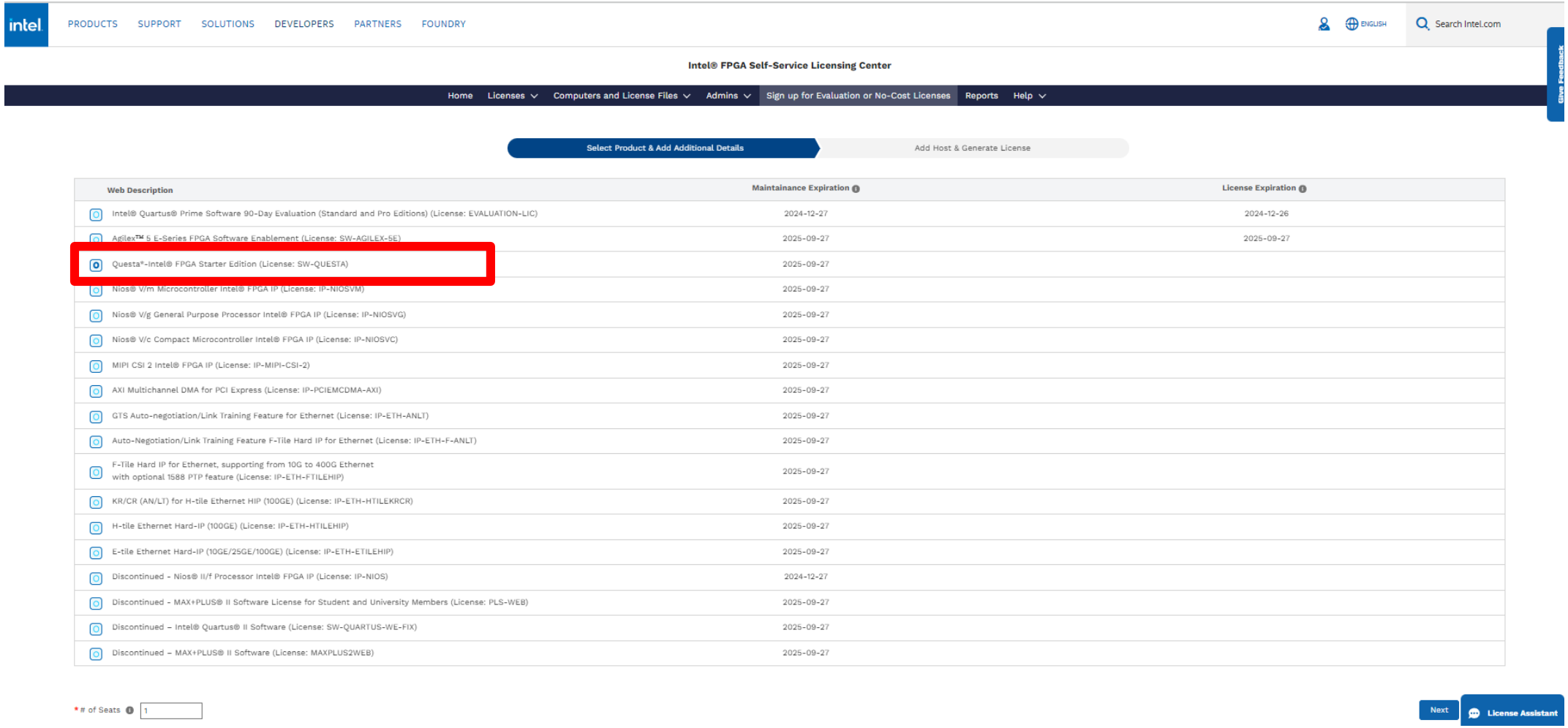


Obtaining Questa Intel License



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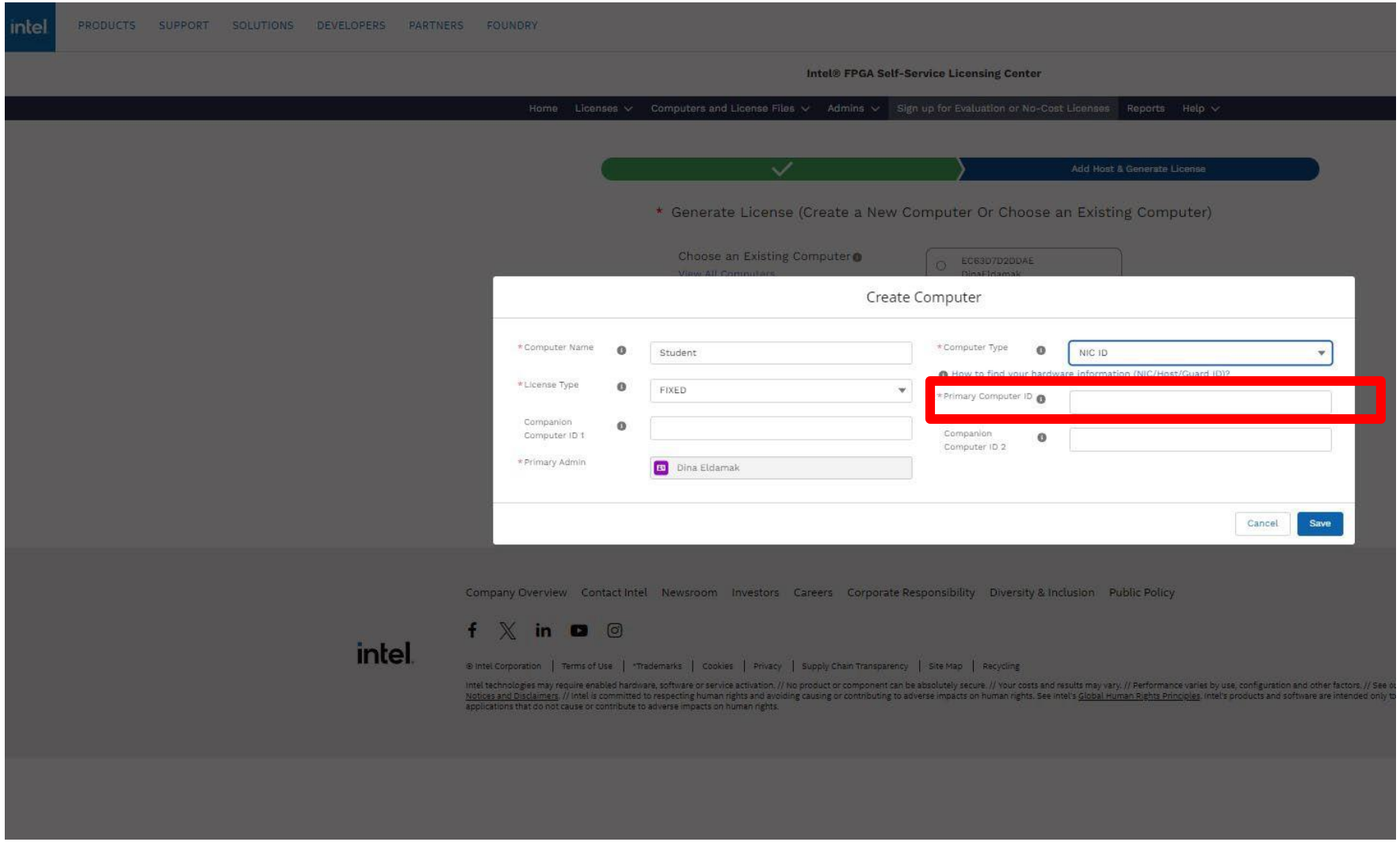
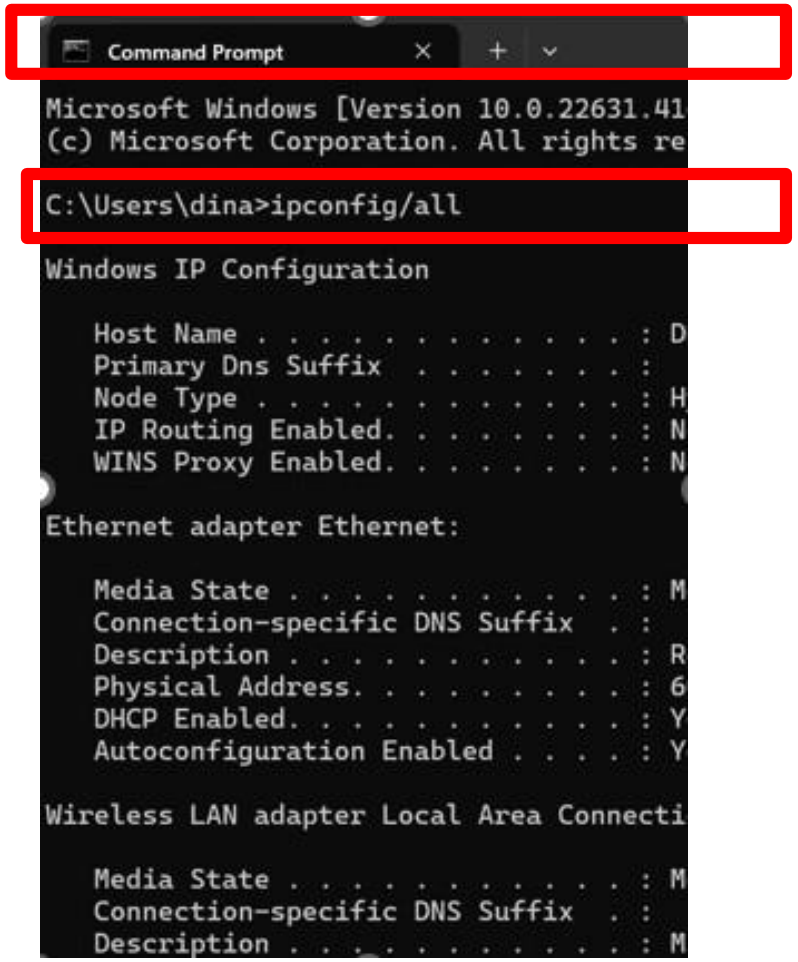
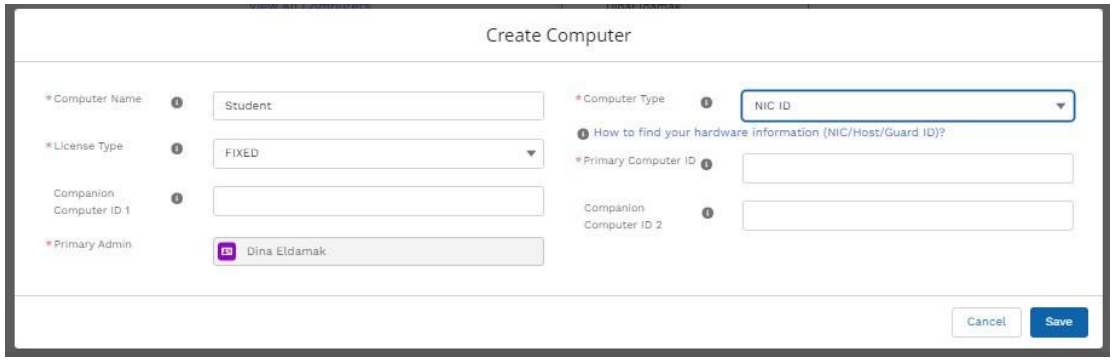
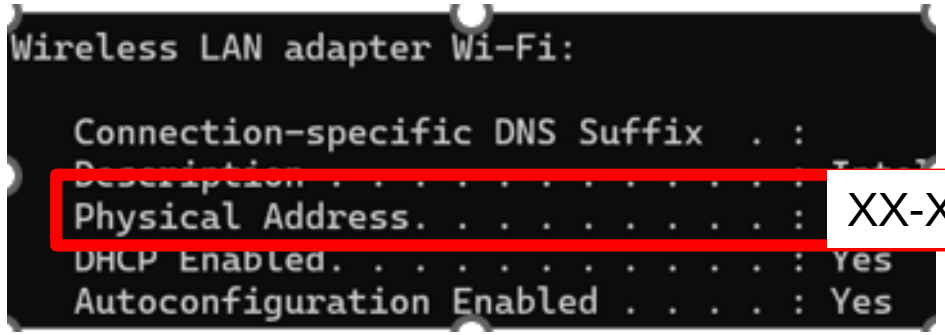


Finding Computer ID







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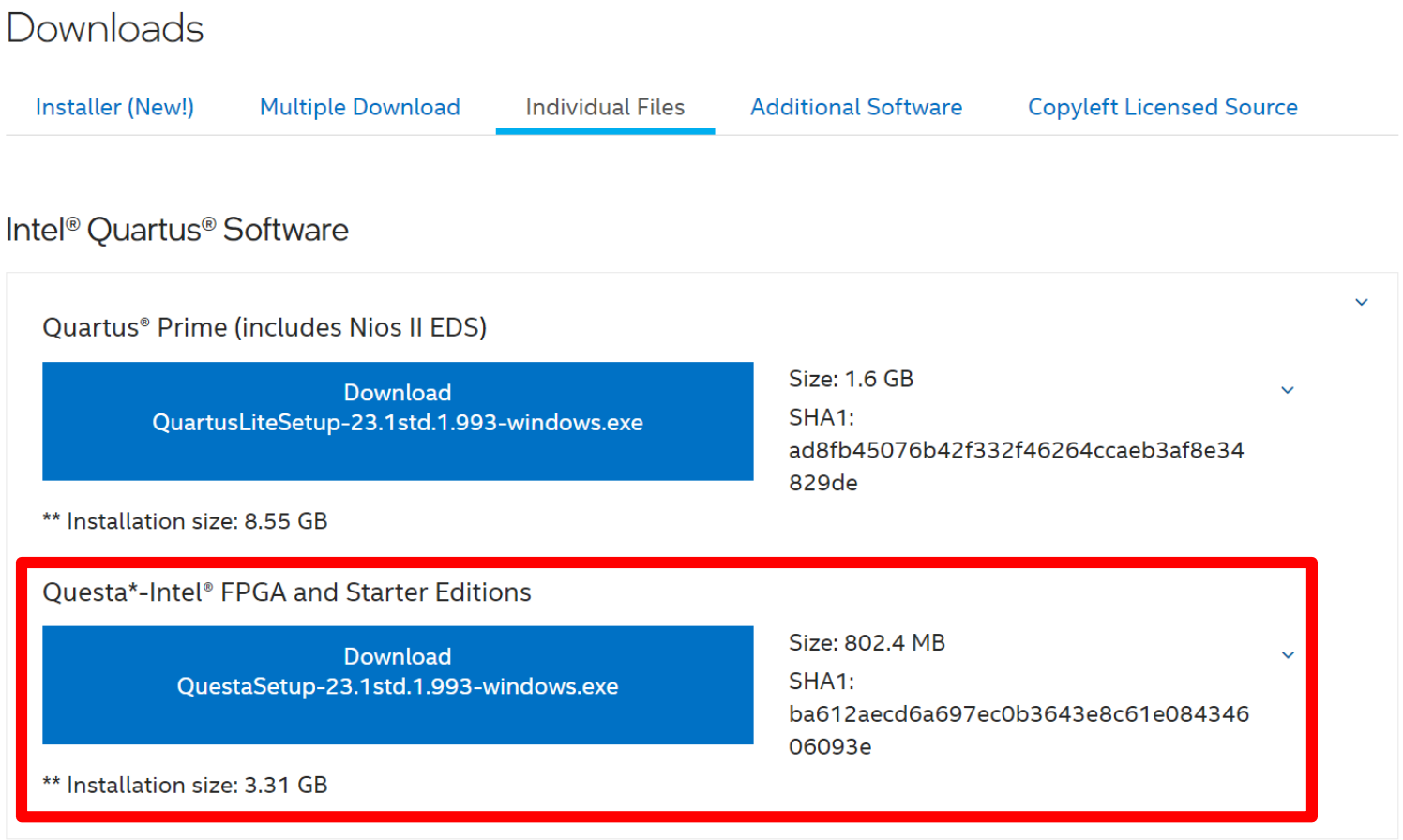
Remove the dashes before you enter the physical address in create computer

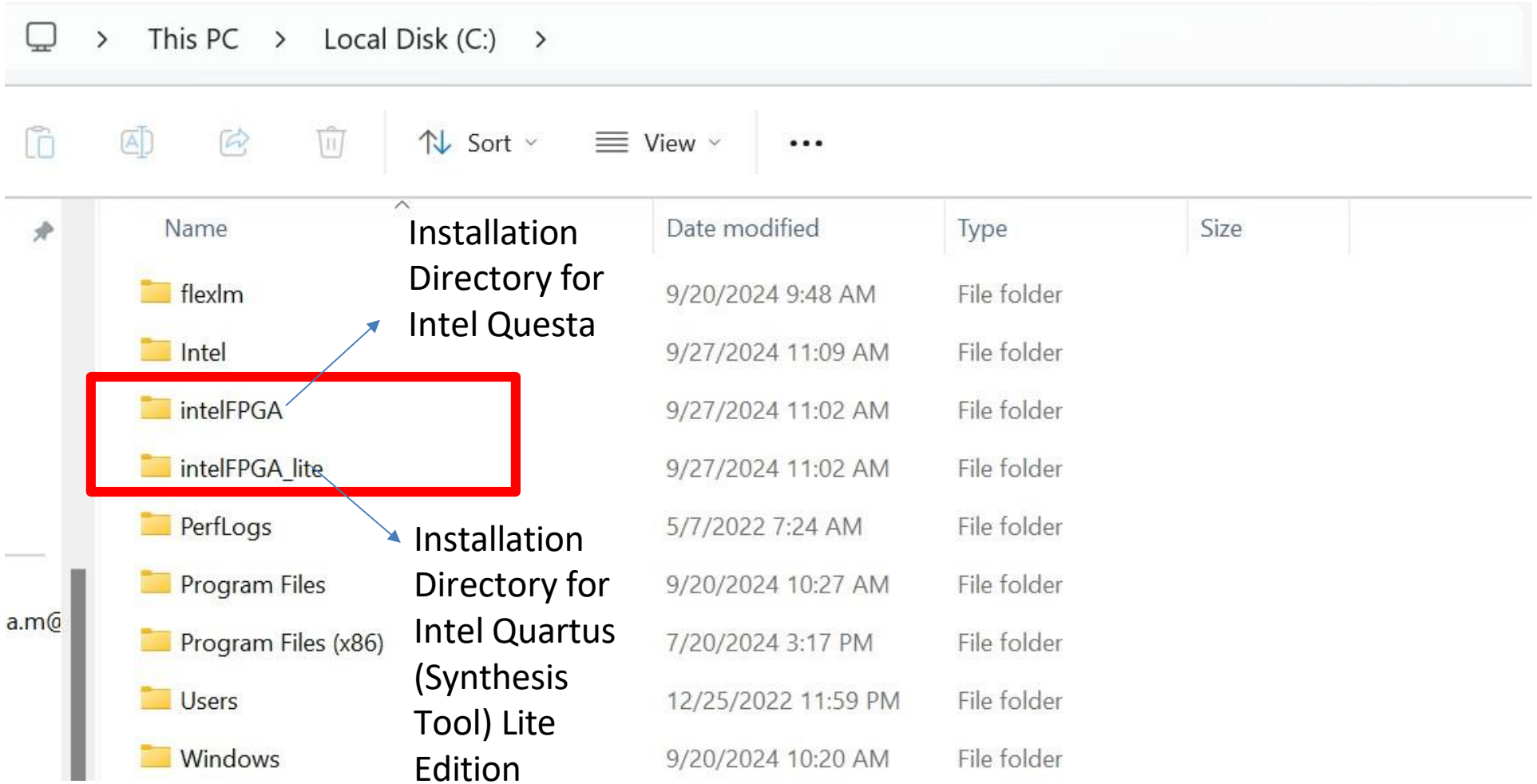
Generate License and obtain it by email

Download Intel Questa Software



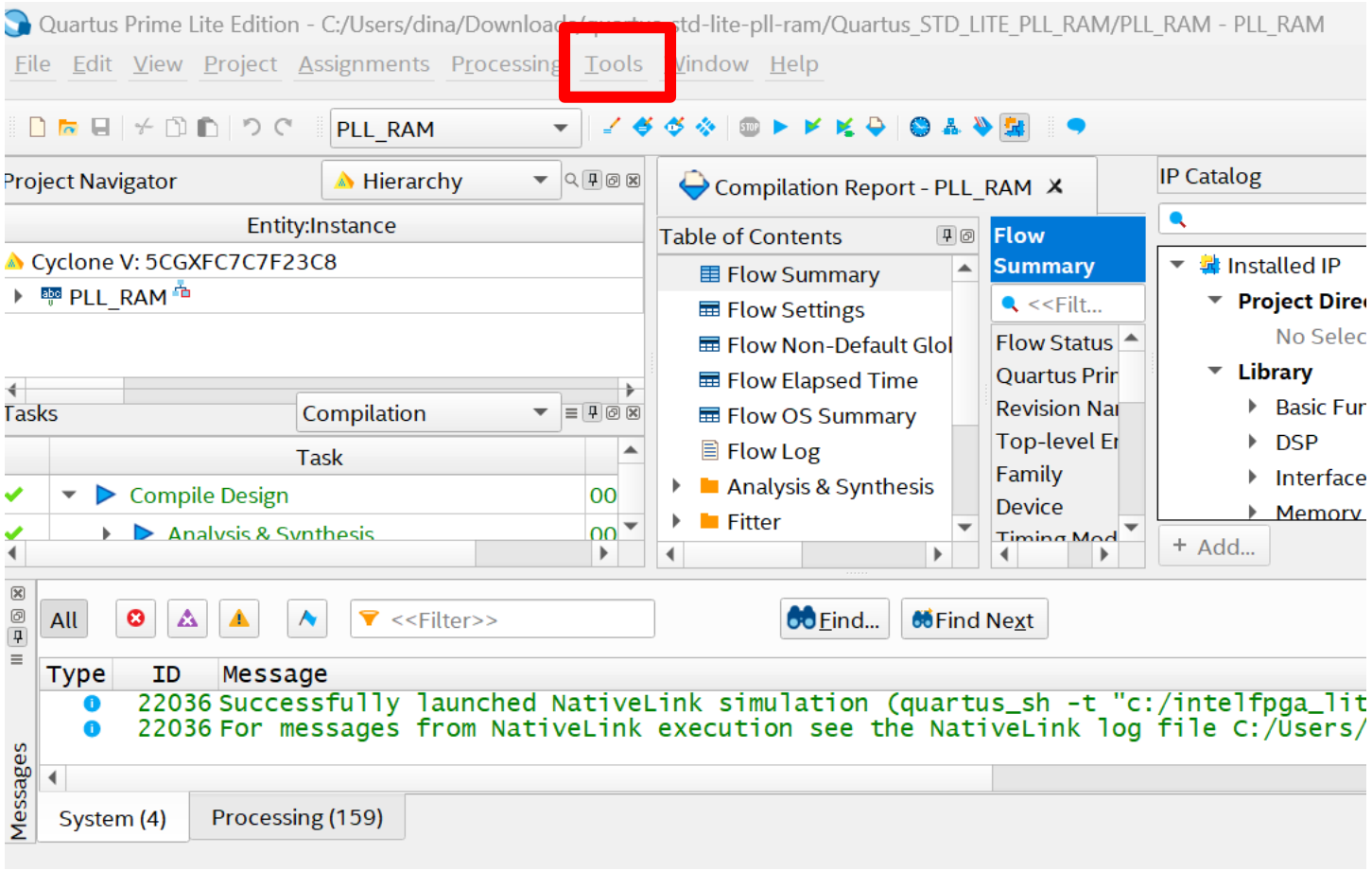
https://www.intel.com/content/www/us/en/software-kit/825278/intel-quartus-prime-lite-edition-design-software-version-23-1-1-for-windows.html

Check your C: Folder

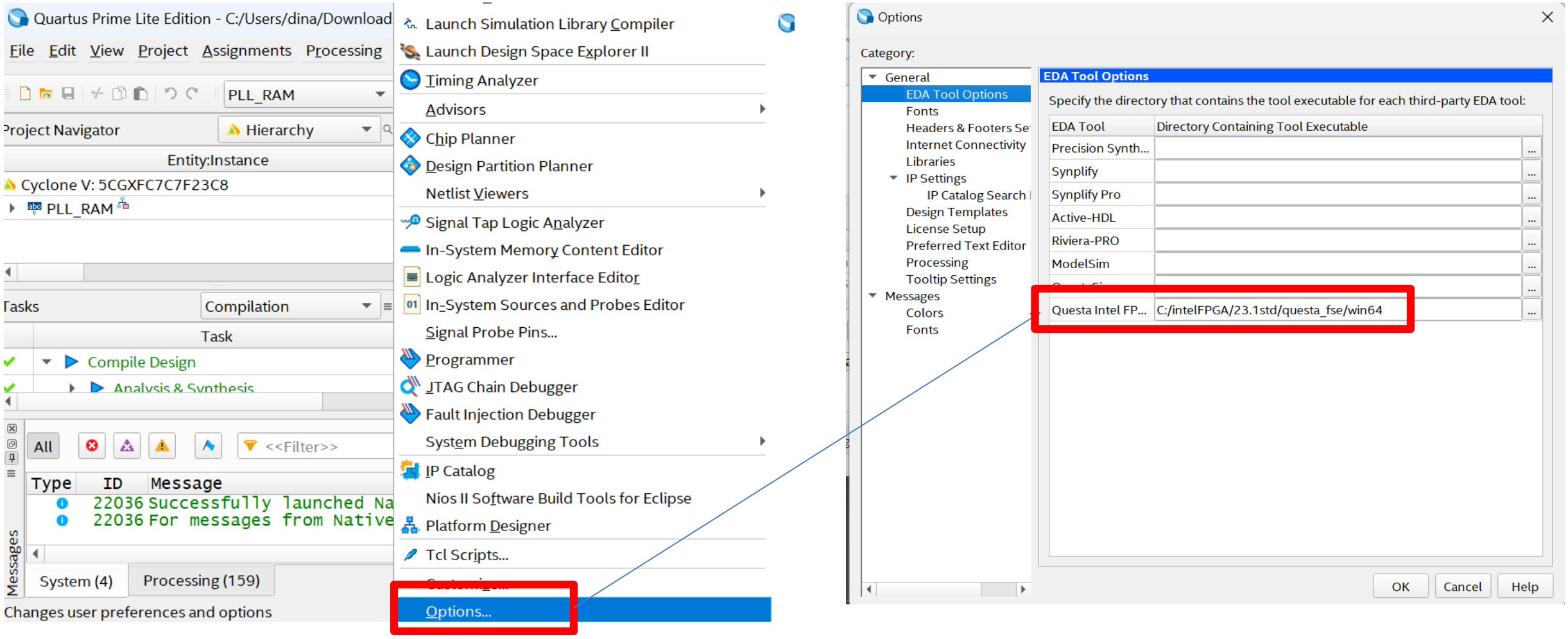


Setup Intel Questa

Open Intel Quartus

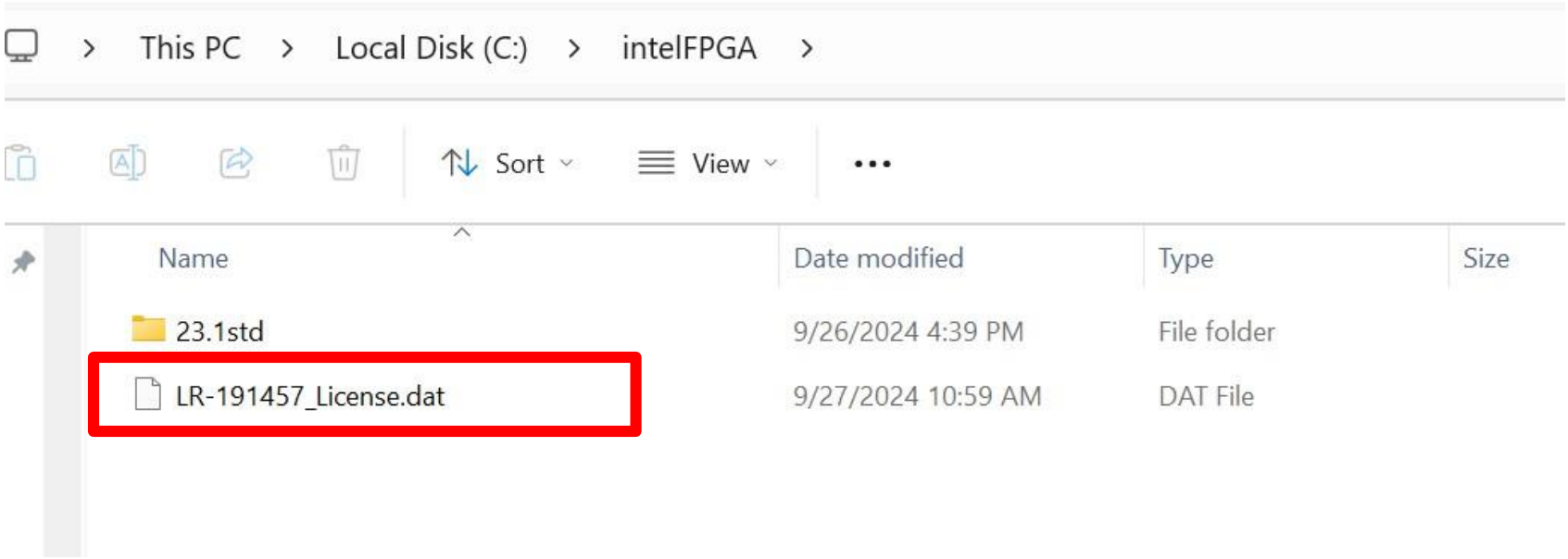


Setup Intel Questa

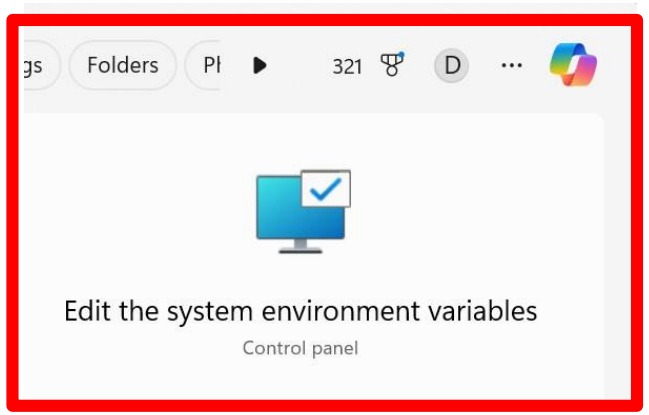


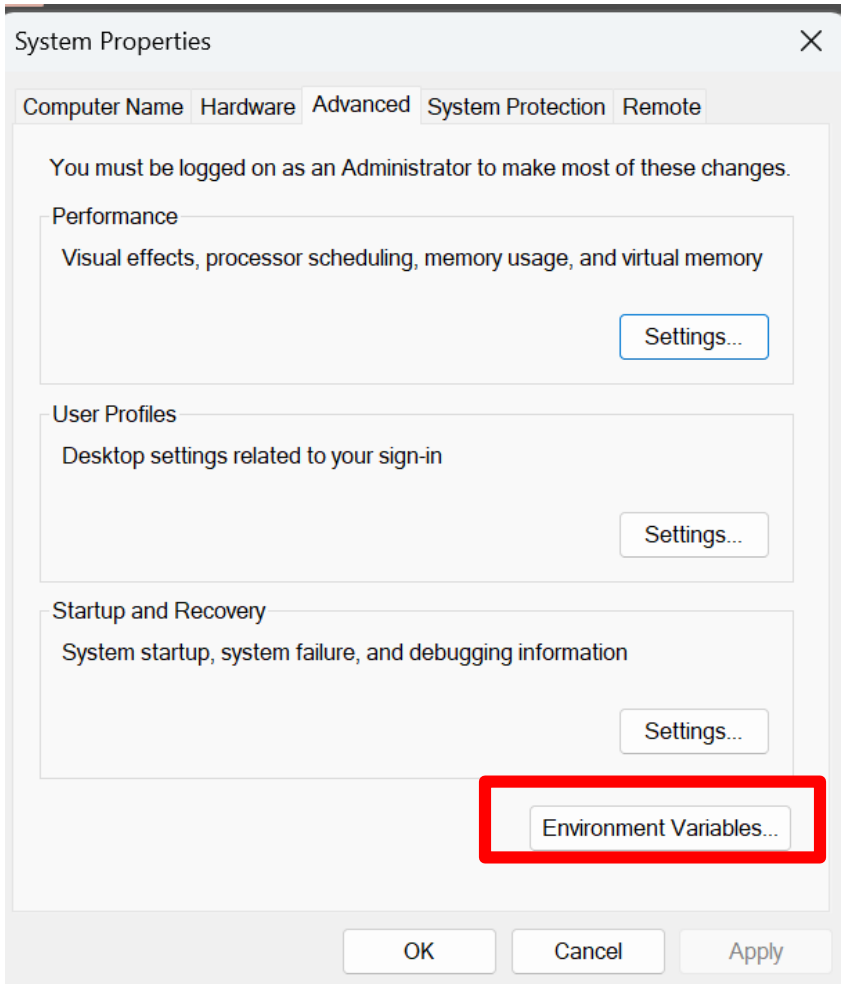
Adding License File

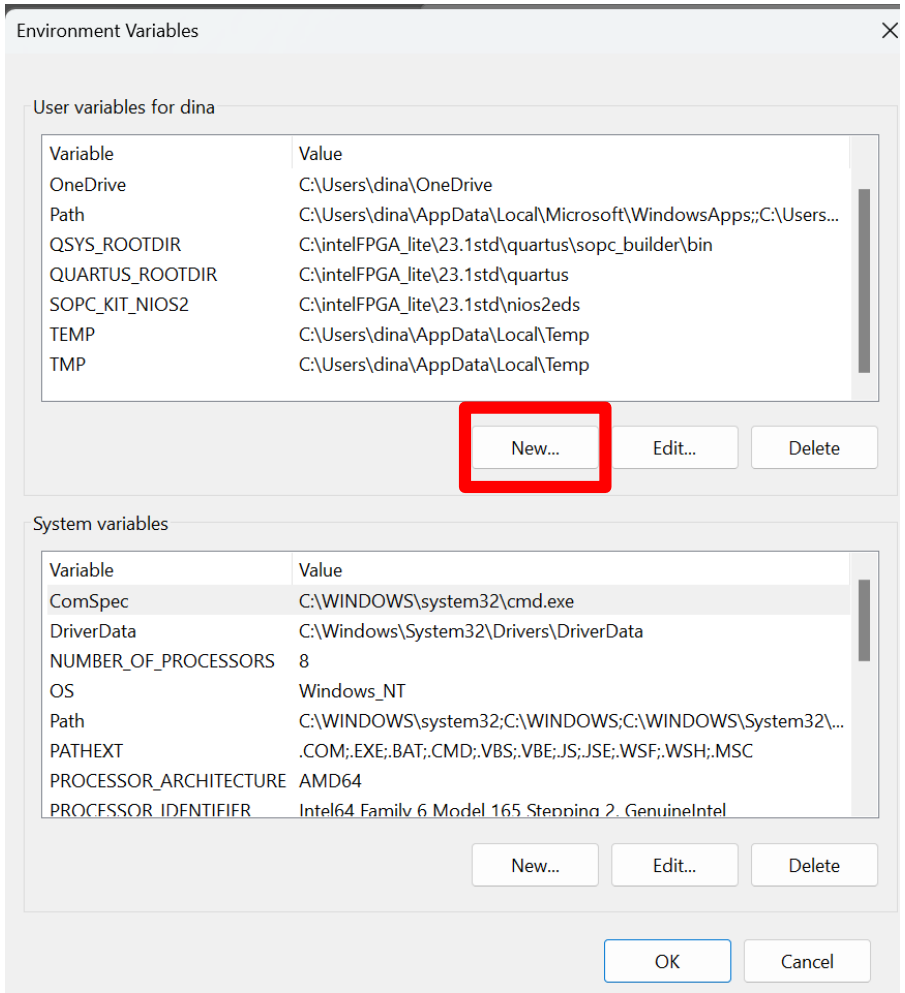
Copy license file to intelFPGA folder



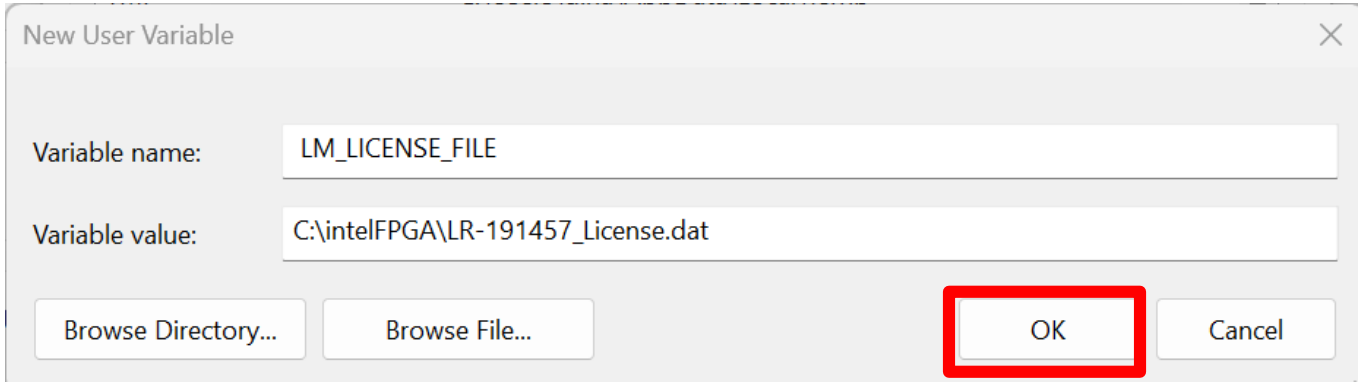
Adding License File

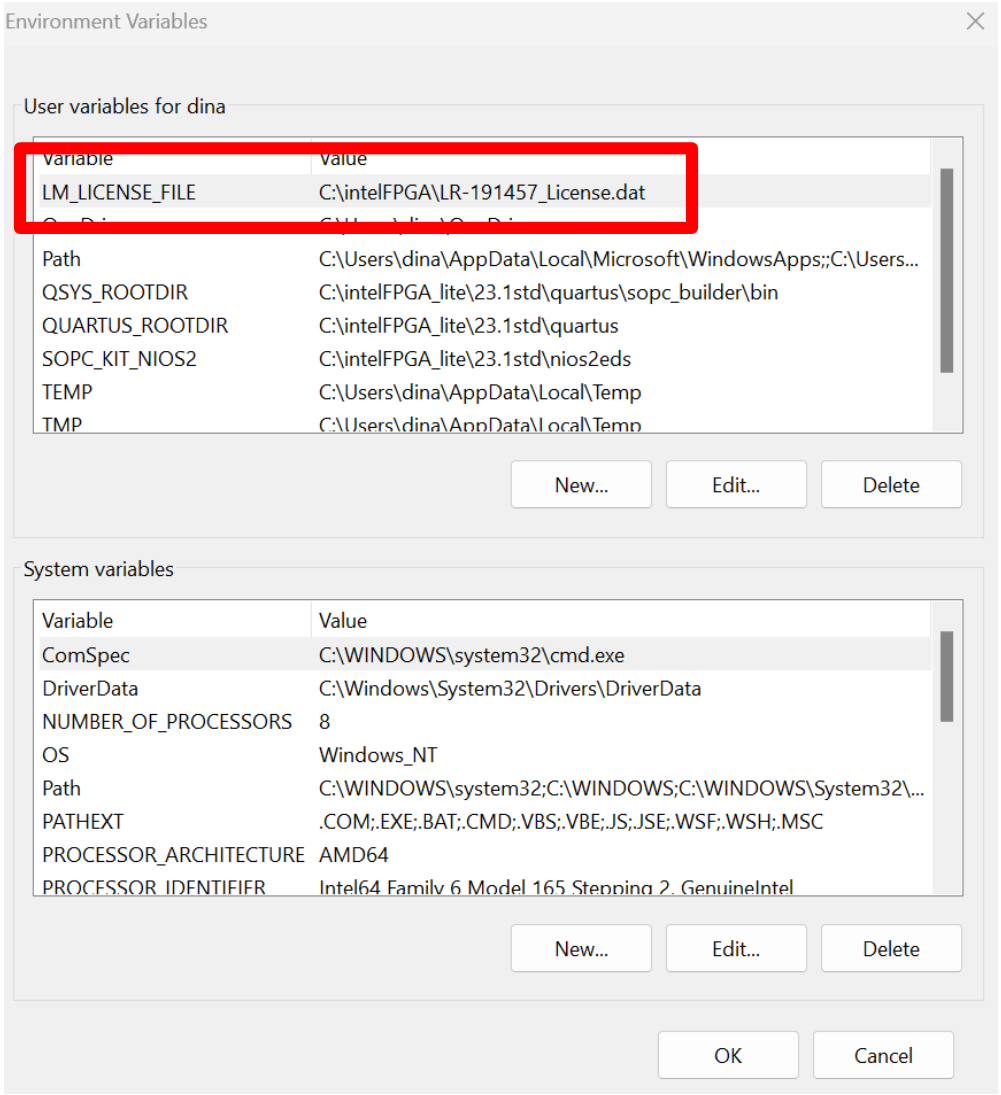






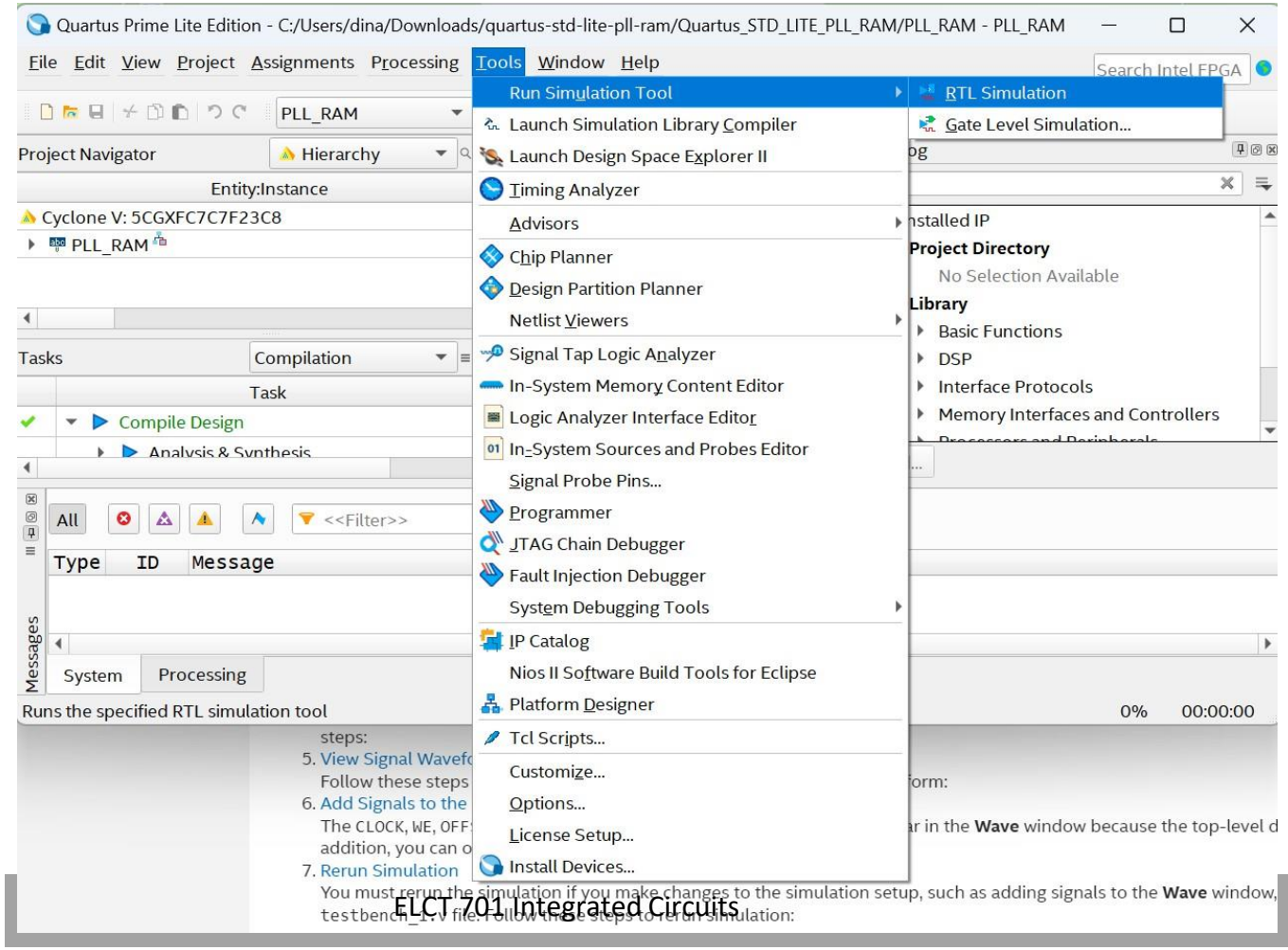
Adding License File



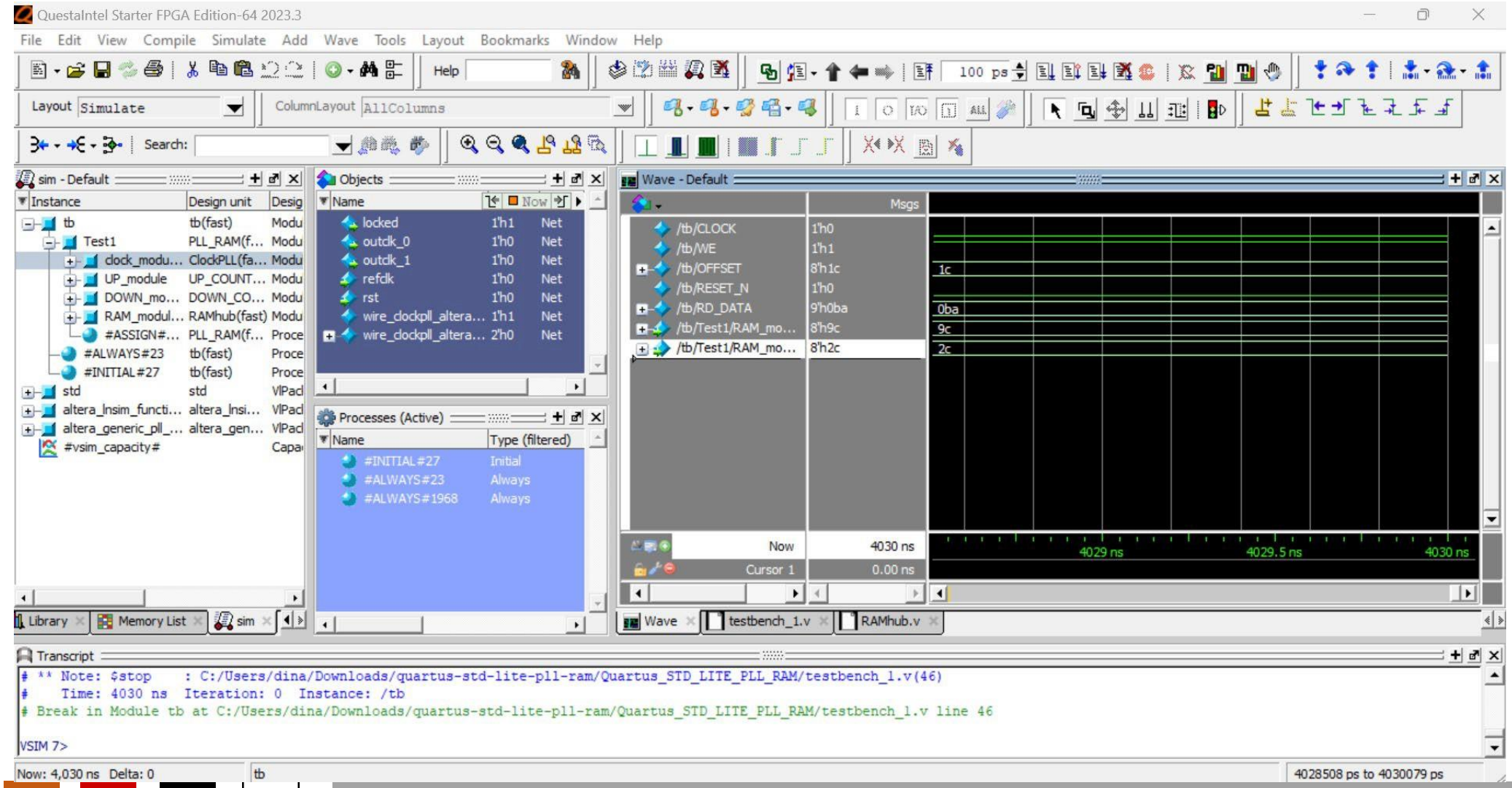


Launch Intel Questa

Restart windows then launch Intel Quartus



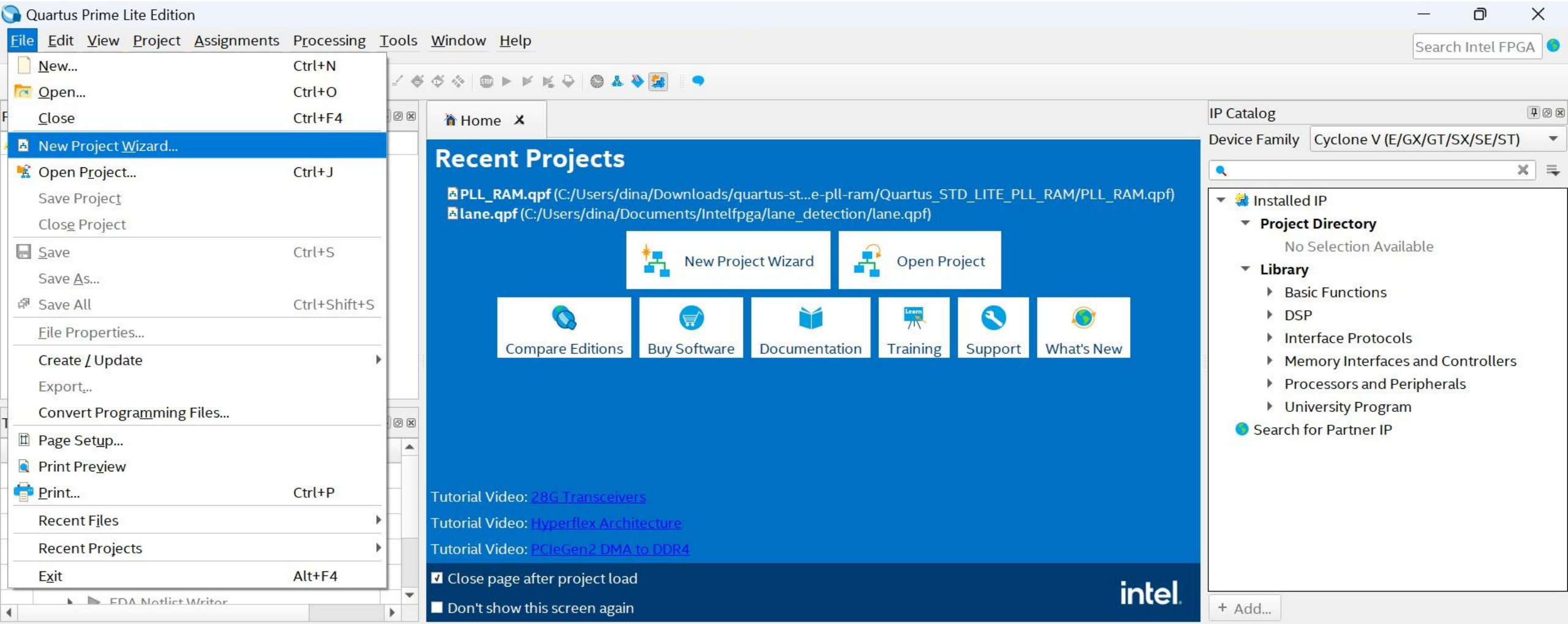
Launch Intel Questa



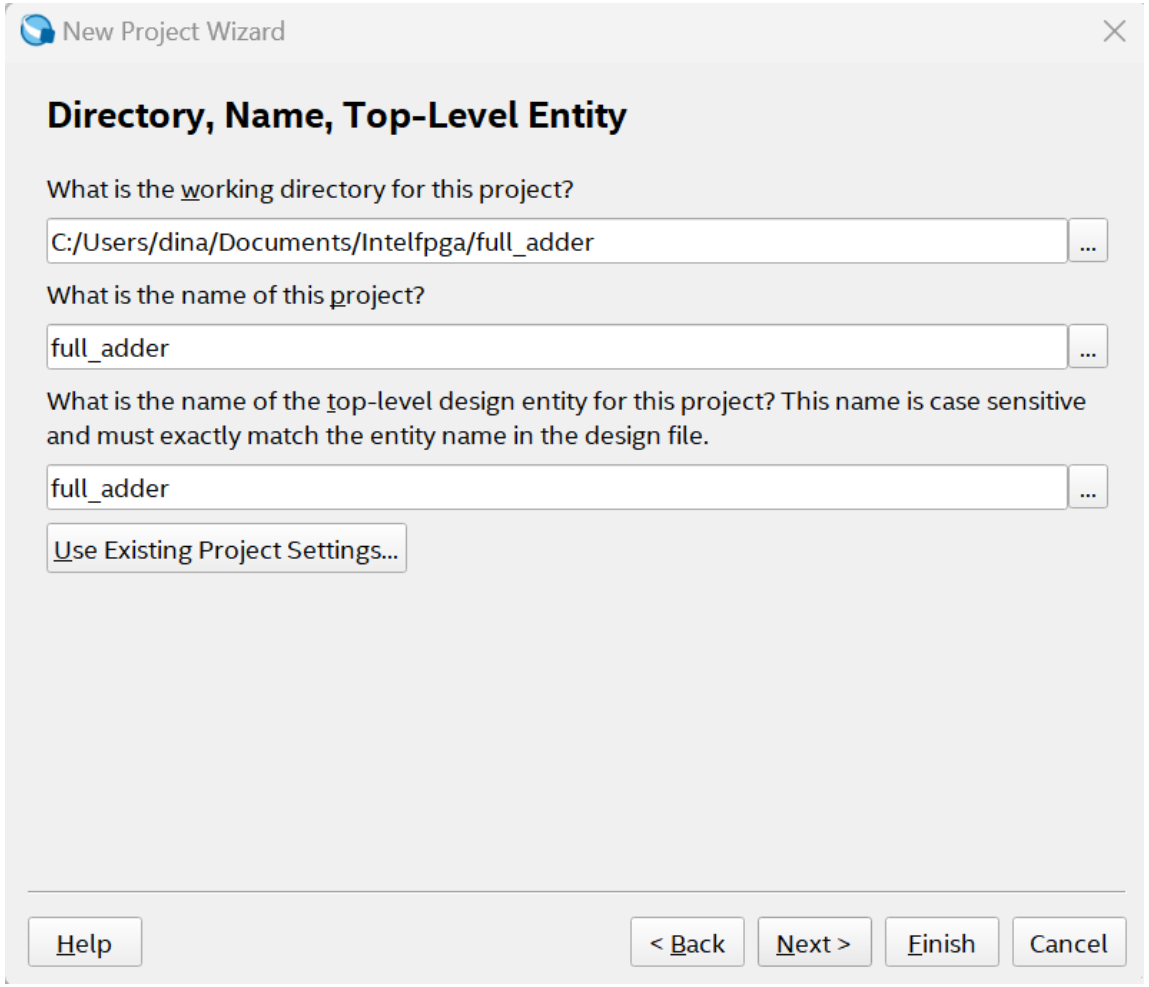
VHDL Simulation using Questa Intel FPGA Edition

Tutorial

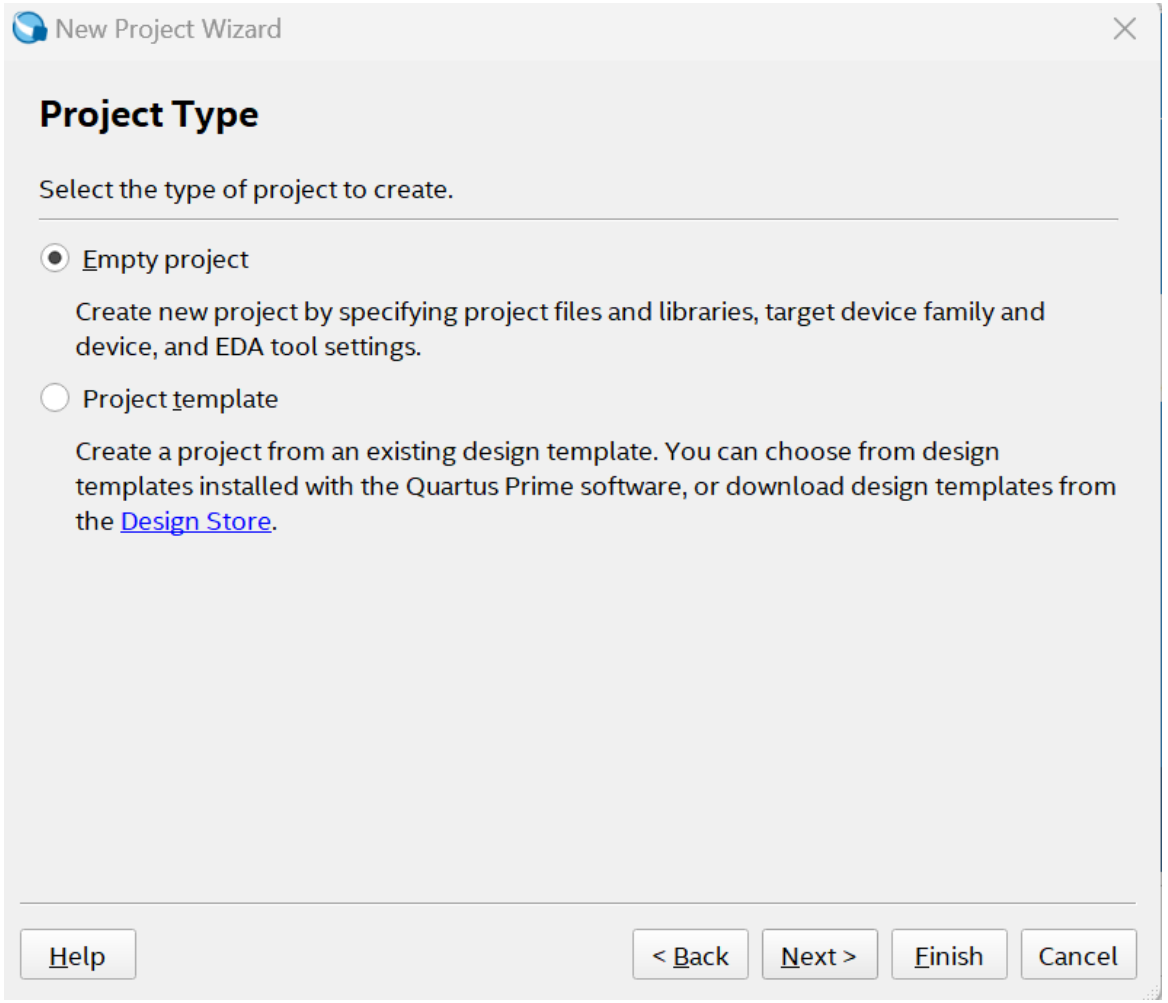
Create New Project



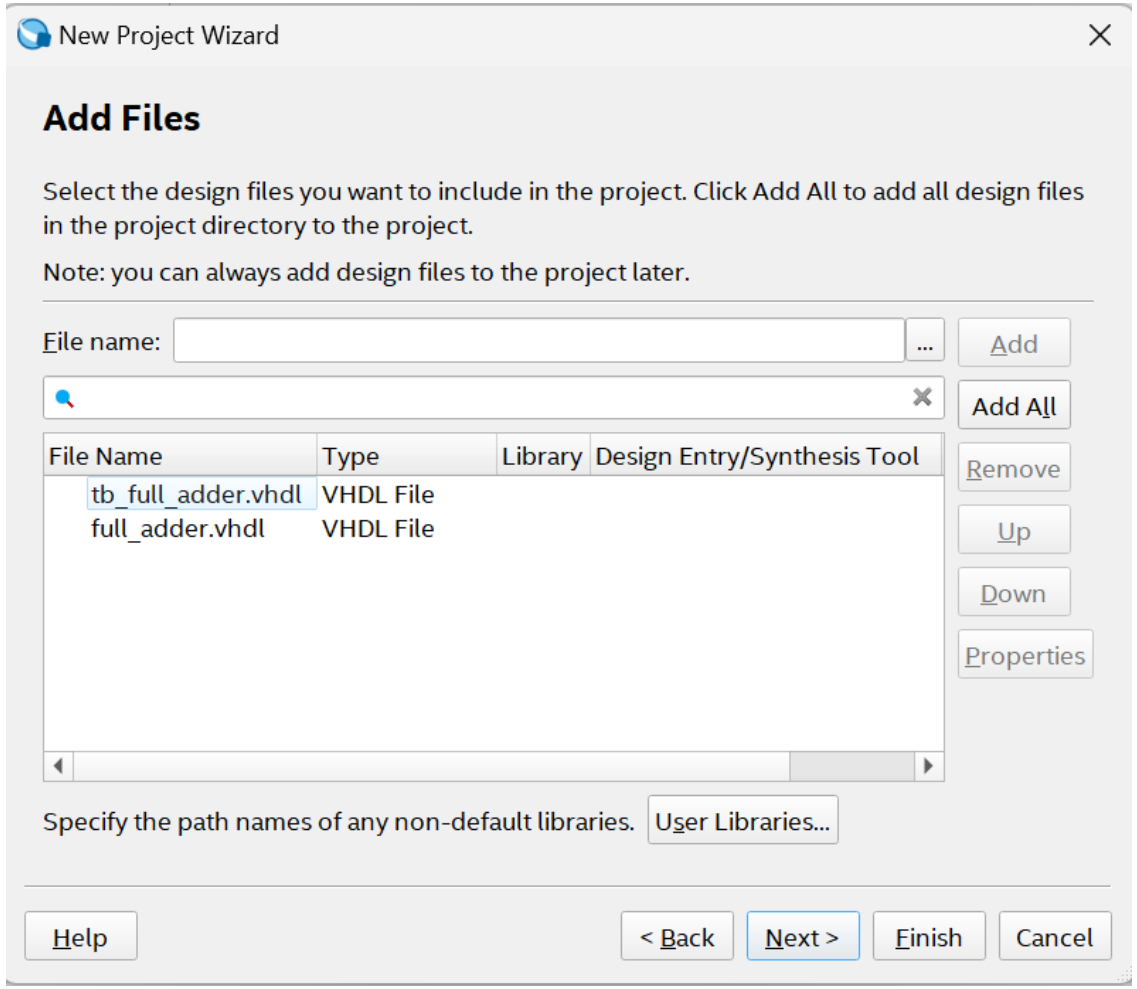
Create New Project



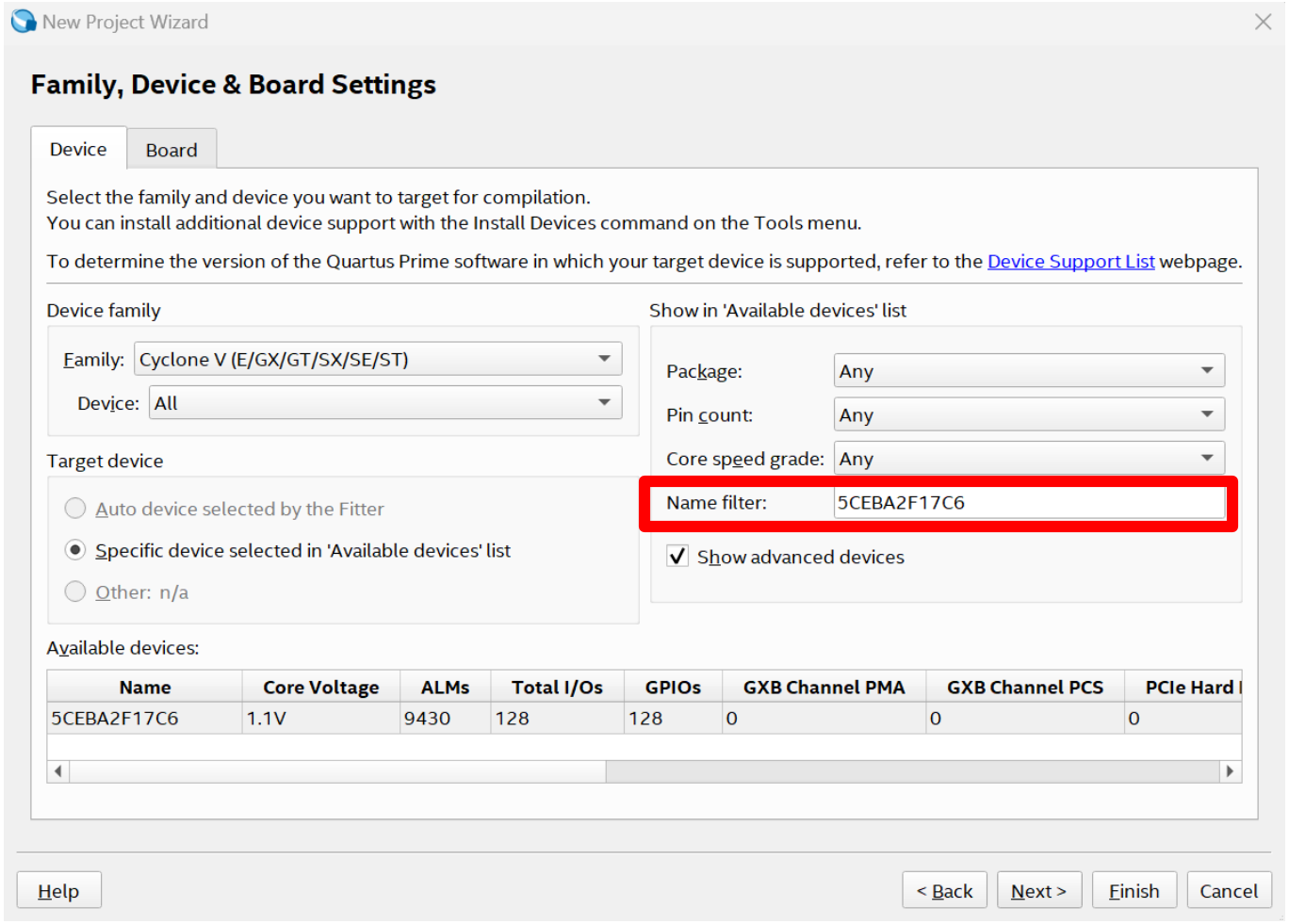
Create New Project



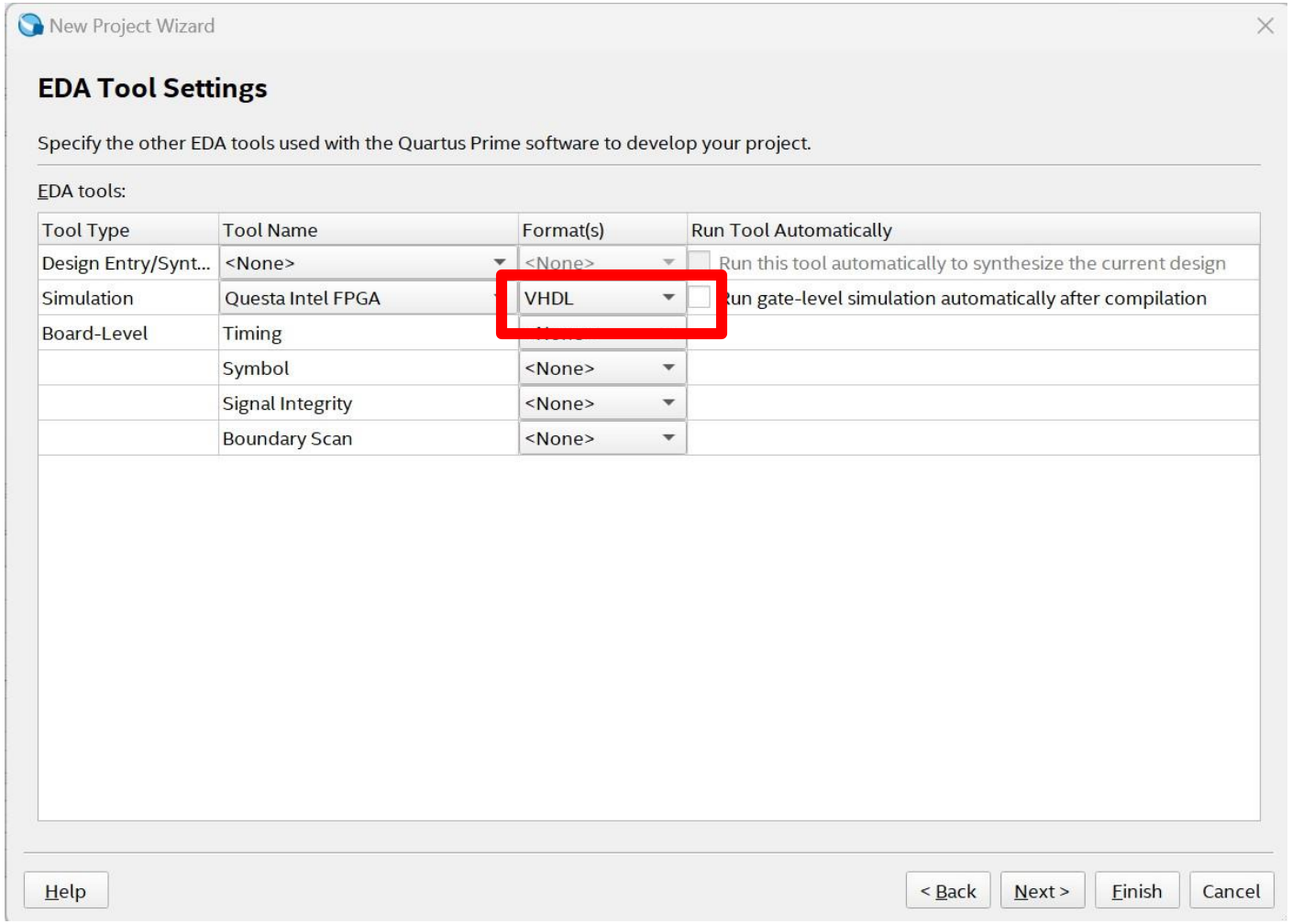
Add VHDL Files



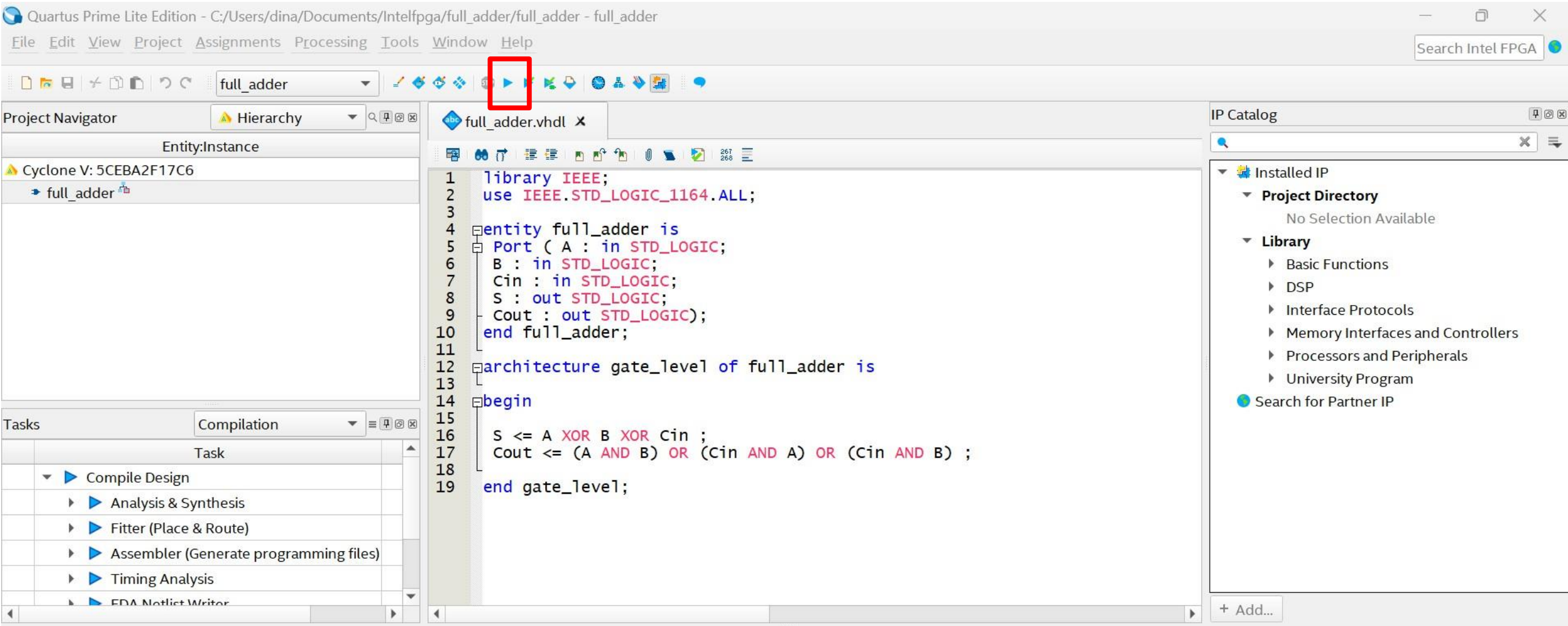
Select FPGA


New Project Wizard
Family, Device & Board Settings
Device
Board
Select the family and device you want to target for compilation.
You can install additional device support with the Install Devices command on the Tools menu.
To determine the version of the Quartus Prime software in which your target device is supported, refer to the Device Support List webpage.
Device family
Family: Cyclone V (E/GX/GT/SX/SE/ST)
Device: All
Target device
Auto device selected by the Fitter
Specific device selected in 'Available devices' list
Other: n/a
Show in 'Available devices' list
Package: Any
Pin count: Any
Core speed grade: Any
Name filter: 5CEBA2F17C6
Show advanced devices
Available devices:
Name | Core Voltage | ALMs | Total I/Os | GPIOs | GXB Channel PMA | GXB Channel PCS | PCIe Hard
5CEBA2F17C6 | 1.1V | 9430 | 128 | 128 | 0 | 0 | 0
Help
< Back
Next >
Finish
Cancel

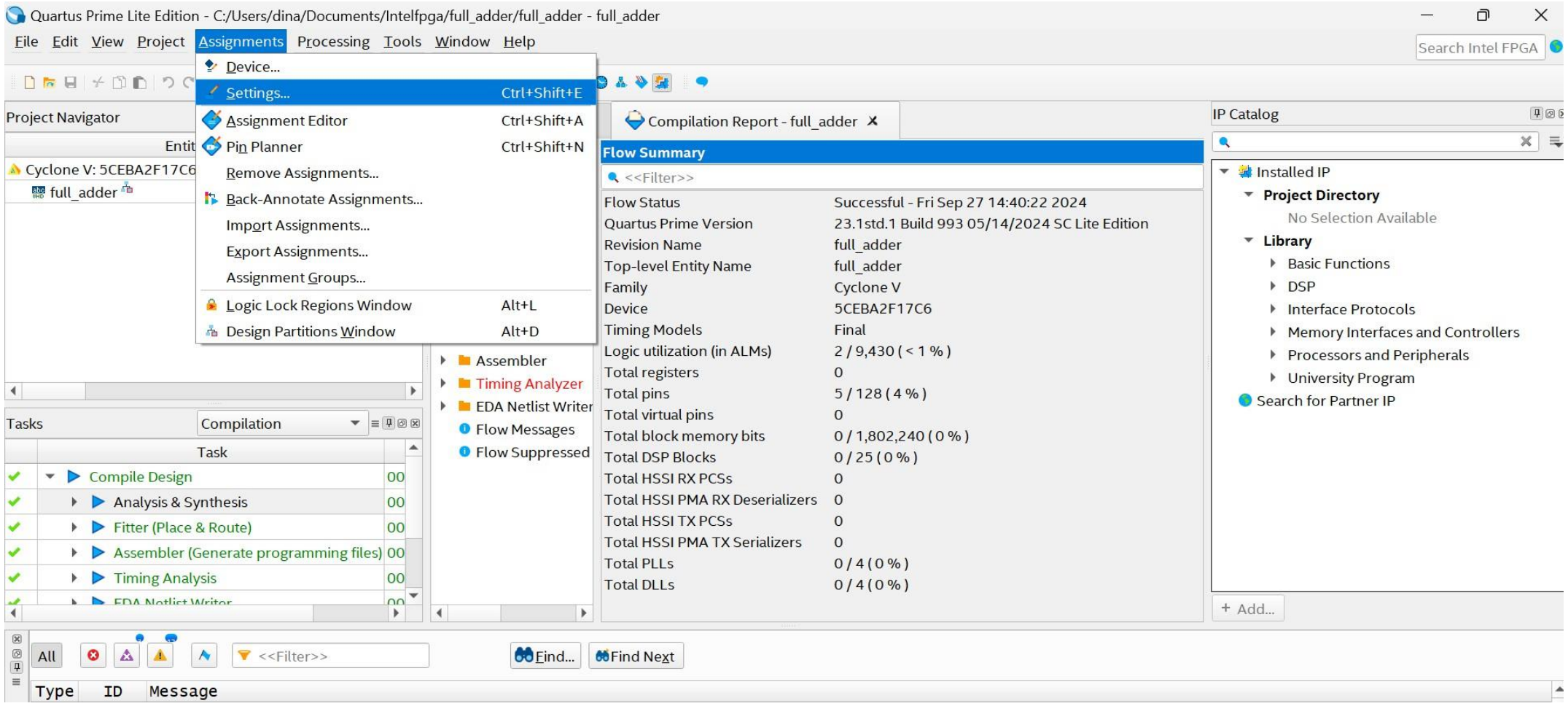
EDA Tools Settings

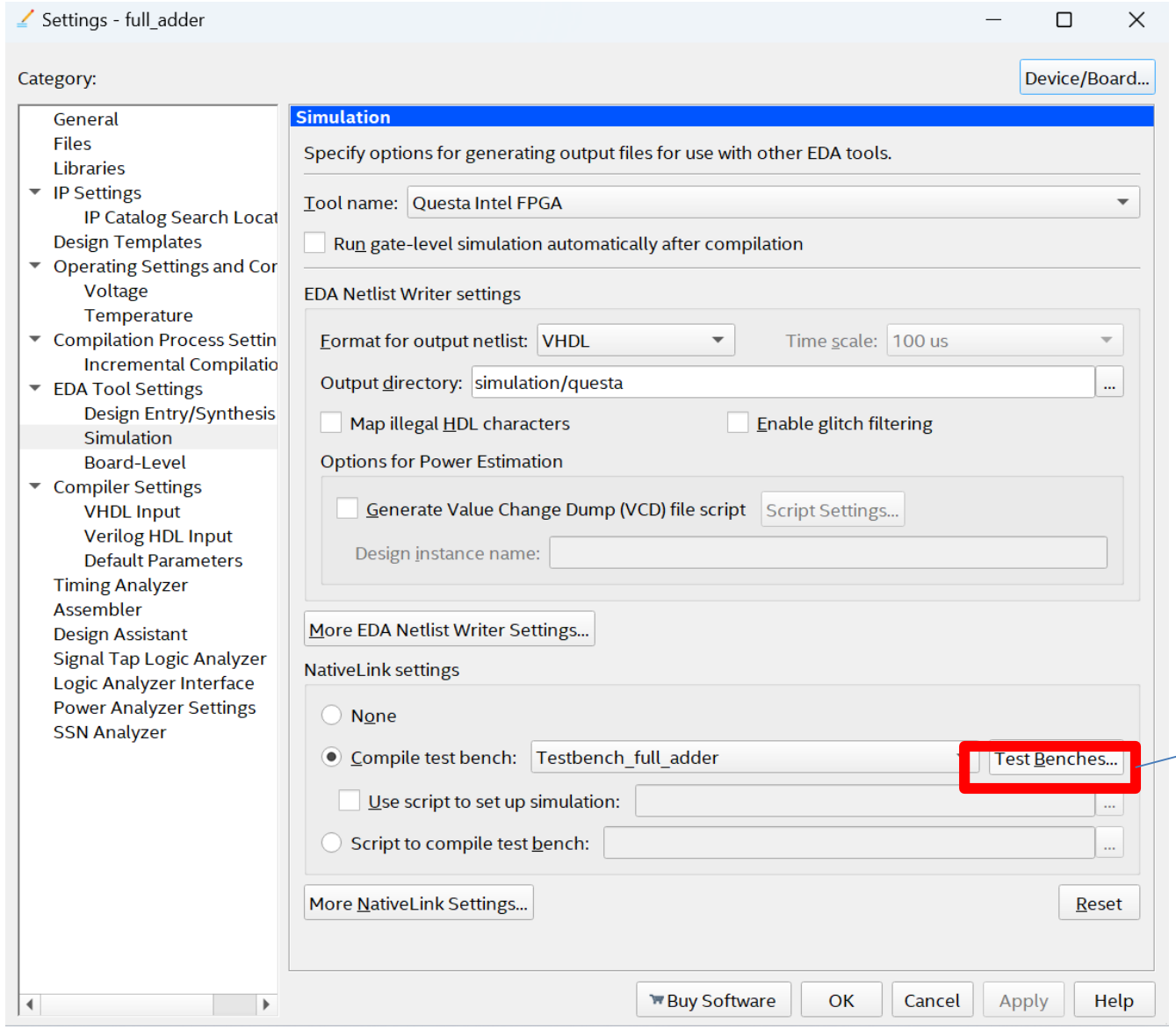


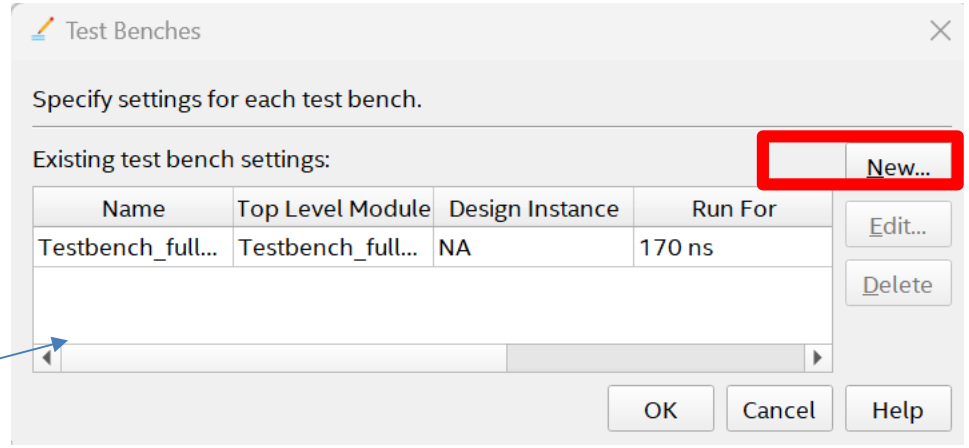
View the VHDL Code and start compilation



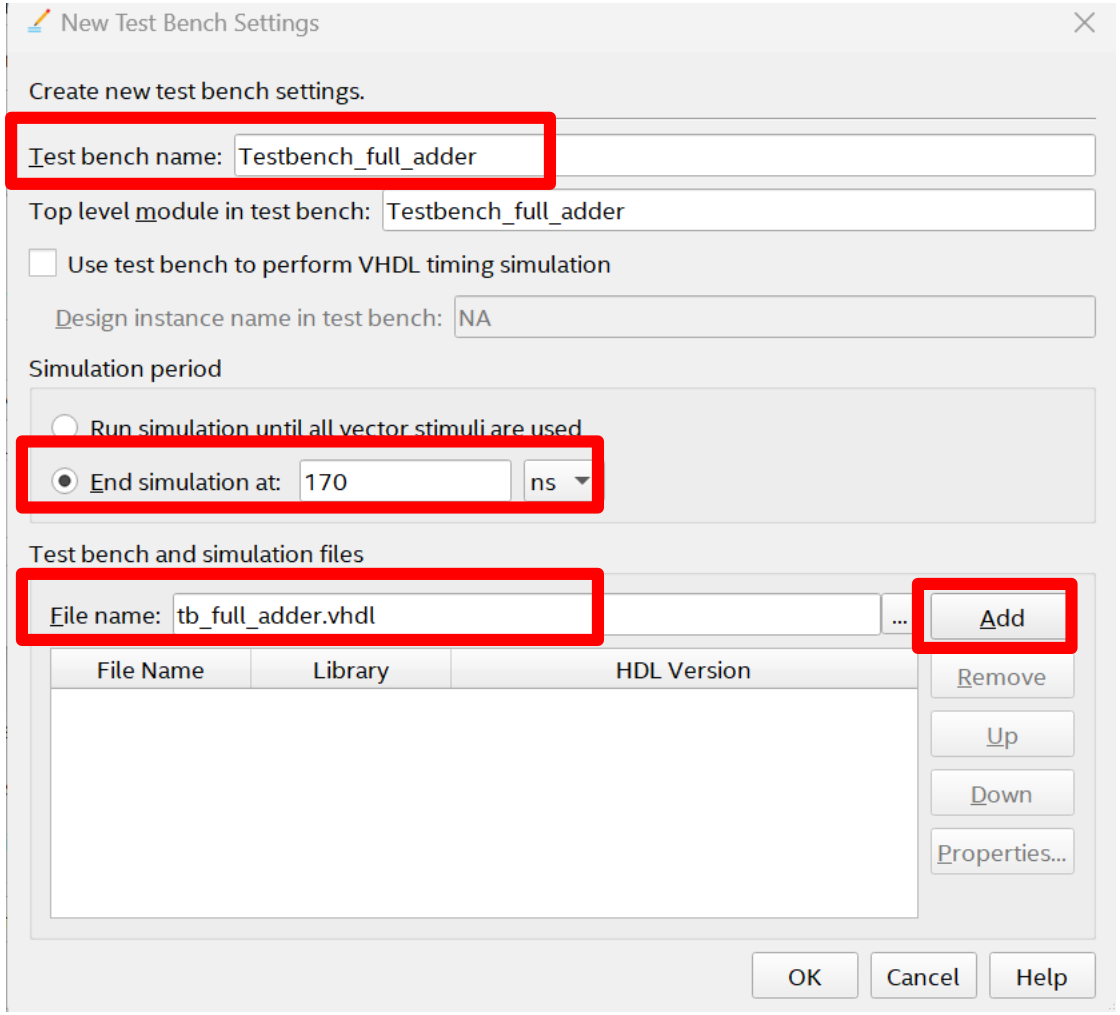
Setup the testbench



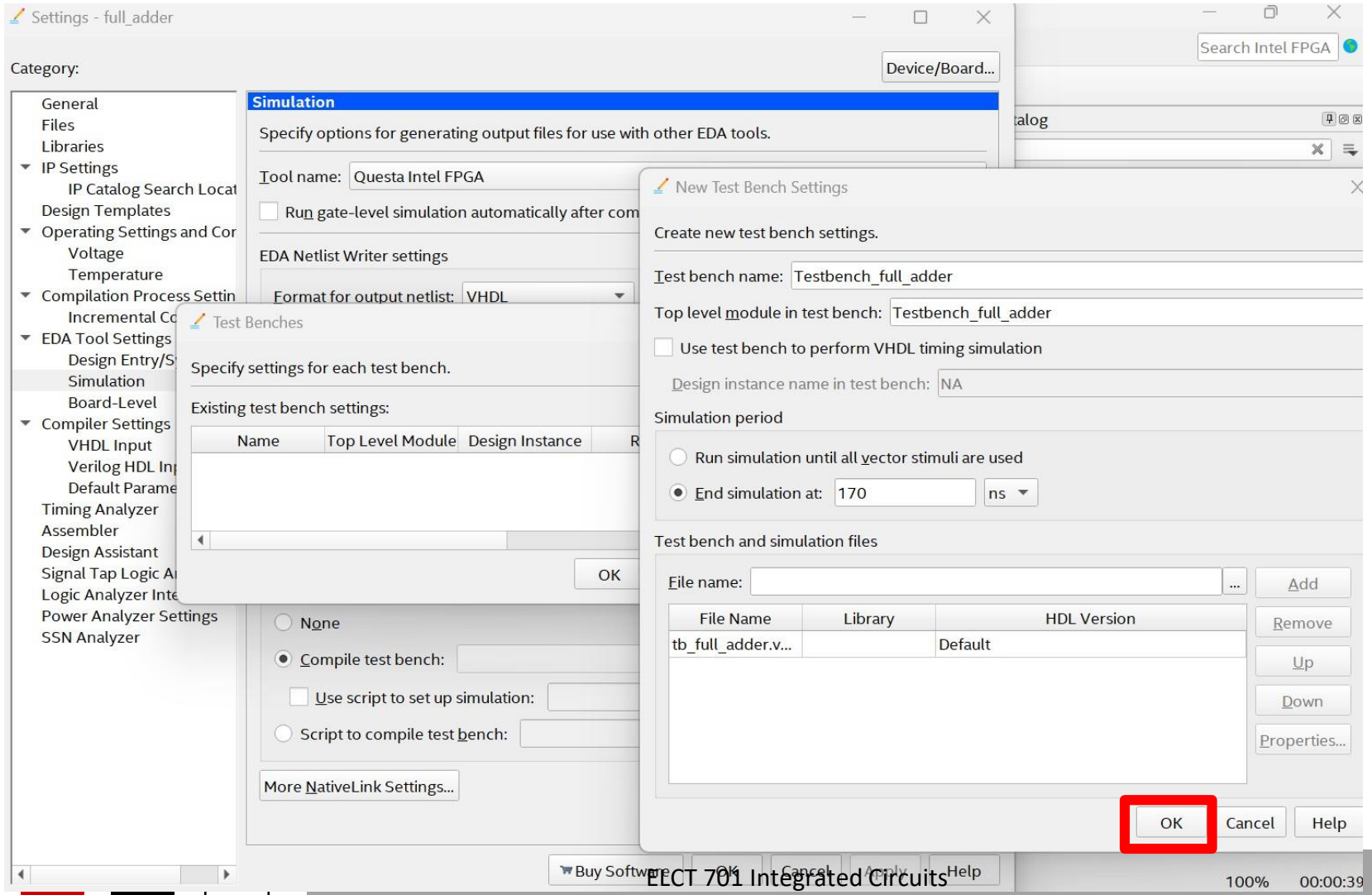

Settings - full_adder
Category:
Device/Board...
General
Files
Libraries
IP Settings
IP Catalog Search Locat
Design Templates
Operating Settings and Cor
Voltage
Temperature
Compilation Process Settin
Incremental Compilatio
EDA Tool Settings
Design Entry/Synthesis
Simulation
Board-Level
Compiler Settings
VHDL Input
Verilog HDL Input
Default Parameters
Timing Analyzer
Assembler
Design Assistant
Signal Tap Logic Analyzer
Logic Analyzer Interface
Power Analyzer Settings
SSN Analyzer
Simulation
Specify options for generating output files for use with other EDA tools.
Tool name: Questa Intel FPGA
Run gate-level simulation automatically after compilation
EDA Netlist Writer settings
Format for output netlist: VHDL
Time scale: 100 us
Output directory: simulation/questa
Map illegal HDL characters
Enable glitch filtering
Options for Power Estimation
Generate Value Change Dump (VCD) file script
Script Settings...
Design instance name:
More EDA Netlist Writer Settings...
NativeLink settings
None
Compile test bench: Testbench_full_adder
Test Benches...
Use script to set up simulation:
Script to compile test bench:
More NativeLink Settings...
Reset
Buy Software
OK
Cancel
Apply
Help


Test Benches
Specify settings for each test bench.
Existing test bench settings:
New...
Name
Top Level Module
Design Instance
Run For
Testbench_full...
Testbench_full...
NA
170 ns
Edit...
Delete
OK
Cancel
Help

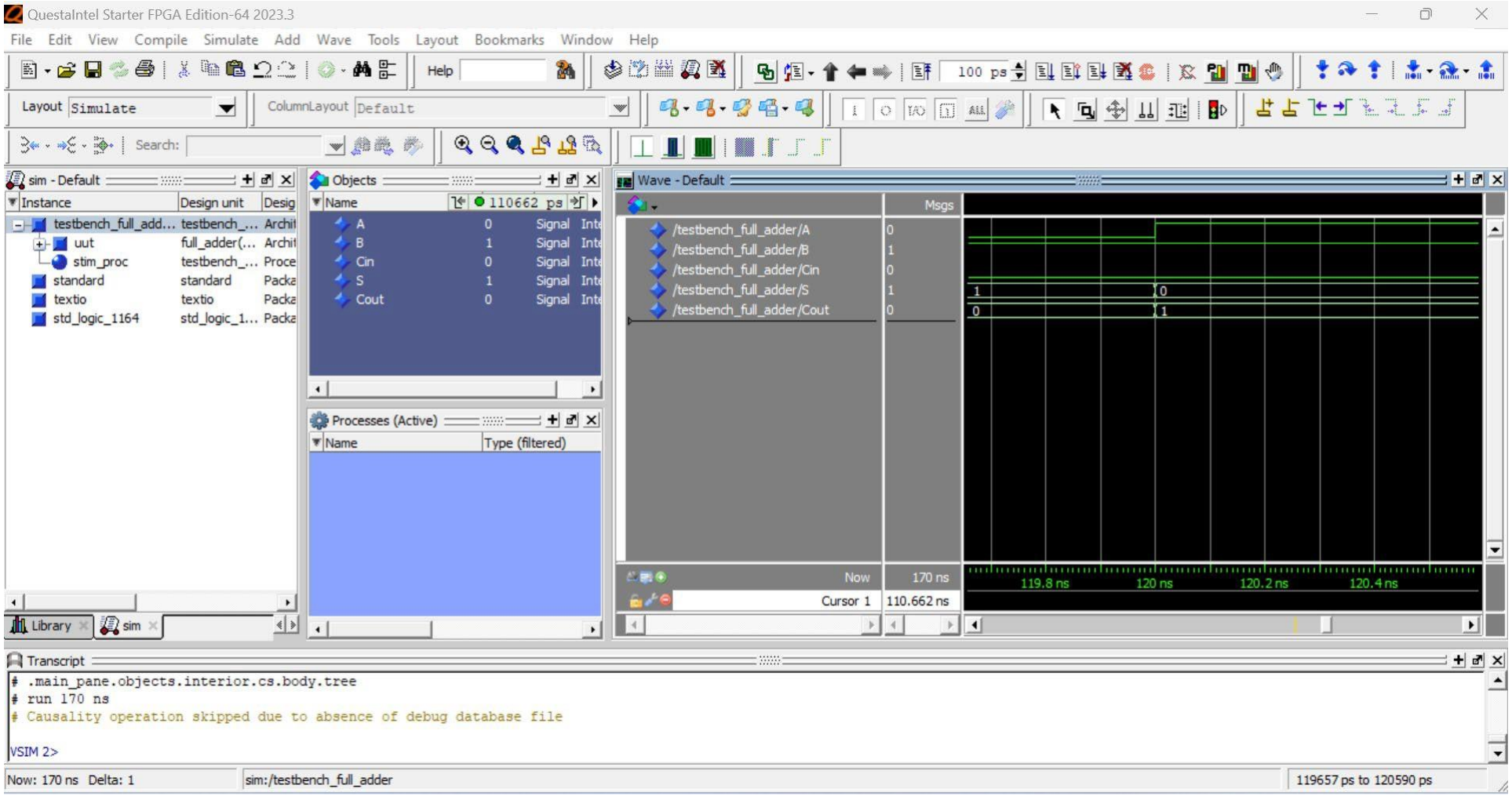
Setup the testbench



Setup the testbench



View the outputs using Questa



Thank you