Faculty of Information Engineering & Technology
Electronics Department
Course: Very Large Scale Integration [ELCT 904]

VHDL Synthesis using Intel Quartus

In this exercise you will synthesize FPGA code for Lane detection for self-driving cars and test it using remote lab.

1. Download Intel Quartus Synthesis Software Lite Edition using this link:

   https://www.intel.com/content/www/us/en/products/details/fpga/development-tools/quartus-prime/resource.html

2. Watch the tutorial Video “FPGA Vision -FPGA Remote Lab” by Prof. Marco Winzker to synthesize the lane detection VHDL code.

   Link: https://www.youtube.com/watch?v=H4WishN64TA

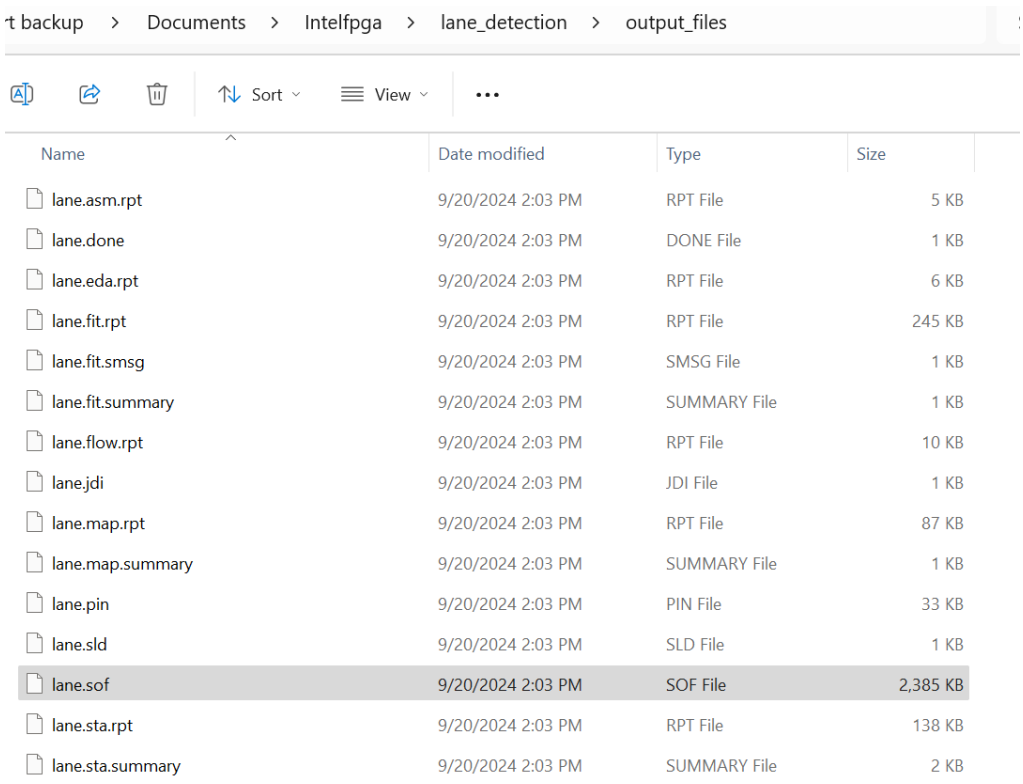
   VHDL Code Link:https://github.com/Marco-Winzker/FPGA-Vision/tree/master/FPGA-Design

3. Create an account to access Intel Cyclone V FPGA using this link:

   https://fpga-vision-lab.h-brs.de/weblab/invitation/1b69632240314530aa7d8a8e389cb1f2/register

4. Login to your account using this link:
   https://fpga-vision-lab.h-brs.de/weblab/login.

5. Upload the .sof file from the output_files folder in your project directory to the remote lab website.



6. Upload an image of your choice and report the output image and the power consumption