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SUPPLEMENTARY INFORMATION:
Highly Efficient Superconducting Diodes and Rectifiers for Quantum Circuitry

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Supplementary Information of 'Highly Efficient Superconducting Diodes and Rectifiers for Quantum Circuitry'

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S1. REPRODUCIBILITY OF SUPERCONDUCTING DIODE PERFORMANCE

The forward and reverse critical currents (I_c^+ and I_c^-, respectively) extracted from I-V sweeps are shown in Fig. S1 vs. out-of-plane magnetic field (B_z) for different values of the

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EuS magnetization (M_{EuS}). The experimental values are blue and orange.

The black dashed lines are the results from

$$\begin{aligned} I_{\mathrm{c}}^{+} &= \min(I_c + aB_z + I_{\mathrm{sM}}, I_c + dI_c - aB_z + I_{\mathrm{sM}}) \\ I_{\mathrm{c}}^{-} &= \min(I_c - aB_z - I_{\mathrm{sM}}, I_c + dI_c + aB_z - I_{\mathrm{sM}}). \end{aligned} \tag{1}$$

Here, I_{sM} is the Meissner current induced by the EuS magnetization (type C superconducting diode (SD) effect in Ref. [1]), I_c and $I_c + dI_c$ the critical currents of the SD edges, and a determines the Meissner current induced by B_z, which is required for the type A SD effect described in Refs. [1–3]. The low $|B_z|$ results in Fig. S1 were analyzed using Eq. 1, and the relevant parameters are shown in Table S1, stressing the remarkable similarity between the different SDs.

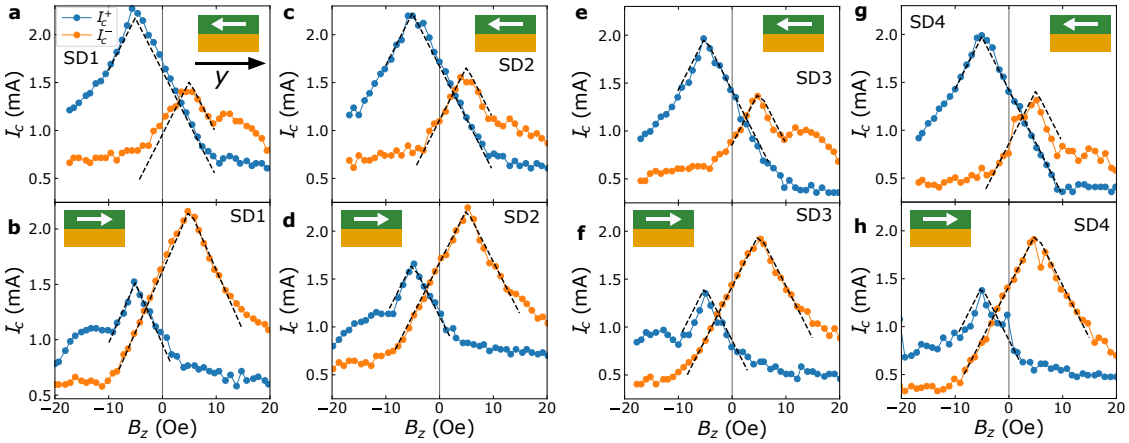

Figure S1. **Forward and reverse critical current dependence of the single superconducting diodes SD1, SD2, SD3, and SD4 on the out-of-plane magnetic field B_z at 1.7 K.** In the upper row (a, c, e, and g), the EuS magnetization is aligned towards $-y$ and in the upper row (b, d, f, and h) towards $+y$. SD1 and SD2 (and S3 and S4) are 100 μm away and the distance between SD2 and SD3 is approximately 1 mm.

	I_c^0 (mA)	δI (mA)	a (mA/T)	I_{sM} (mA)
SD1	1.29	1.11	0.11	0.33
SD2	1.29	1.11	0.11	0.28
SD3	1.14	1.11	0.11	0.28
SD4	1.14	1.11	0.11	0.28

Table S1. Parameters extracted from the SD model used to obtain the black dashed lines in Fig. S1. I_{sM} reverses sign when switching M_{EuS}.

S2. MAGNETIC FIELD DEPENDENCE OF THE SUPERCONDUCTING RECTIFIER CRITICAL CURRENTS

The forward and reverse critical currents of the superconducting rectifier shown in the main manuscript are shown in Fig. S2 vs. B_z for the different magnetization orientations of the EuS. Three different sweeps were measured for each B_z and the error bars measure the deviation in I_c between them. Figures S2d and S2e illustrate the behavior when half the diodes are reversed. The I-V curves show multiple steps, a consequence of the different I_{c}^{+} and I_{c}^{-}.

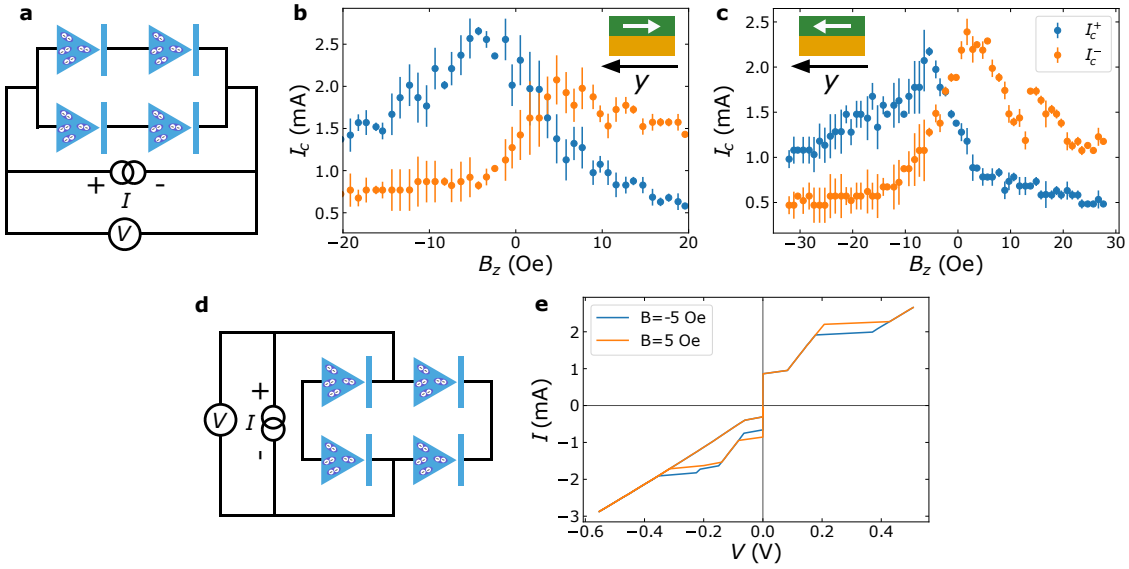

Figure S2. **Forward and reverse critical currents for the superconducting rectifier.** (a) Measurement circuit used to extract the forward and reverse critical currents for the two M_{EuS} orientations shown in (b) and (c). (d) Reference measurement circuit. (e) Typical I-V curves obtained in the measurement configuration shown in panel d. The error bars in panels b and c are obtained from three I-V measurements. The measurement temperature is 1.7 K.

S3. SUPERCONDUCTING DIODE BRIDGE PERFORMANCE FOR DIFFERENT LOAD RESISTORS

The raw data measured to obtain the load resistor (R) dependence of the output voltage in Fig. 2 of the main manuscript is shown in Fig. S3.

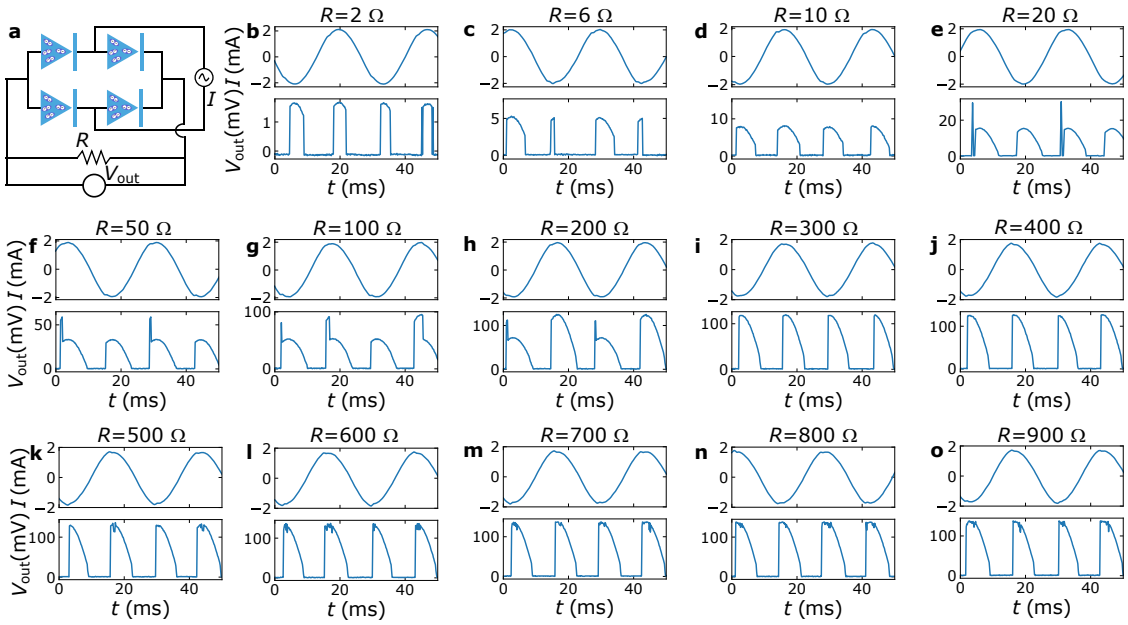

Figure S3. **Full wave superconducting rectifier performance vs. load resistor (R).** (a) Measurement circuit where the input current (I), output voltage ($V_{\rm out}$) and load resistor (R) are defined. (b)-(o) I and $V_{\rm out}$ vs. time. R is indicated for each panel. The measurement frequency is 37 Hz and the temperature is 1.7 K.

A. Resistor model

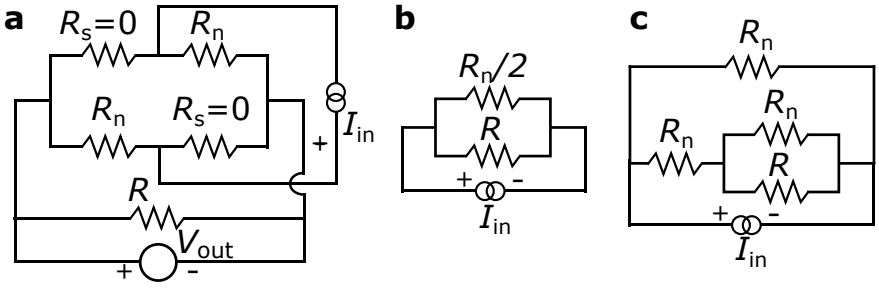

Figure S4. **Equivalent resistor circuits used to understand the superconducting rectifier performance.** (a) Measurement circuit where the input current ($I_{\rm in}$), output voltage ($V_{\rm out}$), and load resistor (R) are defined. (b) Simplified circuit corresponding to panel a. (c) Equivalent circuit describing the rectifier when one of the forward diodes is resistive.

The resistor model in Fig. S4a is used to understand the measured signals. For positive $I_{\rm in}$, the lower left and upper right diodes are reversed. This means that, for $I_{\rm in} > 2\min(I_{\rm c}^{+}, I_{\rm c}^{-})$, they acquire a resistance $R_{\rm n}$. As shown in Fig. S4a, since the upper left and lower right

diodes remain superconducting, the voltage drop across them is zero, resulting in a negative output voltage ($V_{\rm out}$).

We evaluate the efficiency of the rectifying operation for $|I_{\rm in}| > 2\min(I_{\rm c}^{+}, I_{\rm c}^{-})$ using the circuit in Fig. S4a, which can be simplified to the circuit shown in Fig. S4b, which shows that the output resistor is now parallel with two resistive SDs. As a consequence, the output signal can be expressed as a function of R using

$$V_{\rm out}/I_{\rm in} = \frac{R}{2R/R_n + 1}, \tag{2}$$

which is shown by the solid lines in Fig. 2d of the main manuscript. Using Eq. 2 to fit the measured data by least squares gives $R_n = 154\,\Omega$, which is comparable with the $R_n \approx 200\,\Omega$ obtained from the slope of the I-V curves in Fig. 1f. The current efficiency is represented in Fig. 2e, where the black line is the expected efficiency

$$I_{\rm out}/I_{\rm in} = P_{\rm out}/P_{\rm in} = \frac{1}{2R/R_{\rm n} + 1}, \tag{3}$$

extracted from Fig. 2e with $R_n = 154\,\Omega$, where $I_{\rm out(in)}$ and $P_{\rm out(in)}$ are the output (input) current and power, respectively. The black dots are obtained from the experimental data and agree well with the model for high R. However, for $R < 200\,\Omega$, the data in Fig. 2e shows two sets of peaks with a factor of two difference in the amplitude (Fig. S3) which do not agree with Eq. 3. We explain these lower-amplitude peaks considering that either SD1 or SD4 becomes resistive. This results in the equivalent circuit shown in Fig. S4c, which gives the following expression for the current efficiency

$$I_{\rm out}/I_{\rm in} = \frac{1}{2\left(\frac{3R}{2R_{\rm n}} + 1\right)}. \tag{4}$$

When $R \ll R_{\rm n}$, the efficiency given by Eq. 4 is two times smaller than Eq. 3. This is caused by the increase in the resistance of the current path that goes through the load resistor R, which penalizes the circuit efficiency even for $R = 0$. Using $R_n = 154\,\Omega$, Eq. 4 results in the red line in Fig. 2e, which shows good agreement with the experiment at low R. This result is independent of which SD is turning resistive (upper left or lower right in Fig. S4a). Two possible reasons can explain this premature transition to the resistive state: 1. Heating induced by the resistive SDs decreases $I_{\rm c}^{+}$ of the superconducting SDs. 2. Small differences in $I_{\rm c}^{+}$ between the SDs in the bridge. These effects do not occur for higher R because the

current load on the forward diodes decreases with increasing R. Nevertheless, the maximal efficiency achieved is 42±2%, a remarkable metric for such a new device.

1. *Effect of additional contact resistances*

As explained in the main manuscript, the load resistor R was at room temperature and the rectifier was bonded to a chip carrier to perform the realized experiments. Since the bonds were realized using a wedge bonding technique, the V regions near the bonds can also be potentially damaged. We have thus considered the effect of these resistances in a modified model which results in

$$V_{\mathrm{out}}/I_{\mathrm{in}} = \frac{R}{2(R+R_c)/R_n + 1}, \tag{5}$$

where R_c is the contact resistance and accounts for the two contacts connected to R. The results of fitting Eq. 5 to the experimental data, shown in Fig. S5, indicate that $R_c < 50\ \Omega$ is sufficient to account for the discrepancy.

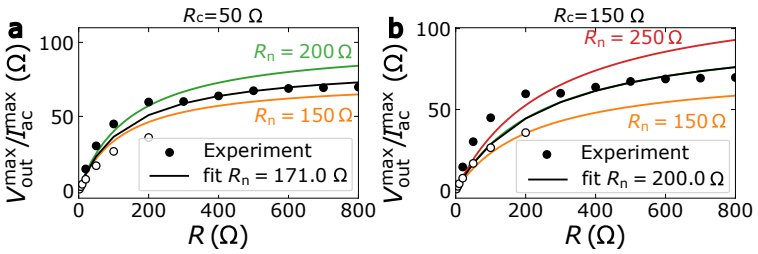

Figure S5. **Influence of contact resistances R_c on the R_n extracted by the resistor model.** Fits for $R_c = 50\,\Omega$ and $R_c = 200\,\Omega$ are shown in panels (a) and (b), respectively. Note that the resistance per individual contact is $R_c/2$.

2. *Resistance of the individual diodes*

To determine the resistance of the individual diodes in the resistive state, we measured the rectifiers characterized here on a different cooldown and using the three-terminal configurations displayed in Fig. S6a. The contact numbers (1, 2, 3, and 4) are specified in the inset whereas the circuit for each measurement is shown in the legend following the convention: $I(I_+, I_-)$, $V(V_+, V_-)$. The results in Fig. S6a show the $I-V$ characteristics obtained at $B = 0$ for each measurement circuit in the full measurement range and Fig. S6b shows the

results for the resistive range at $V > 0$ only. Linear fits to this range have been used to obtain the equivalent resistance of each configuration when the SDs are resistive. Finally, R_i of each diode has been obtained from these values using the slopes obtained from these fits and assuming that the four SDs are resistive, following the system of equations:

$$\begin{aligned} V_1/I &= \frac{R_1(R_3+R_4)}{R_1+R_2+R_3+R_4} \\ V_2/I &= \frac{R_2(R_3+R_4)}{R_1+R_2+R_3+R_4} \\ V_3/I &= \frac{R_3(R_1+R_2)}{R_1+R_2+R_3+R_4} \\ V_4/I &= \frac{R_4(R_1+R_2)}{R_1+R_2+R_3+R_4} \end{aligned} \tag{6}$$

where V_i/I is the inverse of the slope of the $I-V$ curve measured using the contacts enclosing SDi ($I(1,2)\,(3,2)$ encloses SD4, $I(1,2)\,(4,2)$ encloses SD2, $I(1,2)\,(1,3)$ encloses SD3, and $I(1,2)\,(1,4)$ encloses SD1) and R_i the normal state resistance of SDi. The resistances obtained for each diode (see inset of Fig. S6a) are: R(SD1, SD3, SD4)$\approx 209\,\Omega$, and R(SD2)$\approx 210\,\Omega$. This result, obtained by numerical means due to the nonlinearity of Eq. 6, indicates that the four SD resistances are practically identical. This is remarkable since the three terminal measurements also include the resistance of contacts 1 and 2.

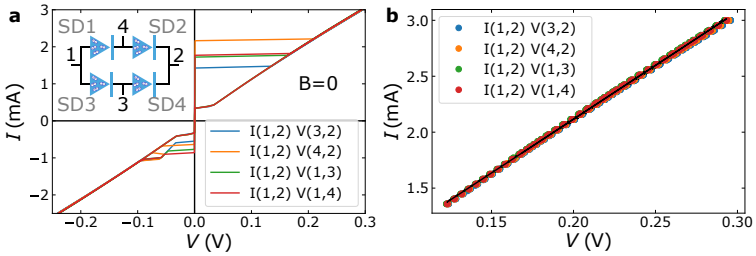

Figure S6. **Three terminal measurements to extract the resistances of the individual SDs at $B = 0$.** (a) Full range (b) V range used to obtain the resistance through linear fits. The inset in panel a shows a schematic of the measured rectifier where the SDs are labeled in gray and the contacts in black. The measurement configurations are indicated in the legends.

B. 102 kHz results

The superconducting rectifier circuits have been measured with input frequencies (f) up to 102 kHz. The results at this f are shown in Fig. S7

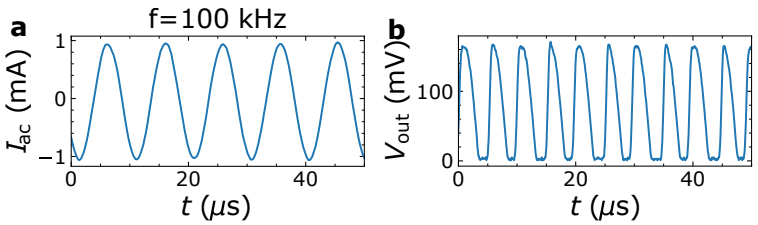

Figure S7. **Full wave superconducting rectifier performance at f =102 kHz.** (a) Input current I_{ac} and (b) output voltage (V_{out}) vs. time. The measurement circuit is the same as in Fig. S3a without the load resistor. I has been smoothed using a moving average filter with a 13-point window and the measurement temperature is 1.7 K.

S4. ROLE OF SMOOTHING CAPACITOR

A. Frequency dependence

The role of a smoothing capacitor on the superconducting rectifier circuit at different f is shown in Fig. S8. As shown in Fig. S8i, the amplitude of the ripple oscillations decreases with increasing frequency following c/f, where c is a constant [4]. An additional feature of the data is that the average signal increases slightly with f (3% within the measured range). Such an increase may be caused by the capacitor discharging current which, as explained in the main manuscript, can help the reversed diodes to become superconducting earlier, thus increasing the average output voltage provided by the superconducting diode bridge.

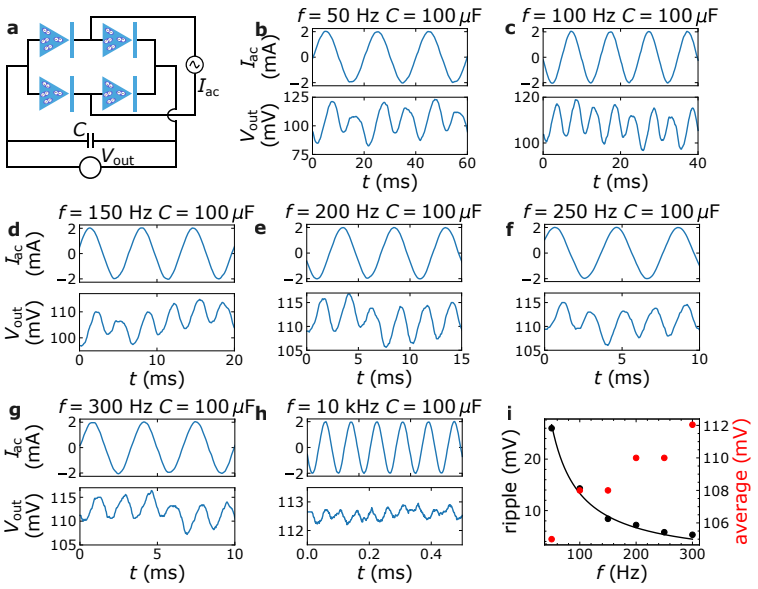

Figure S8. **Frequency dependence of the rectifier signals with a $C = 100\,\mu$F smoothing capacitor.** (a) Measurement circuit. (b)-(h) Applied ac current and measured output voltage (V_{out}). V_{out} and I have been smoothed using a moving average filter with a 5-point window. (i) Frequency dependence of the ripple amplitude and average of the output signal. The measurement temperature is 1.7 K. The line is a fit to ripple$= c/f$ where the resulting $c = (1330 \pm 30)$ mVHz.

B. Calculations

To further understand the measured data and estimate the maximal efficiencies achievable by a superconducting rectifier, we have calculated the effect of a smoothing capacitor on the output signal from a rectifier. The simulated circuit is shown in Fig. S9a. To obtain the voltage across the capacitor (V_{out}), we first calculate the current (I_{cap}) using

$$\frac{dI_{\mathrm{cap}}}{dt} = \frac{I_{\mathrm{cap}}}{CR_{\mathrm{n}}/2} - \frac{1}{R_{\mathrm{in}}}\frac{dV_{\mathrm{in}}}{dt} = 0, \tag{7}$$

where V_{in} is the time-dependent input voltage, which is defined using

$$V_{\mathrm{in}} = \begin{cases} V_0|\sin(\omega t)|, & \text{if } |\sin(\omega t)| > 2I_{\mathrm{c}}^{-},\ \cos(\omega t) > 0 \\ V_0|\sin(\omega t)|, & \text{if } |\sin(\omega t)| > I_{\mathrm{r}},\ \cos(\omega t) < 0 \\ 0, & \text{otherwise.} \end{cases} \tag{8}$$

Equation 7 assumes that $R_{\rm in} \gg R_{\rm n}$, as the experiment, and gives the following expression for $I_{\rm cap}$:

$$I_{\rm cap} = e^{-\frac{2t}{R_{\rm n}C}} \int_0^t \frac{1}{R_{\rm in}} \frac{dV_{\rm in}}{dt} e^{\frac{2t}{R_{\rm n}C}} dt. \tag{9}$$

Integrating Eq. 9 by parts to avoid the $dV_{\rm in}/dt$ term, which has abrupt jumps, we obtain the following expression

$$I_{\rm cap} = \frac{V_{\rm in}(t)}{R_{\rm in}} - \frac{2e^{-\frac{2t}{R_{\rm n}C}}}{R_{\rm in}R_{\rm n}C} \int_0^t \frac{1}{R_{\rm in}} V_{\rm in}(t) e^{\frac{2t}{R_{\rm n}C}} dt, \tag{10}$$

where we used that $V_{\rm in}(t = 0) = 0$. The first term in the right side of Eq. 10 is the applied current and the second one accounts for the charging and discharging of C. $V_{\rm out}$ is determined using

$$V_{\rm out} = \frac{1}{C} \int_0^t I_{\rm cap} dt. \tag{11}$$

It is illustrative to solve Eq. 11 for

$$V_{\rm in} = \begin{cases} V_0, & \text{if } t > 0 \\ 0, & \text{if } t \leq 0, \end{cases} \tag{12}$$

which gives

$$V_{\rm out} = \frac{V_0 R_{\rm n}}{2R_{\rm in}} \left(1 - e^{-\frac{2t}{R_{\rm n}C}}\right) \tag{13}$$

as expected [4]. Note that a simple resistor model without C gives $V_{\rm out} = \frac{V_0}{2R_{\rm in}/R_{\rm n}+1}$. To obtain $V_{\rm out} = \frac{V_0 R_{\rm n}}{2R_{\rm in}}$ as in Eq. 13 for $t \gg R_{\rm n}C/2$ one needs to consider that $R_{\rm in} \gg R_{\rm n}$, which is the assumption by the model.

Equation 11 has been solved for $V_{\rm in}$ defined by Eq. 8 using Python's SymPy package [5]. The parameters used are $\omega = 2\pi f$ with $f = 1$ kHz and $R_{\rm n} = 167\,\Omega$. Figure S9b shows results for $2I_{\rm c}^-/I_{\rm max} = 0.85$ and $I_{\rm r}/I_{\rm max} = 0.5$, and Fig. S9c shows results for $2I_{\rm c}^-/I_{\rm max} = 0$ and $I_{\rm r}/I_{\rm max} = 0$. Here, $I_{\rm max} = V_0/R_{\rm in}$. Figs. S9b and S9c show an initial charging time that requires several cycles because the RC time constant of the circuit $t_c = (R_{\rm n}C)/2 = 0.8$ ms does not allow for fully charging the capacitor within a single cycle. After this transient behavior, the simulated signals show small oscillations with average values of 44% and 63% of the maximum output voltage $V_{\rm max}$ obtained without C and shown as dashed lines in Figs. S9b and S9c. Note that the average value of $|sin(\omega t)|$ for a full cycle ($2/\pi \approx 0.637$) is very similar to the value obtained from Fig. S9c. As expected, the average output signal for $t > 5$ ms changes by less than 0.4% by the effect of C. We attribute this small difference to accumulated numerical errors.

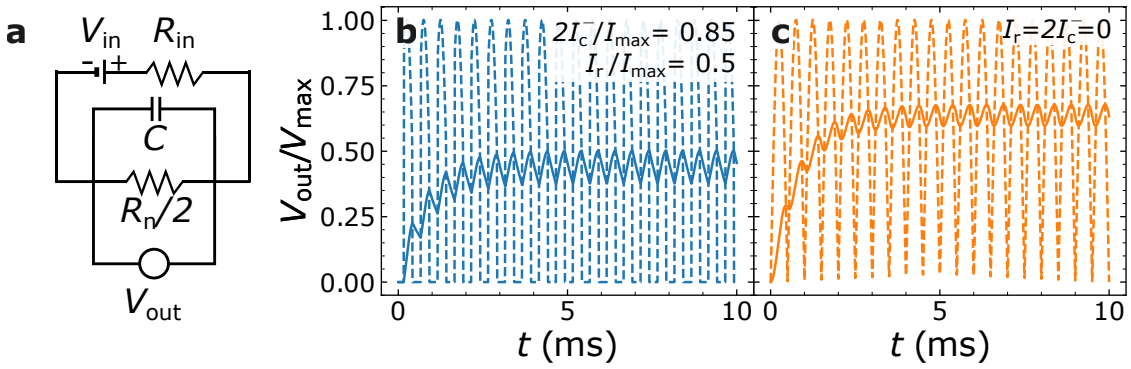

Figure S9. **Simulations on the effect of a smoothing capacitor C.** (a) Simulated circuit where the input voltage ($V_{\rm in}$), output voltage ($V_{\rm out}$), input resistor ($R_{\rm in}$), parallel resistor ($R_{\rm n}/2$), and capacitor $C = 10\,\mu$F are defined. (b) and (c) Normalized $V_{\rm out}$ vs. t. for the circuit with (solid line) and without (dashed line) capacitor. The normalized $I_{\rm c}^+$ and $I_{\rm c}^-$ values are indicated at the inset.

S5. REPRODUCIBILITY

A. Results on a second V/EuS rectifier

We patterned a second rectifier in the same V/EuS thin film as the rectifier discussed in the main manuscript. Both devices were designed to be identical and display similar properties, as illustrated in Fig. S10. Figure S10a shows that, for $B_z \approx -5$ Oe, there are two different $I_{\rm c}^+$ and $I_{\rm c}^-$. We attribute this behavior to the imperfect alignment of the EuS magnetization at the edges, resulting in some SDs having a slightly different critical current. Fig. S10c shows the R-dependence of the measured signal, which is remarkably similar to the results from the rectifier shown in the main manuscript. This is illustrated by the fitting results, which yield almost identical $R_{\rm n}$ values within 3%.

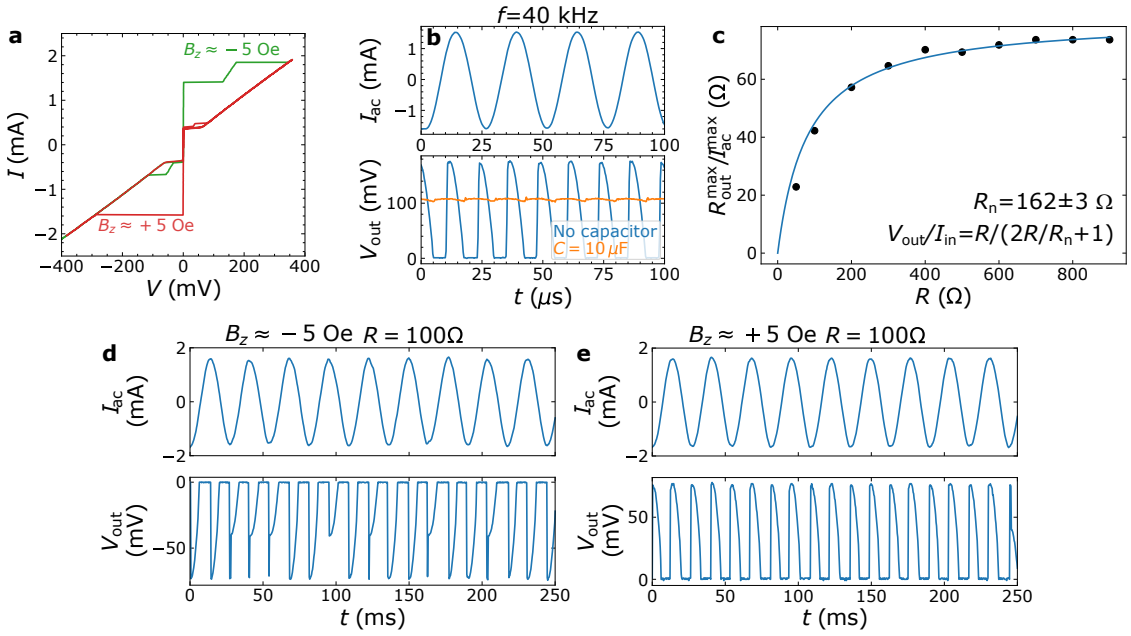

Figure S10. **Second V/EuS rectifier.** (a) Two-terminal I-V characteristics of the rectifier at $B_z \approx \pm 5$ Oe. (b) Ac to dc signal conversion at $f = 40$ kHz. (c) Load resistor dependence of the output signal (dots) and fit to the resistor model in the main manuscript (blue line, inset equation) showing that R_n is nearly identical to that of the first rectifier. (d) and (e) Reversible operation of the rectifier circuit with B_z. I_{ac} has been smoothed using a moving average filter with a 13-point window. The measurement temperature is 1.7 K.

B. Results on a niobium-based rectifier

To showcase the versatility of our superconducting rectifier circuit, we have also realized a rectifier in a niobium-based superconducting diode [Nb(5 nm)/Au(4 nm)/EuS(5 nm)]. In this case, the only difference in the design is that the SD width was reduced from 8 to 6 μm and larger B_z were applied to reduce the critical currents (Fig. S11a) and minimize heating. As shown in Fig. S11b, the output signal is significantly smaller than for the V/EuS rectifiers. This is due to the lower R_n of the Nb-based superconducting diodes, as obtained from the fitting. The reversible operation of the rectifier is shown in Figs. S11c and S11d. Note that, in this case, the performance is not as good as that of the V/EuS rectifiers because the diode efficiency $|\eta| = |I_c^+ - I_c^-|/(I_c^+ + I_c^-) < 0.33$. $|\eta| > 0.33$ guarantees that the forward diodes do not turn resistive when the reverse ones do, and the current through the forward diodes increases. Introducing a capacitor in the Nb-based diodes resulted in smaller signals, which

we attribute to the discharging currents interfering with the rectifier operation. We believe that the V-based rectifiers are more robust due to the higher $|\eta|$.

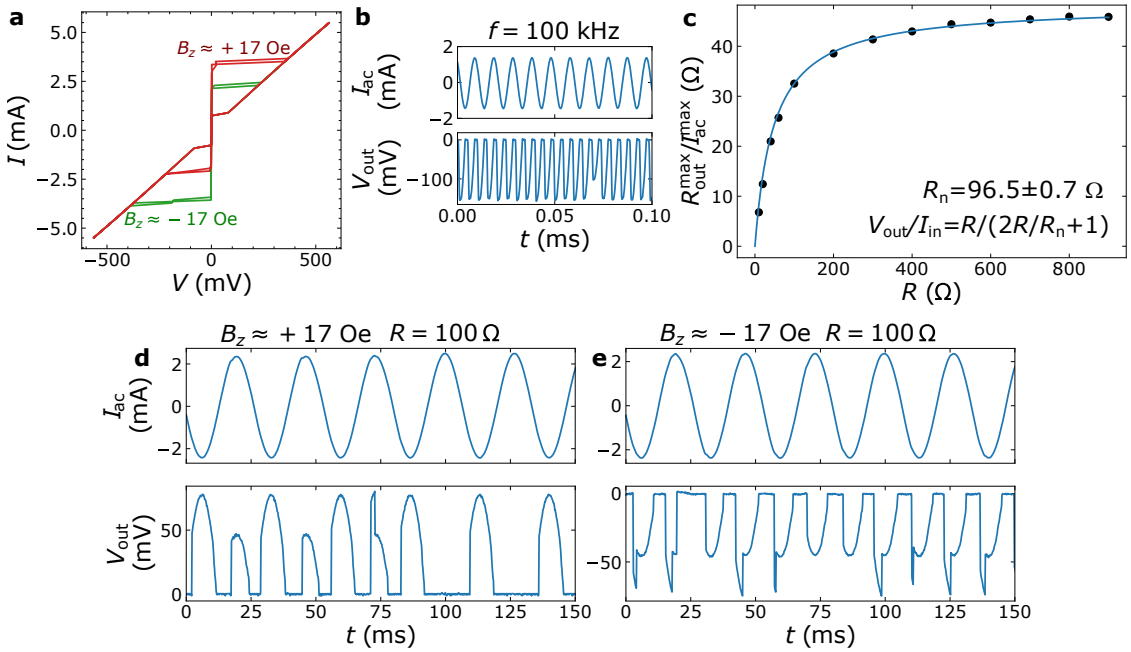

Figure S11. **Nb/Au/EuS rectifier.** (a) Two-terminal I-V characteristics of the rectifier. (b) Full wave rectifier at $f = 100$ kHz. (c) Load resistor dependence of the output signal (dots) and fit to the resistor model in the main manuscript (blue line, inset equation). (d) and (e) Reversible operation of the rectifier circuit with B_z. I_{ac} has been smoothed using a moving average filter with a 13-point window. The measurement temperature is 1.7 K.

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