Extending Silicon Transducer Temperature Range

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Abstract

The article considers the necessity of expanding the operational capabilities of mechanical sensors for the further development of science and technology. To solve the problem of extending the operating temperature range above +100°C for integral mechanical transducers with an insulating p-n junction, experimental studies are needed to optimize the design, fabrication technology, and metrological capabilities. The paper also discusses the development of a dielectrically insulated sensor using SOI technology. Research and development in this area is ongoing and aims to overcome the problems associated with limited operating temperature conditions and improve the metrological characteristics of the SOI.

The further development of science and technology requires a significant expansion of the operational capabilities of mechanical sensors. For this purpose, we are looking at work associated with the creation of high-temperature integral piezoresistive transducers (IPT). Semiconductor-itegrated transducers (IPTs) surpass traditional conductive transducers in most technical and economic aspects [1]. However, there are several challenges that hinder the development in this field, with the main one being limited operating-temperature conditions. Most of the IPTs currently available are designed to operate at low temperatures, up to +100°C. Yet, by improving insulation quality, it is possible to extend the upper limit to temperatures restricted by the onset of the material's intrinsic conductivity or the plastic deformation of the elastic element. Primarily, it is advisable to investigate the potential for expanding the operating temperatures of IPTs with silicon-based piezoresistors. Because of its well-studied characteristics, advantageous physical properties, and technological compatibility, silicon remains unrivaled by any other semiconductor.

The wide possibilities for expanding the operating temperature range of IPTs (Integrated Passive Transducers) have been opened up by modern advancements in microelectronic technology. Among the currently used methods of dielectric isolation, silicon-on-sapphire (SOS) technology [2] and silicon-on-insulator (SOI) technology [3] are of particular interest.

Based on the SOS (Silicon-on-Sapphire) technology, IPTs with dielectric isolation are being successfully developed, which are characterized by [2]:

- high metrological characteristics;
- high technological feasibility, particularly for flat elastic elements;
- excellent dielectric isolation between tensor resistors and elastic elements;
- operation within a temperature range up to the limit of silicon's intrinsic conductivity.

The development of IPTs with silicon elastic elements and silicon piezoresistors, interconnected and isolated from each other by a dielectric layer with a linear thermal expansion (CLTE) coefficient of matching, is considered promising [4]. The main technological operations for their fabrication are based on the process of creating integrated circuits with dielectric isolation using the silicon-on-insulator (SOI) method.

The advantages of IPT-SOI include:

- utilization of technologically advanced methods such as chemical etching for shaping;

- application of diffusion or ion implantation technology combined with other microelectronics processes;
- creation of a structure in IPT with a matched coefficient of linear thermal expansion (CLTE);
- possibility of using electro-adhesive bonding to connect IPT with the sensor housing.

It should also be noted that the influence of the isolating properties of the p-n junction on the metrological characteristics of IPT at temperatures above +100 ° C has not been sufficiently studied, and the actual operational limits are not defined. Therefore, the investigation of possibilities to expand the operating temperature range for IP with a p-n junction is an open question.

All the presented approaches do not exclude each other but complement one another, and therefore, they should be developed in parallel. SOS converters have obvious operational advantages, but silicon converters are more economically beneficial. Therefore, the question of expanding the upper limit of the temperature range for IPT with a p-n junction and the development of new solutions such as SOI remains relevant.

1 IPT with Insulating P-N Junction

IPT with an isolating p-n junction has advantages due to the well-developed manufacturing technologies and the merits of silicon as a material for the elastic element. Currently, IP with a p-n junction operates in the range of ±60°C, and therefore, it may be practically important to expand its operating range in the positive temperature region without switching to new materials or insulating substrates. A theoretical model that allows analyzing the characteristics of piezoresistors based on p-n junctions at elevated temperatures is discussed in Reference [5]. However, this question is still not explored sufficiently from a practical perspective.

Let us consider a priori information on this issue. The metrological characteristics of the bridge measurement circuit and the upper limit of the working temperature range of IPT with a p-n junction depend on the leakage currents of the piezoresistors and the shunt effect of the elastic element.

The temperature dependence of the resistance of an integrated piezoresistor is determined by the temperature-induced changes in the resistance of the resistive layer, R_{ch}, and the resistance of the "p-n junction - substrate (elastic element)", R_{sh}.

$$R_{in}(T) = \frac{R_{ch}(T)}{1 + \frac{R_{ch}(T)}{R_{sh}(T)}} \tag{1}$$

According to [5], express the temperature dependence of R_{ch} and R_{sh} as

$$R_{ch} = R_0 \left[1 + \alpha_0 \left(T - T_0\right)\right] \tag{2}$$

$$R_{sh} = \frac{2 \cdot V_{in}}{I_{rev0} W^2 L} e^{-\beta\left(1 - \frac{T_0}{T}\right)} \tag{3}$$

where: R_0 is the resistance of the piezoresistor under normal conditions, α is the temperature coefficient of the resistive layer of the piezoresistor, which has a positive sign in the temperature range of 0°C ÷ 200°C; β- the coefficient depending on the law of increasing reverse current. According to Table II in [6], it is determined by the approximate value of $\beta = (37 \div 39)$. That is, $I_{rev} = I_{\text{rev } 0} \cdot e^{38 \cdot \left(\frac{T-293}{T}\right)}$.; I_{rev0} is the initial value of the reverse current; L is the number of squares in the piezoresistor channel; W is the width of the piezoresistor channel; V_{in} is the voltage supplied to the piezoresistor.

As the temperature increases, the resistance of the piezoresistive layer increases, while R_{sh} decreases due to the exponential growth of the reverse current of the p-n junction. The appearance of a maximum on the temperature dependence curve $R_{in} = f(T)$ can be considered as the upper limit

of the piezoresistor's functionality, denoted as T_{max}. The position of the maximum is determined by the condition $\frac{dR_{in}}{dT} = 0$.

$$2\ln\left[\frac{T_0}{T} + \alpha_0 T_0\left(1 - \frac{T_0}{T}\right)\right] + \beta\left(1 - \frac{T_0}{T}\right) = \ln\frac{2V_{in}\alpha_0 T_0}{\rho_{ch} L^2 \beta I_{rev0} W^2} \tag{4}$$

where ρ_{ch} is the resistivity of the resistive layer of the piezoresistor ; T_{max} the greater the right-hand side of equation (4).

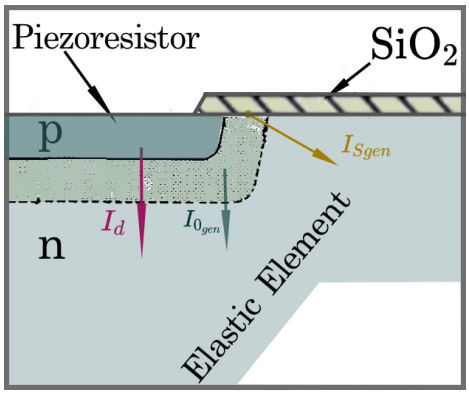

Figure 1: Components of leakage current (reverse current) I_{rev} and its areas of occurrence

The most noticeable influence has the initial value of the reverse current I_{rev0}. The reverse current of the p-n junction, or the reverse current of the I-V characteristic (I_{rev}), can be divided into three components [6] (see Figure 1):

I_{0gen} - the current generated by charge carriers in the depleted region of the p-n junction within the volume of the elastic element. I_{Sgen} - the current generated by the charge carriers in the depleted region of the p-n junction on the surface of the elastic element. I_d - the diffusion component of the reverse current. Therefore, the total reverse current is given by the equation:

$$I_{rev} = I_{0_{gen}} + I_{Sgen} + I_d \tag{5}$$

The main contribution at temperatures up to $+100°C$ is made by the component I_{Sgen}. The density of this current is $(0.08 \div 1.6) \times 10^{-4}\ A \cdot m^{-2}$.

The upper limit of the operating range also depends on the voltage applied to the piezoresistor. As V_{in} increases, R_{sh} increases, reducing the influence of the resistance of the elastic element. The increase in R_{sh} leads to a shift of T_{max} toward higher temperatures. However, this effect is observed under limited conditions, depending on the magnitude of the breakdown voltage of the p-n junction.

The highest value of T_{max} corresponds to the configuration in which no reverse bias potential is applied, i.e., "piezoresistor-substrate (elastic element)" with $V_{ch-ee} = 0$. Increasing the potential for reverse bias leads to an increase in I_{rev}.

Figure 2 shows plots of the dependence of R_{in} (input resistance), sensitivity coefficients, and normalized null output on temperature for transducers made according to [7].

To solve the problem of extending the operating temperature range above +100°C for IPT with p-n junction experimental studies are required to optimize the design, manufacturing technology and evaluation of metrological capabilities.

2 IPT with Dielectric Isolation

Based on the analysis of existing technological capabilities [1], existing design solutions [8], and the experimental verification of several technological approaches, it can be concluded that it is possible to develop IPT with dielectric insulation of monocrystalline piezoresistors using a low temperature glass layer on a monocrystalline silicon elastic element. To develop SOI-type IPT, it is necessary

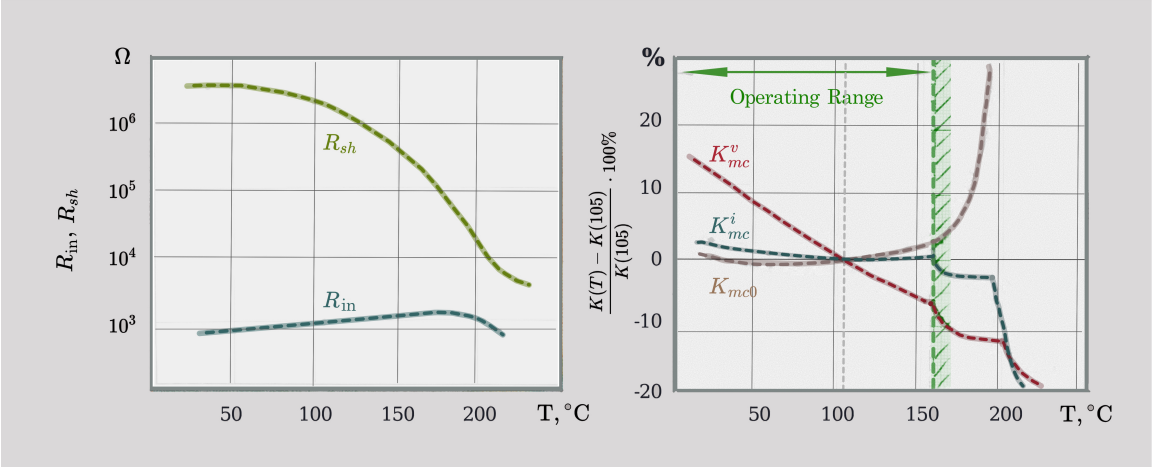

Figure 2: Temperature dependence of parameters IPT made according to to^{17} : (a) R_{in} - input resistance of full bridge measuring circuit (MC) ; R_{sh} - resistance "p-n junction - substrate (elastic element)" (b) K_{mc0} - normalized zero output of MC; K^v_{mc} - bridge sensitivity when MC is fed with stabilized voltage $V_{in} = 5$ V; K^i_{mc} - bridge sensitivity when MC is fed with stabilized current $I_{in} = 5$ mA.

to address the challenges primarily associated with developing the silicon-glass-silicon structure and then optimize the design and technological solutions to ensure metrological characteristics comparable to existing IPTs. Figure 3 illustrates the structure of such a transducer [9].

The sequence of manufacturing operations is as follows. Two silicon wafers of n-type (p-type can also be used) oriented in plane (100) are used. Piezoresistive diffusion p^+-type channels of depth $(2 \div 2.5)\mu m$ are formed on wafer A using oxidation, photolithography, and boron diffusion operations (to doping levels greater than $1 \times 10^{19} cm^{-3}$). Also formed p^+-type diffusion contact regions with a depth of $(5 \div 6)\mu m$ and chemical anisotropic etching of alignment marks as recesses at $(5 \div 6)\mu m$. On one side of the wafer $Wafer_1$, where diffusion channels are formed, and on either side of the wafer $Wafer_2$, a layer of glass with a thickness of $(0.8 \div 1.2)\mu m$ is deposited using the spin coating of an alcohol suspension. Subsequently, the wafers are aligned with each other along the base cuts and fused under a slight pressure at a temperature of $(750 \div 800)^{\circ C}$. Using a 25% solution of KOH, wafer $Wafer_1$ is etched until the alignment marks and diffusion contacts become visible. The reverse side of $Wafer_2$ is etched anisotropically to form the required configuration of the elastic elements. Then, using photolithography and isotropic chemical etching processes, resistors are defined, consisting of a piezoresistive channel with a thickness of $(2 \div 2.5)\mu m$ surrounded by a protective layer of $Wafer_1$ material with a thickness of $(2.3 \div 3.5)\mu m$. It is also possible to leave areas of silicon from $Wafer_1$ underneath the conductive tracks and contact pads, as shown in Figure 4 (B). Aluminum is deposited on the side of the piezoresistors through thermal evaporation in a vacuum, and using photolithography, current-carrying tracks and contact pads are formed. After the annealing process, the wafers are separated into individual IPT crystals.

The layer of material $Wafer_1$ with resistance R_w and thickness H_w is intended to protect the main piezoresistor channel R_{ch}. The main metrological characteristics of the piezoresistors, such as the resistance value R_{chw}, the gauge factor K_{chw}, the temperature coefficient of resistance α_r^{chw}, and the temperature coefficient of sensitivity α_k^{chw}, are determined by the following relationships:

$$R_{chw} = \frac{R_{ch} \cdot R_w}{R_{ch} + R_w} = \frac{\rho_w R_s \cdot L_w}{R_s \cdot H_w + \rho_w \frac{L_w}{L_{ch}}}; \tag{6}$$

$$K_{chw} = \frac{1}{R} \cdot \frac{dR}{d\varepsilon} = \frac{R_s \cdot K_w H_w + \rho_w K_{ch} \frac{L_w}{L_{ch}}}{R_s H_w + \rho_w \frac{L_w}{L_{ch}}}; \tag{7}$$

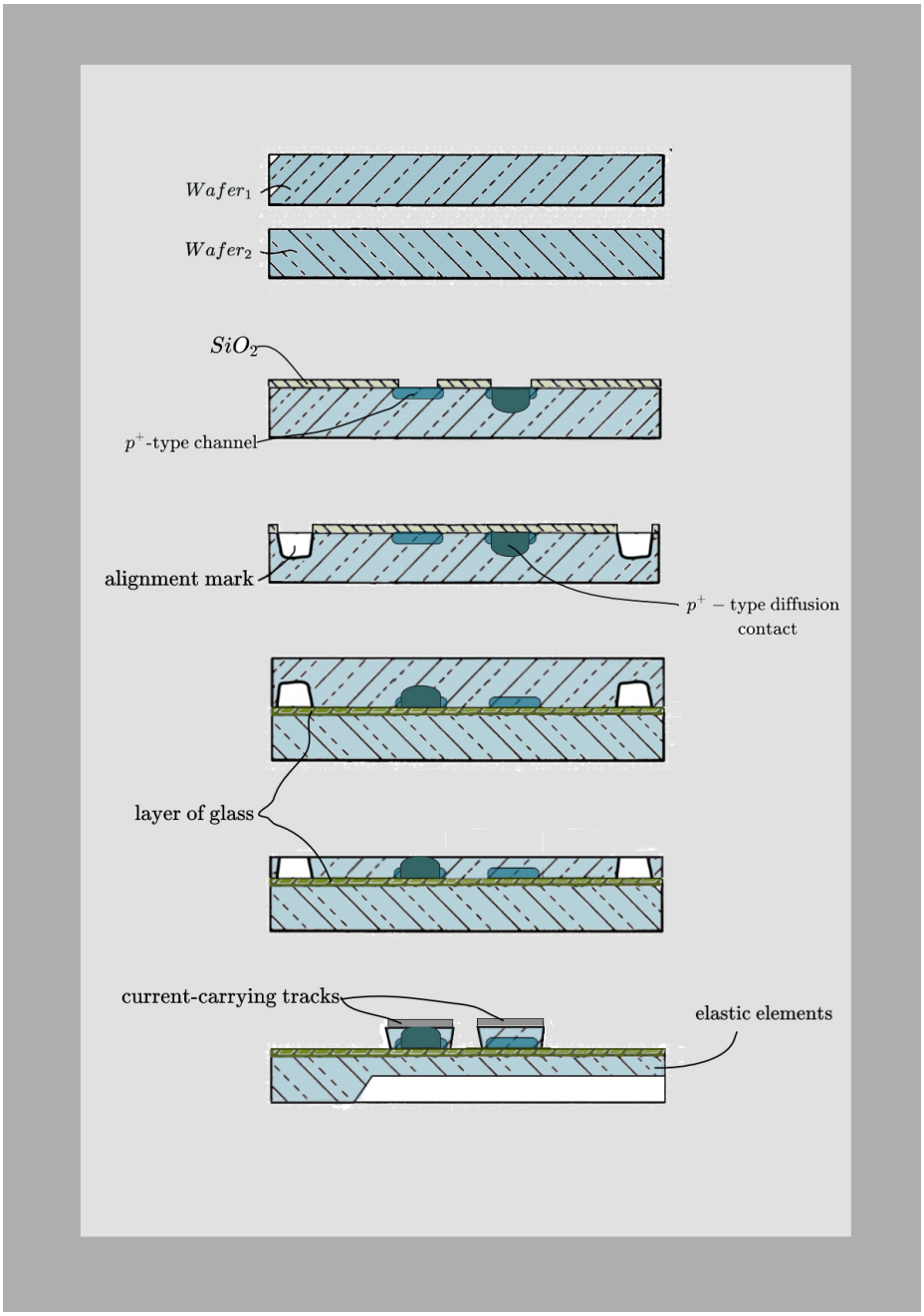

Figure 3: Sequence of manufacturing operations of high-temperature IPT by SOI method.

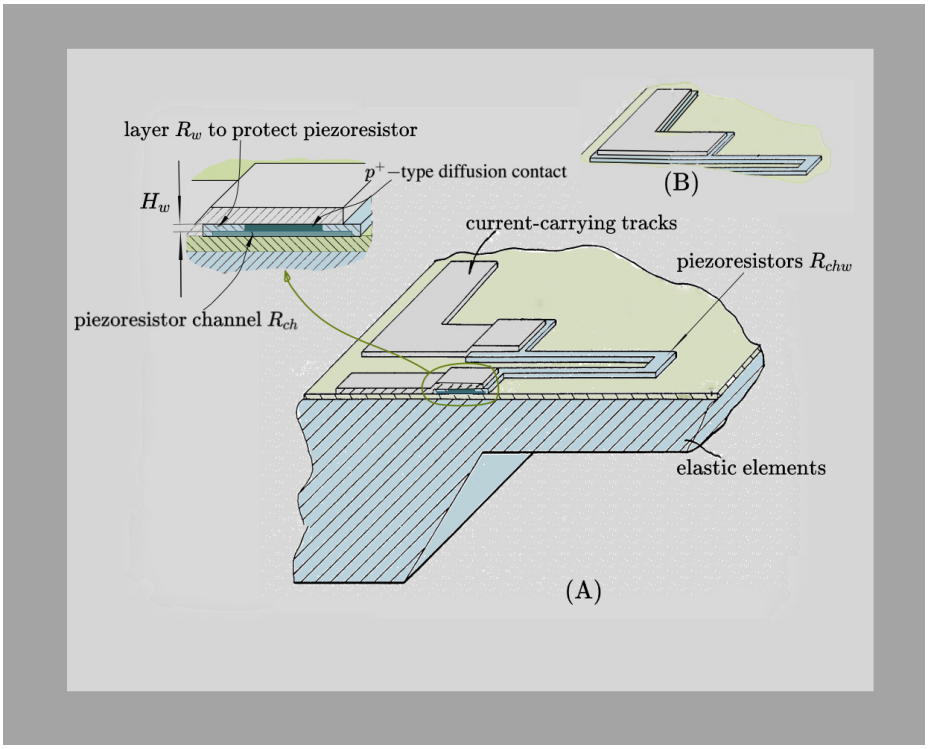

Figure 4: Structure of a high-temperature mechanical IPT manufactured by the SOI method

$$\alpha_r^{chw} = \frac{1}{R_{chw}} \cdot \frac{dR_{chw}}{dT} = \frac{R_s \cdot \alpha_r^w \cdot H_w + \rho_w \alpha_r^{ch} \cdot \frac{L_w}{L_{ch}}}{R_s \cdot H_w + \rho_w \cdot \frac{L_w}{L_{ch}}}; \tag{8}$$

$$\alpha_k^{chw} = \frac{1}{K_{chw}} \frac{dK_{chw}}{dT} = \frac{R_s \alpha_k^w H_w + \rho_w \alpha_k^{ch} \frac{L_w}{L_{ch}} \frac{K_{ch}}{K_w}}{R_s H_w + \rho_w \frac{L_w}{L_{ch}} \frac{K_{ch}}{K_w}} \tag{9}$$

$$\delta\alpha_k^{chw} = \frac{\alpha_k^w - \alpha_k^{ch}}{\alpha_k^{ch}} \tag{10}$$

where ρ_w is the resistivity of the material of the first wafer in $\Omega \cdot cm$; R_s is the surface resistance of the strain resistor channel in $\Omega/\square$; L_w and L_{ch} are the number of squares in the topology of the layer R_w to protect the piezoresistor and the piezoresistor channel R_{ch}, respectively, K_{ch} and K_w are the gauge factors of the piezoresistor channel and the material of the first wafer $Wafer_1$, respectively; $\delta\alpha_k^{chw}$ is the relative difference in the temperature coefficients of sensitivity between the material $Wafer_1$ and the piezoresistor channel.

Considering that the relative difference in the temperature coefficients of sensitivity between the $Wafer_1$ material and the piezoresistor channel R_{ch} depends primarily on the parameters of the layer R_w, when the values of $\frac{\delta\alpha_k^{chw}}{\alpha_k^{chw}}$ are less than 1%, the influence of the layer on the characteristics of the strain gauge channel can be neglected. In that case, the optimal value of the thickness H_w is determined by the following relationship:

$$H_w \leqslant \frac{\rho_w \cdot L_w \cdot K_{ch}}{R_s \cdot L_{ch} \cdot K_w \cdot \delta\alpha_k^{chw}} \cdot 10^{-2} \tag{11}$$

This relationship ensures that the influence of the R_w layer on the characteristics of the piezoresistor channel remains within an acceptable range.

From the provided considerations, we can draw the following conclusions:

- Insulating properties of p-n junctions at temperatures above $+100°C$ require further study. The current limit of $125°C$ is not the maximum operating temperature for monocrystalline silicon with insulating p-n junctions.
- Abrupt changes in the temperature dependences of the parameters occur when the junction isolation resistance decreases to a value of $R_{sh} \leqslant 200R_{in}$. This indicates the need to study the isolation of piezoresistive channels from the elastic element using a p-n junction layer depleted of charge carriers at temperatures higher than $+100°C$.
- The IPT-SOI design, which includes a monocrystalline silicon elastic element and piezoresistive channels electrically isolated from each other by a glass layer with a matched coefficient of thermal expansion, shows promise for the development of small-sized high-temperature sensors.

In summary, further research is needed to understand the insulating properties of p-n junctions at high temperatures, and the IPT-SOI design with a glass layer is a promising approach for developing high-temperature sensors.

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