Design and Analysis of Second and Third Order PLL at 450MHz

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ABSTRACT

Designing of an analog circuit satisfying the design constraints for desired application is a challenging job. Phase Lock Loop (PLL) is an important analog circuit used in various communication applications such as frequency synthesizer, radio, computer, clock generation, clock recovery, global positioning system, etc. Since all these applications are operating at different frequency, satisfying design constraints for PLL with respect to type of PLL operating frequency, Bandwidth, Settling time and other parameters is an critical and time consuming issue. In this paper, selection and design for Second order and third order PLL suggested using MATLAB, Simulink as a simulation tool. The simulated results for the design PLL at 450 MHz indicates good accuracy when the behavior model is compared with the mathematical model. Finally the performance of PLL is tested and calculated for parameters like lock time, lock range, Bandwidth.

KEYWORDS

PLL, Charge Pump PLL, Baseband PLL, VCO, Simulink, CAD, EDA tool.

1. INTRODUCTION

Phase locked loop is an excellent research topic as it covers many disciplines of electrical engineering such as Communication Theory, Control Theory, Signal Analysis, Noise Characterization, Design with transistors and op-Amps, Digital Circuit design and non-linear circuit analysis. The first PLL ICs came in existence around 1965 was built using purely analog devices. Recent advances in integrated circuit design techniques have led to an increased use of the PLL as it has become more economical and reliable. Now a whole PLL circuit can be integrated as a part of a larger circuit on a single Chip i.e SoC [1] [13]. MATLAB simulink [15] is effective tool to get prior idea about PLL parameters to fulfill requirements before actual chip design.

Phase-locked loops [17] are known to have plenty of applications, from low-frequency ones, e.g., motor controller [18] and synchronous power converters [19], to RF applications, e.g., frequency synthesizers [2][20]. For low-speed applications, phase-locked loop (PLL) systems can be implemented in DSP [19], [21]. On the other hand, for high-speed applications, PLL systems are realized in analog way [18], [20] and in digital way [3]. The accuracy of the required frequencies is very important in these designs as the performance is based on this parameter [1] [13] [4].

As the name suggests, the phase locked loop operates by trying to lock to the phase of a very accurate input signal through the use of its negative feedback path. A basic form of a PLL consists of three fundamental functional blocks namely Phase Detector (PD), Loop Filter (LF), Voltage Controlled Oscillator (VCO). The block diagram of PLL is shown in the figure 1. The different types of PLL can be broadly categorized as Analog PLL, Digital PLL and Hybrid PLL.

Figure 1. The block diagram of PLL

The presence of two nonlinear devices as phase-detector and VCO, in closed loop makes PLL, a nonlinear device. Therefore in this work, the performance of PLL designed for 450 MHz frequency is tested against VCO sensitivity, free running frequency, amplitude and phase of VCO, Loop filter transfer function.

The remainder of the paper is organized as follows. In Section 2, the basic of Linearized model of PLL and structure of third order PLL is explained. The equation for lock time (T_L), Bandwidth (BW) and lock range ($\Delta\omega_L$) is listed. In section 3, the frame for PLL design using Matlab/Simulink is explained. In section 4, the obtained results were compared with theoretical calculation.

2. LINEARIZED PHASE DOMAIN MODEL FOR PLL

The generalized loop response for the higher ordered PLL can be written as equation 1 [1], [2], [14]

$$\frac{\theta_o}{\theta_i} = \frac{K_p K_v F(s)}{s + K_p K_v F(s)} \dots\dots\dots (1)$$

Where,

θ_o = the output phase in radians

θ_i = the input phase in radians

K_p = the phase detector gain in volts per radian

K_v = the VCO gain in radians per volt-second

$F(s)$ = the loop filter transfer function (dimensionless)

The loop characteristics can be controlled by changing different types of loop filters then the order of PLL is $n+1$ where n order of the loop filter.

The simplest filter is a one-pole RC circuit. The loop transfer function in this case is given an equation 2.

$$F(s) = \frac{1}{1+sRC} \dots\dots\dots (2)$$

The loop response for 2nd order PLL can be found out using equation (2), (3).

$$\frac{\theta_o}{\theta_i} = \frac{\frac{K_p K_v}{RC}}{s^2 + \frac{s}{RC} + \frac{K_p K_v}{RC}} \dots\dots\dots (3)$$

Comparing the equation (3) with standard transfer function equation of second order filter we get,

$$\xi = \frac{1}{2\sqrt{K_p K_v RC}} \dots\dots\dots (4)$$

$$\omega_n = \sqrt{\frac{K_p K_v}{RC}} \dots\dots\dots (5)$$

Where,

RC = Time constant in sec.

ξ = damping ratio

ω_n = natural frequency

For sinusoidal phase detector K_p is $\frac{1}{2}$ of peak to peak voltage of PD output [4].

Using equation (3), (4), (5) we get,

$$\text{Lock time, } T_L = 2\pi/\omega_n \dots\dots\dots(6)$$

$$\text{Lock range, } \Delta\omega_L = \pi\xi\omega_n \dots\dots\dots(7)$$

$$\text{Bandwidth, } BW = \omega_n \left[1 - 2\xi^2 + (2 - 4\xi^2 + 4\xi^4)^{1/2} \right]^{1/2} \dots\dots(8)$$

Using these mathematical model formulae, the corresponding values for lock time, Lock range, Bandwidth is calculated for different types of PLL, Baseband PLL, Charged Pump PLL [2]. While designing charged pump PLL the pump current I_p and selection of C(mostly in nF) are the

important design factor to be considered. Typically for most of the designs value of I_p is $100\mu A$ to 1 mA [2] [7] [4].

$$\omega_n = \sqrt{\frac{I_p K_{vco}}{2\pi C_p}} \dots\dots\dots(9)$$

$$\xi = R_p \sqrt{\frac{I_p C_p K_{vco}}{2\pi}} \dots\dots\dots(10)$$

As expected, if $R_p=0$, then $\xi =0$. With complex poles, the decay time constant is given by equation (11)

$$\frac{1}{\xi \omega_n} = \frac{4\pi}{R_p I_p K_{vco}} \dots\dots\dots(11)$$

As seen from the closed loop transfer function of second order PLL. [2] if we decrease the $I_p * K_{vco}$, the gain crossover frequency decreases (or shifts toward the origin), degrading the phase margin. But this compensated type PLL suffers from a drawback. Since the charge pump drives the series combination of R_p and C_p , each time a current is injected into the loop filter, the control voltage experiences a large jump. Even in the locked condition, mismatches between I_{UP} and I_{DOWN} and the charge pump injection and clock feed through of S1 and S2 introduce voltage jump in V_{CONT} as shown in figure 3.

Figure.2. Structure of third order charge pump PLL

Figure. 3.Addition of C2 to improve stability

Design and analysis of third order PLL is important as higher order design are concerns with system stability designed for wide applications. Transfer function for second order filter for charge pump PLL is given by equation (12) . The structure of third order charge pump PLL and System model of charge pump PLL block diagram shown in figure 2,figure 4 respectively.

Transfer function of loop filter is given by equation (12)

$$\{Rp+1/C_pS\} // 1/C_2S \quad \dots\dots\dots (12)$$

The open loop and closed loop transfer function is given by equations (12), (13).

$$G_0(s) = \frac{\frac{I_p K_{vco}}{2\pi} (sRC_1 + 1)}{S^3 RC_1 C_2 + S^2 (C_1 + c_2)} \quad \dots\dots\dots (13)$$

$$G_c(s) = \frac{\frac{sI_p K_{vco} R}{2\pi} + \frac{I_p K_{vco}}{2\pi C_1}}{s^3 mRC_1 + \frac{sI_p K_{vco} R}{2\pi} + \frac{I_p K_{vco}}{2\pi C_1}} \quad \dots\dots\dots (14)$$

Where, I_p is the current of charge pump,

K_{vco} is the VCO gain constant

$m = \frac{C_2}{C_1}$ is the capacitance ratio.

Usually, C_2 is much smaller than C_1 ($m \ll 1$). Comparing equation (13) with equation (14) will get ξ , ω_n and m .

$$G_c(s) = \frac{2\xi\omega_n s + \omega^2}{m \frac{2\xi}{\omega_n} s^3 + (m+1)s^2 + \omega_n^2} \dots\dots\dots (15)$$

Figure 4. System model of charge pump PLL block diagram

3. FRAME WORK FOR PLL DESIGN

The set up arrangement done for PLL(Charge Pump PLL)is parameter measurement is shown in the figure 5.

3.1. Setup for PLL Simulation in Simulink

The input provided in set up is the order coefficient of Loop filter. For e.g., using the transfer function of Loop filter incorporated in automated program written in Matlab which guides to find the input to find the proper range of input applied to the set up assembly to get desired output. Similarly for other input parameters Like, VCO gain in Hz/volts and quiescent frequency were found out.

For analysis of third order PLL setup used is almost same as second order PLL, Input for assemble are Transfer Function of loop filter, Kvco, quiescent frequency of VCO.

Figure 5. Setup for measurement of PLL parameters in Simulink

3.2 Measurement of PLL parameters

The simulation is done in Simulink/Matlab 2009b on Intel processor core 2 Duo processor@ 2.93 GHz with 1.96GBRAM .The simulated results for filter output ,phase detector output and VCO outputs can seen in real time using scope in Simulink. The obtained VCO output filter output, Phase detector output for Charge pump PLL is shown in figure 7, figure 8 and figure 9 respectively. Similarly filter output (control signal),PD output and reference signal & VCO output shown in figure 10,11,12 respectively. These obtained data at least 5000 samples per result were stored in workspace. The peak value i. e A_1 and next peak value A_2 are found out from these samples using program written in Matlab [9], [10]. Using these retrieved values ξ and ω_n was found out using the formulae figure 6 [4].The automated program files guides to find calculated and observed value for given RC time constant.

Figure 6. Measurement of PLL

$$\xi = \frac{\ln(A_1/A_2)}{\sqrt{\pi^2 + [\ln(A_1/A_2)]^2}} \quad \dots\dots\dots(11)$$

$$\omega_n = \frac{2\pi}{T\sqrt{1-\xi^2}} \quad \dots\dots\dots (12)$$

Where,

A_1 =First maximum peak amplitude

A_2 = First minimum peak amplitude

Figure 7. Charge pump PLL filter output

Figure 8. Charge pump PLL Phase detector output

Figure 9. Charge pump PLL VCO output and input signal

Figure 7,8,9 shows Charge pump PLL filter output, Charge pump PLL Phase detector output and Charge pump PLL VCO output and input signal respectively these results are obtained by design and simulation of second order charge pump PLL, shows once the reference signal is tracked then phase detector outputs with minimum phase difference between input and output signal.

Figure 10. Third order Charge pump PLL filter output

Figure 11. Third order Charge pump PLL Phase detector output

Figure 10, 11, 12 shows Third order Charge pump PLL filter output, Phase detector output and VCO output and input signal with $\Delta\theta = 90$ respectively. It can be observed that when $\Delta\theta = 90$, and the reference signal is track PD output is zero. Figure 13 shows the step response of third order system for different damping factor. It can be observed that, as the damping factor of the system increases the settling time decreases.

Figure 12. Third order Charge pump PLL VCO output and input signal

Analysis of third order PLL using Bode plot of open loop and closed loop transfer function are shown in figure 14, figure 15 respectively, from the open loop bode plot critical phase margin is obtained and stability of system obtained by closed loop bode plot. Previous work involved design of PLL for specific phase margin but this work gives design and analysis of PLL for critical phase margin and how it affects behavior of PLL in terms of its parameters by changing damping factor shown in table 2.

Figure 13. Step response for different values of ξ of Charge pump PLL

Figure 14. Open loop Bode plot of third order CPPLL

Figure 15. Closed loop Bode plot of third order CPPLL

4. RESULT AND DISSCUSSION

For the different type of PLL, the comparative study of obtained results of PLL for parameter such as setting time (sec to msec), Bandwidth(Hz to MHz), Lock range(Hz-KHz) is shown in figure 16-24

Figure 16. Baseband PLL TYPE II for lock time

Figure 17. Baseband PLL TYPE II for Bandwidth

From figure16,17,18 ,It can be found out that Baseband PLL can be used for narrow BW applications such as GPS its around (0-10Hz) since the drawback is as Kvco increases setting time increases therefore selection RC time constant is acritical issue. and its lock range is small in range of few Hz.

Figure 18. Baseband PLL TYPE II for lock range

Figure 19. Linearized Baseband PLL TYPE II for lock time

Figure 20. Linearized Baseband PLL TYPE II for Bandwidth

Figure 21.Linearized Baseband PLL TYPE II for lockrange

Figure 19,20,20 shows performance of linearized baseband PLL.and from the graph 21,It was found that,for Linearized PLL K_{VCO} increases its lock range decreases drastically. The linearized model and the nonlinearized model differ in that the linearized model uses the approximation $\sin(\Delta\theta(t)) \cong \Delta\theta(t)$ to simplify the computations. This approximation is close when $\Delta\theta(t)$ is near zero. Thus, instead of using the input signal and the VCO output signal directly, the linearized PLL model uses only their phases.

Figure 22.Charge pump PLL TYPE II for lock time

From table 2 it can seen that with this approach, we get faster settling time for critical phase margin. For this novel method of design and analysis of charge pump PLL considering parameters such as settling time, overshoot, capacitor ratio(m) and loop gain are obtained better

results in terms of faster settling time ,wide BW as compare to previous work where settling time in μsec and bandwidth in KHz.

Figure 23.Charge pump PLL TYPE II for Bandwidth

Figure 24.Charge pump PLL TYPE II for lock range

From the graph 22-24,It was observed that ,for Charge pump PLL we get wider Bandwidth [9],[11],[12],faster settling time and lage lock range [13].The comparative result table for baseband, Lineaized baseband and chgre pump PLL is listed in table 1.

Table 1. Comparative result table for all types of PLL

PLL TYPE	Kvco in Hz/volts	Lock time		Lock Range		Bandwidth	
		Cal	Obs	Cal	Obs	Cal	obs
Baseband PLL	6.36 KHz/volts	0.75 sec	0.9 sec	0.75 Hz	0.65 Hz	12.5Hz	10.8Hz
	12.7 k Hz/volts	0.54sec	0.60 sec	0.93 93Hz	0.9394Hz	17.96Hz	16.24 Hz
	18.5KHz/volts	0.45sec	0.52 sec	1.33 Hz	1.145Hz	21.66Hz	18.74 Hz
Charge pump PLL	100 Mhz/volts	1.13 μ sec	1.5 μ sec	2.83 MHz	2.19 MHz	8.6 MHz	6.28 MHz
	250 Mhz/volts	70.4 μ sec	90.5 μ sec	2.89 MHz	2.78 MHz	138 MHz	152 MHz
	400 Mhz/volts	56.1 μ sec	79.3 μ sec	3.17 MHz	2.9 MHz	173 MHz	152 MHz
Linearized baseband PLL	10 Khz/volts	4.7 msec	5.2 msec	671.2Hz	601.98Hz	2.0397 KHz	1.8293 KHz
	30 Khz/volts	2.7 msec	2.4 msec	405.2Hz	464.97Hz	3.5922 KHz	4.119 KHz
	70 Khz/volts	1.5 msec	1.6 msec	186.0Hz	182.0765 Hz	6.3493 KHz	6.213 KHz

Table 2.Simulation results for 0.707 and 0.9

Parameter	$\xi=0.707$	$\xi=0.9$
Settling time	125.7nsec	98.76nsec
Overshoot%	1.18%	0.0000347%
m	0.000083	0.00001
Loop gain	4.575Mhz	7.9056Ghz

5. CONCLUSION

Design and Analysis of PLL parameters using Mathematical model and the behavior model of PLL is tested with MATLAB simulink tool. The effect on parameters of second order and third

order PLL at 450Mhz is discussed in this work. Simulation results show that ξ and ω_n affect the behavior of different PLL types. From the observed results, it is found out that, Linearized PLL is not used widely in communication applications due to constraint of smaller lock range for higher value of K_{VCO} . The use Baseband PLL is restricted to for narrow BW applications such as GPS systems in mobile communication whereas, Charge pump PLL can be widely used for many communication application due to its advantage as it provides wider Bandwidth, less setting & wider lock range.

Design and simulation of third order PLL by propose novel method is more efficient to provide stability of system using Matlab/ Simulink model and this novel method shows very good precision in designed parameters for wider communication applications.

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