Basic Logic Gate Realization using Quantum Dot Cellular Automata based Reversible Universal Gate

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ABSTRACT

Quantum-dot Cellular Automata is a new technology for development of logic circuits based on nanotechnology, and it is an one of the alternative for designing high performance computing over existing CMOS technology. The Research on reversible circuits is going on both VLSI and QCA based design due to low power consumption. In this paper we are presenting basic logic gate design using Reversible universal gate and also presenting the effectiveness of Reversible Universal Gate(RUG) by comparing it with other reversible gates.

Keywords

Reversible Universal Gate, Quantum Cell, Majority Voter, Inverter, Quantum Dot Cellular Automata.

1. INTRODUCTION

Due to miniaturization of transistors, the fundamental building block of digital circuits in VLSI technology such as CMOS, the performance of computer chips has shown outstanding development in the last decades. CMOS technology represents binary information by switching the electric current [1] [2] [3] [4]. However, this paradigm has serious drawbacks as device sizes are reduced. The interconnection of devices and signals is one of these problems. Another problem is with regard to the quantization of charge, which becomes significant as transistors become smaller. Finally, current switching results in huge energy dissipation. Recent studies show that the spatial limits of conventional electronics will be reached in the next few years and, as a consequence, this continuing development of VLSI based design is threatened; new approach is required in the circuit design. Quantum-Dot Cellular Automata (QCA) is one of the best alternatives from of the several alternatives based on nanotechnology to the CMOS-VLSI technologies [3].

One of the most pressing hurdles in the development of innovative computation paradigms and systems is energy dissipation [5] [6]. A possible solution is reversible computing. QCA is a promising emerging Nanotechnology that relies on novel design concepts. The basic logic devices for QCA are the majority voter (MV) and inverter (INV) [1]. QCA cells and some simple devices have already been successfully developed [7], [8], and [9]. A four-phase clocking scheme for QCA also known as Landauer clocking has been proposed in [10]. QCA has very low power consumption. The universal gate structures such as AOI (and-or-inverter) [11] have been proposed to achieve the cost effective digital design. However, these gates realize the irreversible logic and, therefore, can't be the right choice for energy efficient design.

Landauer [6] proved that for irreversible logic computations, each bit of information loss generates $k_B T \ln 2$ joules of heat energy as the energy required for a binary transition E_{bit} is given by the Shannon-von Neumann- Landauer (SNL) expression [6]

$$E_{bit} \geq E_{SNL} = k_B T \ln 2 = 0.017 eV, (1)$$

Where k_B is the Boltzmann constant, $T=300K$. This is the minimum energy to process a bit. However, the reversible computation allows computing beyond the SNL limit. Bennett [13] showed that zero power dissipation in logic circuits is possible only if a circuit is composed of reversible logic gates.

The reversible logic conserves energy using a charge recovery process in CMOS. On the other hand, the QCA circuit is a clocked information preserving system [14]. The energy dissipation of a QCA circuit can be significantly lower than $k_B T \ln 2$. This energy conservation is extra feature in favor of the QCA based circuit design. However QCA is more error prone to circuit designation [11].

The above scenario leads to another approach to design new gate structure based on QCA that will behave in reversible manner and also realizes the all basic logic functions. QCA based reversible circuit design satisfies the requirement for energy saving and at the same time ensure the defect tolerance. The reversible universal logic gate (RUG) has already proposed [12] that reduce the number of logic gates and garbage outputs in a digital design around it as compared to other existed reversible gates. Reversible Universal gate (RUG) is area saving implementation of complex logic simultaneously ensuring energy loss close to zero. So in this paper we are presenting realization of all basic logic gates using RUG.

2. REVERSIBLE GATE

A logic gate L is reversible if, for any output Y, there is a unique input X such that

$$L(X) = Y$$

If a gate L is reversible, there is an inverse gate L' which maps Y to X for which

$$L'(Y) = X.$$

From common logic gates, NOT gate is reversible, as can be seen from its truth table below.

TABLE 1: TRUTH TABLE FOR NOT GATE

INPUT	OUTPUT
0	1
1	0

The original motivation was that reversible gates dissipate less heat (or, in principle, no heat). In a normal gate, input states are lost, since less information is present in the output than was present at the input. This loss of information loses energy to the surrounding area as heat, because of thermodynamic entropy. Another way to understand this is that charges on a circuit are grounded and thus flow away, taking a small charge of energy with them when they change state. A reversible gate only moves the states around, and since no information is lost, so energy is conserved. Any reversible gate must have the same number of input and output bits. Many reversible gate exists namely Fredkin, Toffoli, QCA1, QCA2 RUG, PERES, TR, in which RUG is Universal Gate and use's much less number of QCA cells.

3. REVERSIBLE UNIVERSAL GATE (RUG)

Reversible Universal Gate has a 3-bit input as A, B, and C and 3-bit output as $AB+BC+CA$, $AB+A'C'$ and $B'C+BC'$. The First output is majority function, second output is Universal function and third output is XOR function. Shown in figure 1.

Figure 1: Block Diagram of RUG Gate

RUG logic design is consist of seven majority gates (MV) and four inverter, as shown in figure 1, retains in the simple clocking scheme. For the wire A, B, C it is in different clock zone because to main signal strength. Similarly all MV's also kept in corresponding clock zones.

RUG gate is universal; this means that for any Boolean function $f(x_1, x_2, x_3, \dots, x_m)$, there is a circuit consisting of RUG gates which takes $x_1, x_2, x_3, \dots, x_m$ and some extra bits set to 0 or 1 and outputs $x_1, x_2, x_3, \dots, x_m$, $f(x_1, x_2, x_3, \dots, x_m)$, and some extra bits. Essentially, this means that RUG gate can be used to build systems that will perform any desired Boolean computation in a reversible manner. So in this paper we are presenting, how to realize basic logic gates using RUG.

The $F2=AB+A'C'$ in the RUG gate is called Universal Function and which can be used to any logic with a given number of variables with minimum number of wire crossings [15]. So from [15], presence of universal function RUG based QCA circuits are very much cost-effective in terms of number of logic gate, wire crossing, cells count as compared to the designs based on existing reversible gate. This is the concept of a special form of reversible logic with universal functionality.

The implementation and effectiveness of RUG has been reported[12] and RUG is very cost effective reversible circuit design as compared to other existing gates based on less number of gates and garbage outputs. So RUG is very efficient for circuit designing while taking energy saving into consideration.

4. REALIZING BASIC LOGIC GATES USING RUG

The RUG gate takes three input bit A, B, C and produces three bit F1, F2, F3 as output as shown in figure:1; using various input combination on the RUG ; we can form basic logic gates as output. We are presenting how to realize basic logic gates using RUG

4.1 AND, NOT, XOR Gate Realization

The logic AND, NOT and XOR can be formed by setting 0, A and B as input in respective position in RUG gate as shown in figure 2.

Figure 2: Logic AND, NOT and XOR Gate

4.2 OR Gate Realization

The logic OR can be realized by setting 1, A and B as input in respective position in RUG gate as shown in figure 3.

Figure: 3. Logic OR Gate

4.3 NAND , NOR Gate Realization

The logic NOR and NAND gate can be realized by setting A', B', and 1 as input in respective position in RUG gate as shown in figure 4.

Figure 4: Logic NAND and NOR Gate

5. EFFECTIVENESS OF RUG

A comparative study on the performance of conventional reversible gates and the RUG in implementing standard function is also reported in table II. The performance in terms of average number of gates required in implementing all thirteen 3-variable standard functions is shown in Fig.5. It

points to the fact that the realization of logic circuits around RUG can result in better cost effective design than that of with other conventional reversible gates. Moreover, the reversible gates such as Feynman, toffoli etc. can't provide efficient realization of all thirteen standard functions.

TABLE II
DIFFERENT REVERSIBLE GATES IN REALIZING 13 STANDARD FUNCTIONS

13 standard functions	CQCA	FREDKIN	PERES	QCA1	TOFFOLI	TR	RUG
01. $F=AB'C$	2	2	2	2	3	2	3
02. $F=AB$	1	1	1	1	1	3	1
03. $F=A'BC+A'B'C'$	6	3	4	3	4	3	2
04. $F=A'BC+AB'C'$	4	4	3	6	-	4	3
05. $F=A'B+BC'$	3	5	5	2	4	4	3
06. $F=AB'+A'BC$	3	3	8	6	-	5	3
07. $F=A'BC+ABC'+A'B'C'$	7	5	5	6	-	7	3
08. $F=A$	1	1	1	1	1	1	1
09. $F=AB+BC+CA$	1	8	11	1	-	6	1
10. $F=A'B+B'C$	3	1	4	3	4	3	3
11. $F=A'B+BC+AB'C'$	6	4	2	6	2	2	3
12. $F=AB+A'B'$	3	2	3	3	2	2	1
13. $F=ABC'+A'B'C'+AB'C+A'BC$	9	11	4	7	2	3	3
Average Number of gates	3.7692	3.8462	4.0769	3.6154	2.5556	3.4615	2.3077

The figure 5. Bellow present graph in implementation of thirteen standard functions and can be easily seen that the RUG takes less number of gates as compared to other reversible gates.

Figure.5: Number of gates taken to implement 13 standard functions by different reversible gates(y coordinate) vs. 13 standard functions. (X coordinate)

The design capability of RUG is further evaluated in implementing adder operations and subtractor. The cost of a design is estimated in terms of number of reversible gates (Gate) and the number of garbage outputs (garbage) in

implementing of adder/subtractor. The comparative results are noted in Table III. The performance analysis considering the average number of gates and garbage outputs required for all those realization is represented in Fig.6.

Table III: Implementation of adder and subtractor by different reversible gates with gate count

Gates	Criteria	Half adder	Full adder	Half subs tractor	Full subs tractor	Average Value
Tinfoil	#Gates	2	4	3	4	3.25
	#Garbage's	3	7	5	8	5.75
NG[17]	#Gates	1	4	2	6	3.25
	#Garbage's	1	7	3	10	5.25
TR[19]	#Gates	2	6	1	2	2.75
	#Garbage's	4	11	1	2	4.5
QCA1[16]	#Gates	2	3	3	4	3
	#Garbage's	2	4	4	8	4.5
FREDKIN	#Gates	3	6	4	6	4.75
	#Garbage's	5	9	6	10	7.5
PERES	#Gates	1	2	3	6	3
	#Garbage's	1	2	5	9	4.25
RUG	#Gates	1	2	2	3	2
	#Garbage's	1	3	3	5	3

The figure 6. Bellow present graph while implementing adder and subtractor and it can be easily seen that the RUG takes less number of gates as compared to other reversible gates.

Figure: 6. Number of gates and garbage's taken (y-coordinate) vs. TOFFOLI, NG, TR, QCA, FREDKIN, PERES and RUG Gates (x-coordinate) in implementing adder and subtractor

Now it can be easily seen from Figure: 5 and Figure: 6 that the RUG implements all 13 standard function and adder/ subtractor in less number of gates and garbage. So RUG is very efficient for circuit designing while taking energy saving into consideration.

6. CONCLUSION

RUG is a 3X3 input output reversible logic gate having majority function and universal function and XOR function as outputs; like any other reversible gates RUG do not erase information and ultimately it leads high performance computing. In this paper we have shown how to realize basic logic gates using RUG and also presented effectiveness of RUG gate by comparing it with other existing reversible gate and I found it realizes all standard functions as well as symmetric function with better cost-effective result in terms of number of logic gate, wire crossings, cells count.

7. REFERENCES

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