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IMPLEMENTATION OF FPGA BASED DA-PID CONTROLLER FOR TEMPERATURE SYSTEM

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Abstract - In this paper, modular design of embedded feedback controllers using the Field Programmable Gate Array (FPGA) technology is presented. To this end, a novel Distributed Arithmetic (DA)-based Proportional Integral Derivative (PID) controller algorithm is implemented and integrated into a digital feedback control system. The DA-based PID controller savings 80% hardware utilization to the multiplier-based scheme. It also offers good closed-loop performance while using less resource, resulting in cost reduction, high speed, and low power consumption, which is desirable in embedded control applications. The complete digital control system is built using commercial FPGAs to control a simple temperature loop.

I. INTRODUCTION

The Proportional Integral Derivative (PID) controller is one of the most common types of feedback controllers used in dynamic systems. This controller has been widely used in many different areas such as aerospace, process control, manufacturing, robotics, automation. Implementation of PID controllers has gone through several stages of evolution, from the early mechanical and pneumatic designs to the microprocessor based systems. Recently, Field Programmable Gate Arrays (FPGA) have become an alternative solution for the realization of digital control systems, previously dominated by the general-purpose microprocessor systems. The FPGA-based controllers offer advantages such as high speed, complex functionality, and low power consumption.

II. DIGITAL TEMPERATURE CONTROL

Fig.1 block diagram for digital temperature control

PID CONTROLLER

Fig.2 block diagram for PID controller

The PID controller involves three separate parameters; the proportional, the integral and derivative values. The proportional value determines the reaction to the current error. The integral value determines the reaction based on the sum of recent errors. The derivative value determines the reaction based on the rate at which the error has been changing. The weighted sum of these three actions is used to adjust the process via a control element such as the position of a control valve or the power supply of a heating element.

PULSE-WIDTH MODULATION

Fig.3 PWM Generation

PWM is a very efficient way of providing intermediate amounts of electrical power between fully on and fully off. A simple power switch with a typical power source provides full power only, when

switched on. PWM is a comparatively recent technique, made practical by modern electronic power switches. The term duty cycle describes the proportion of on time to the regular interval or period of time; a low duty cycle corresponds to low power, because the power is off for most of the time. Duty cycle is expressed in percent, 100% being fully ON. PWM works well with digital controls, which, because of their on/off nature, can easily set the needed duty cycle.

VOLTAGE COMPARATOR

An operational amplifier has a well balanced difference input and a very high gain. The parallel in the characteristics allows the op-amps to serve as comparators in some functions. A standard op-amp operating in open loop configuration (without negative feedback) can be used as a comparator. When the non-inverting input (V_+) is at a higher voltage than the inverting input (V_-), the high gain of the op-amp causes it to output the most positive voltage it can. When the non-inverting input (V_+) drops below the inverting input (V_-), the op-amp outputs the most negative voltage it can. Since the output voltage is limited by the supply voltage, for an op-amp that uses a balanced, split supply, (powered by $\pm V_S$) this action can be written: Where $\text{sign}(x)$ is the sign function. Generally, the positive and negative supplies V_S will not match absolute value.

FPGA

The FPGA is an integrated circuit that contains many (64 to of 10,000) identical logic cells that can be viewed as standard components. Each logic cell can independently take on any one of a limited set of personalities. Based on the principle of functional Completeness FPGA: Functionally complete elements (Logic Blocks) placed in an interconnect framework. Interconnection framework comprises of wire segments and switches.

LM35

The LM35 series are precision integrated-circuit temperature sensors, whose output voltage is linearly proportional to the Celsius (Centigrade) temperature. The LM35 does not require any external calibration or trimming to provide typical accuracies of $\pm 1/4^\circ\text{C}$ at room temperature and $\pm 3/4^\circ\text{C}$ over a full 55 to $+150^\circ\text{C}$ temperature range. Low cost is assured by trimming and calibration at the wafer level. The LM35 is rated to operate over a 55 to $+150^\circ\text{C}$ temperature range, while the LM35C is rated for a 40° to $+110^\circ\text{C}$ range (-10° with improved accuracy). The LM35 series is available packaged in hermetic TO-46 transistor packages, while the LM35C, LM35CA, and LM35D are also available in the plastic TO-92 transistor package.

DELAY LINE A/D CONVERTER

Fig.4 Block diagram for delay line ADC

Static and dynamic output voltage regulation capabilities depend on the characteristics of the A/D converter. Conventional high-speed, high-resolution A/D converters consume power and chip area, and require precision analog components. Also, in the switching power supply, the sensed analog voltage V_{sense} comes from the output of a switching power converter.

This signal usually has significant switching noise, which can be a problem for many conventional A/D converters such as the basic flash configuration. Taking into account the specific requirements discussed in Section II, we introduced a novel delay-line A/D configuration shown in Fig. 5. The delay-line A/D converter is based on the principle that the propagation delay of a logic gate in a standard CMOS process increases if the gate supply voltage is reduced.

PID CONTROLLER IMPLEMENTATION USING FPGA

The FPGA implementation of the PID controller, a major effort is placed on the hardware optimization of the controller. In this regard, an area-efficient DA-based algorithm for the PID controller is proposed in this section. An area efficient controller means that it can fit in a smaller FPGA chip, resulting in cost reduction of the controller hardware.

An improved PID control algorithm

$$U(s) = K(bU_c(s) - Y(s) + \frac{1}{sTi}(u_c(s) - Y(s)) - \frac{sTd}{1 + sTd/N}Y(s)) \quad (1)$$

Where,

K, b, Ti, Td, and N are controller parameters,
U(s), Uc(s), and Y (s) denote the Laplace
transforms of u, uc, and y,

Denoting the sampling period as T, and using
backward differences to discretize the derivative term
and forward differences for the integral term can be
written as

$$u(k) = P(k) + I(k) + D(k) \quad (2)$$

Where k denotes the k-th sampling instant.

$$P(k) = K(bu_c(k) - y(k))$$

$$I(k) = I(k-1) + \frac{K}{T_i}(u_c(k-1) - y(k-1))$$

$$D(k) = \frac{T_d}{T_d + NT}D(k-1) - \frac{kT_d N}{T_d + NT} \quad (3)$$

$$(y(k) - y(k-1))$$

in which y(k) is the feedback signal at the current
instant k, y(k-1) is the feedback signal at the
previous instant k-1, uc(k) is the command signal at
the current instant, uc(k-1) is the command signal at
the previous instant, I(k-1) is the integral term at the
previous instant, D(k-1) is the derivative term at the
previous instant, K, b, Ti, Td, N are controller
parameters, and T is the sampling period.

DISTRIBUTED-ARITHMETIC (DA)

Distributed Arithmetic (DA) is a bit-serial
computation algorithm that performs multiplication
using a Look-up Table (LUT)-based scheme.
Consider a sum of product calculation written as

$$Y = \sum_{k=0}^{N-1} A_k x_k \quad (4)$$

where Ak's are constant coefficients, xk's are
input data of size N, and Y is the output.
Representing xk in a bit-wise format and assuming
that it is a 2's complement fractional number, we
have

$$x_k = -x_{k,0} + \sum_{j=1}^{M-1} x_{k,j} 2^{-j} \quad (5)$$

where xk,j is the j-th bit of xk, xk,0 is the sign bit,
and M is the word size. Substituting (5)
into (4), we have

$$Y = \sum_{k=0}^{N-1} A_k (-x_{k,0} + \sum_{j=1}^{M-1} x_{k,j} 2^{-j}) \quad (6)$$

$$= - \sum_{k=0}^{N-1} A_k x_{k,0} + \sum_{j=1}^{M-1} (\sum_{k=0}^{N-1} A_k x_{k,j}) 2^{-j} \quad (7)$$

$$Z_j = \sum_{k=0}^{N-1} A_k x_{k,j} \quad (j \neq 0) \quad (8)$$

$$Z_o = - \sum_{k=0}^{N-1} Z_j 2^{-j} \quad (9)$$

the output Y can then be expressed as follows

$$Y = \sum_{j=0}^{M-1} Z_j 2^{-j} \quad (10)$$

DA-BASED PID CONTROLLER

Assuming that uc(k), uc(k-1), y(k), y(k-1), and
D(k-1) are m-bit fixed-point numbers and [j]
represents the j-th bit of each number, we have

$$p(k) = \sum_{j=0}^{m-1} Kb * u_c(k)[j] - K * y(k)[j] \quad (11a)$$

$$y(k-1)[j] - y(k-1)[j] * 2^j$$

$$I(k) = I(k-1) + \sum_{j=0}^{m-1} \frac{KT}{T_i} (u_c(k-1)[j] - y(k-1)[j]) * 2^j \quad (11b)$$

$$D(k) = \sum_{j=0}^{m-1} (\frac{T_d}{T_d + NT} D(k-1)[j] - \frac{KT_d}{T_d + NT} (y(k)[j] - y(k-1)[j])) * 2^j \quad (11c)$$

The contents of LUTP is shown in Table 1,
with other LUTs taking a similar form. Using the four
LUTs and the corresponding shift-add accumulators
(ACCs), the P(k), I(k), and D(k) terms can be
obtained in m clock cycles. The main advantage of
the DA expression given by (11a), (11b), and (11c)
lies in its capability to compute the PID function
utilizing the LUT-rich FPGA.

Table-1 contents of the LUTP .

Uc(k)[j]	y(k)[j]	LUTP
0	0	0
0	1	-K
1	0	Kb
1	1	Kb - K

Based on equations (11a)-(11c), the direct DA
implementation of the PID controller consists of four
delay blocks, four LUTs, four ACCs, and four adders.

The delay blocks 1 and 2 are used to obtain uc(k-1)
and y(k-1), while the delay blocks 3 and 4 are
used to generate the terms I(k-1) and D(k-1),
respectively. Four LUTs and four ACCs are used to
provide the terms P(k), I0(k), D1(k), and
D2(k), respectively. The ACC consists of a shift
register and an adder/subtractor. Finally, one adder
computes the sum of I(k-1) and I0(k), resulting in

$I(k)$, one adder calculates the sum of $D1(k)$ and $D2(k)$, resulting in $D(k)$, and two adders calculate the sum of $P(k)$, $I(k)$, and $D(k)$, resulting in $u(k)$. The throughput (speed) of this PID implementation is $(m+1)$ clock cycles, i.e., m clock cycles to generate the result, and one more clock cycle to update the $u(k-1)$, $y(k-1)$, $I(k-1)$, and $D(k-1)$ terms. For the multiplier-based controller the throughput is one clock cycle. The latency is also $(m+1)$ clock cycles, whereas for the multiplier-based method it is one clock cycle. However, in terms of complexity, the DA-based scheme requires 4 LUTs, 4 ACCs, 4 delay blocks, and 4 adders, whereas the multiplier-based method requires 5 multipliers, 4 delay blocks, and 7 adders which is less area efficient than the DA-based scheme.

Fig.5 Architecture of DA-based PID controller.

To design a PID feedback controller for a temperature control system the FPGA-based temperature control system is comprised of the following components:

- (1) A tube with a fan, a light bulb, and a thermistor,
- (2) An I/O panel that includes a Digilent DIO2 board with an on-board CPLD, push-button keys with an LCD display, and a PS2 keyboard which is connected to the DIO2 board,
- (3) An ADC chip mounted on a separate circuit board, and
- (4) A Digilent D2E FPGA development board consisting a Xilinx Spartan-2E FPGA based temperature control system can be used for the process.

Fig.6 Components of the FPGA-based digital temperature control system

The thermistor in series with a resistor is used for temperature measurement inside the tube. The voltage V_t across R_t is used to calculate the temperature which is sampled by the ADC to be used in the control law.

Two PWM generators are implemented to control the DC motor and the lamp. The motor and lamp are turned either on or off depending on the PID controller output u . If u is a negative number, the PWM generator for the fan will generate a PWM waveform with appropriate duty cycle, while the PWM generator for the lamp will generate an off pulse.

If u is positive, the opposite will be true. In our implementation, u is a 34-bit fixed-point two's complement number. It is converted to a sign and magnitude representation and then scaled accordingly in order to generate the correct PWM output. Both PWM generators run at a clock frequency of 50MHz with a PWM period of 20ms.

The ADC used in this system is a Maxim MAX189 12-bit ADC with an internal reference voltage of 4.096V. The ADC interface polls the ADC every 20ms to receive the sampled data. The received 12-bit ADC data is converted into a 16-bit fixed-point format in order to represent the feedback signal y . The 16-bit fixed-point representation contains 4 bits for the integer portion and 12 bits for the fraction portion.

A PS2 keyboard, which is connected to the I/O board, is used for user input. An LCD on the I/O board displays the user's requests entered from the keyboard. The user interface decodes the user's requests and sends appropriate commands to other modules in the system.

Both multiplier-based and DA-based PID controllers are implemented. Each PID controller is integrated with the rest of the system. Considering that general-purpose microprocessors can only accommodate fixed bit-width data representation, FPGA offers an attractive feature of customizable bit-widths [4]. For both controllers, the inputs, u_c and y , are both 16-bit fixed-point two's complement numbers with 4 bits for the integer portion and 12 bits for the fraction portion. Due to the bit-serial nature of

the DA-based PID controller, parallel-in-serial-out (PISO) shift registers are used to serialize the inputs.

Fig.7 block diagram of the FPGA-based temperature control system

The LUTs of the DA-based PID controller are implemented using the existing 4-input LUTs inside the FPGA slices. The choice of word length in fixed-point arithmetic is crucial in maintaining system stability. Even though a longer word length will reduce quantization effects, it will result in an increase in hardware resources; however, shorter word lengths will affect the controller precision, causing an increase in control error, or destabilization of the system. Therefore, a compromise has to be made between the amount of hardware resources required and the controller precision desired. In this paper, the word length for the fractional part of the bit-width is 12 which was experimentally found to be sufficient for the application being studied. However, the performance of the controller in face of discretization may be further studied using analysis or simulation tools such as the DSP

Builder, a development tool that interfaces between the FPGA development software and the MathWorks MATLAB/Simulink tools.

Fig.8 Experimental setup

IV. CONCLUSIONS

In this paper, an FPGA-based digital feedback control system using a novel DA-based PID Controller is presented. Based on the LUT scheme, the proposed PID controller reduces 14% the cost of the FPGA design. Also, due to the flexibility of the LUT in the FPGA, this FPGA-based PID controller can be easily extended to incorporate other algorithms such as Anti-windup protection or adaptive schemes. This design approach would specifically be suitable for the next generation of FPGA chips, in which A/D and D/A converters are built inside the chip. In such a case, the proposed structure would be more efficient in terms of Hardware resources and control performance compared with the standard micro-controller IP cores. The complete system was designed using a modular approach and integrated and downloaded into Xilinx XC9572XL. The system was tested by simulations and Experiments, demonstrating good closed-loop stability and performance.

REFERENCES

- [1] L. Samet, N. Masmoudi, M. W. Kharat, and L. Kamoun, "A digital PID Controller for Real-time and Multi-loop Control: A Comparative Study," IEEE Int. Conf. on Electronics, Circuits and Systems, Vol. 1, pp. 291-296, Sept. 1998.
- [2] F. Krach, B. Braselton, J. Carletta and R. Veillette, "FPGA-Based Implementation of Digital Control for a Magnetic Bearing," American Control Conference, Vol.2, pp. 1080-1085, June 2003.
- [3] F. Ricci, H. Le-Huy, "An FPGA-Based Rapid Prototyping Platform for Variable-Speed Drives", IEEE Industrial Electronics Society Annual Conference, vol.2, pp. 1156-1161, Nov. 2002.
- [4] L. Charaabi, E. Monmasson, I. Slama-Belkhouja, "Presentation of an Efficient Design Methodology for FPGA Implementation of Control Systems: Application to the Design of an Antiwindup PI Controller," IEEE Industrial Electronics Society Annual Conference, Vol. 3, pp. 1942 - 1947, Nov. 2002.
- [5] Altera Flex10K Embedded Programmable Logic Family Data Sheet, Altera Corp., 2003; <http://altera.com>.
- [6] Xilinx Inc., Spartan IIE Data sheet: <http://www.xilinx.com>.
- [7] Moallem M., "A Laboratory Testbed for Embedded Computer Control", IEEE Transactions on Education, Vol. 47, No. 3, pp. 340-347, 2004.