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ENHANCEMENT OF SWITCHING TIME AND POWER OF CMOS DEVICES

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Abstract- Mosfets have been used widely in electronic devices as the basic building blocks of processors, controllers, and Switches etc. But perhaps the simplest and the most common Among such a myriad of applications is the cmos inverter with It's powerful switching characteristics. We make an attempt to Present ways to further improve the switching characteristics and The transition region of the cmos inverter without any Significant trade-off losses. This indirectly leads to a mos which Operates at a lower power as will be shown. The tradeoffs, which Do not degrade the device significantly, have been presented too. The latest techniques for achieving them have been discussed as Well.

I. INTRODUCTION

Recent advancements in CMOS* technology have permitted use of the devices in practically every nook and corner of the world. These devices have become so ubiquitous that it is hard to find oneself in an environment bereft of them. As the basic building block of any electronics they have virtually conquered the world. Shrinking at an enormous rate, billions of them are now fit into a size as small as a Business card. So any tiny bit of improvement in a facet of the device will have a tremendous effect on the mankind due to their sheer numbers.

In this paper we examine methods, some mature, yet some others under active development, to improve the switching delay, power consumption in switching, switching speed. An added advantage of one of the method we use will also help in reducing crosstalk noise (which is due to the mutual capacitance between the metal lines). Although NMOS device is regarded as a device capable of delivering faster switching than CMOS, the CMOS has been considered noting it's considerably less power requirements due to lower currents over the spectrum of application of voltage input (V_{in}) to the transistor. We attempt to show that the solution to most of the above problems is the reduction of the capacitance, the parasitic capacitance in particular. In this context we particularly refer to an important work done at the University of California, Berkeley [3] which elucidates the use of Vacuum spacer, and Corner spacer technologies which utilize filling the gaps between the gate and the contacts with dielectric materials to reduce the effective parasitic capacitance.

We further present how to reduce the transition region in the V_{out} vs. V_{in} characteristics curve of the CMOS inverter device potentially leading to faster switching by a much lesser voltage change which enables us to use circuits which can operate at substantially lower power levels.

II. VACCU SPACER TECHNOLOGY

We are very well aware that capacitance of any system is based primarily on three things

- 1) Area (A)
- 2) Length(d)
- 3) Dielectric(k)

Clearly for a given un-scalable device of fixed dimensions the former two cannot be changed but we can achieve reduced capacitance by decreasing the latter. This can obviously be achieved by using materials of lower dielectric. An ingenious way would be to "trap" vacuum between a material of suitably low dielectric constant to give a „virtual“ feeling of lower effective dielectric and hence reducing the corresponding capacitance as graphically portrayed below in Fig 0.

Figure-0 A vacuum technology based MOS device. Red area is the gate. Blue region implies the substrate. The white region surrounding the gate shows the implementation of the vacuum technology.

The vacuum exists inside the interlayer dielectric (surrounding the gate) which leads to lower capacitance. Parallel methods exist which utilize Silicon Nitride (etc) in “Nitride Spacer” CMOS technologies which among a myriad of benefits has probably the most important feature that it would be relatively easier to fabricate than a vacuum based technology. There is, however, a tradeoff involved, i.e. in the low power standby mode of the device, degradation of the „on“ current has to be taken into account because of using a low “k” dielectric material.

Results obtained at the reference quoted earlier show that delay(or effectively speed) in the linear contact inverter improves by as much as 10 % while simultaneously reducing the afore-mentioned inverter switching energy by 25% using the vacuum spacer technology at a fixed V_{dd} of .76V. Another observation of interest was that 43% power consumption reduction was obtained while using a linear contact inverter with vacuum spacer technology as opposed to a circular-contact inverter with oxide spacer (both were running at the same speed). This represents nearly a double rise in the improvement factor. Factual comparison of the vacuum spacer and the oxide spacer has been shown below diagrammatically based on results obtained in experiments conducted at the reference mentioned before.

The mixed-mode simulation of inverter delay. The delay of the vacuum spacer is decreased by 30% as compared to the oxide spacer.

Figure-1 Comparisons of delays in Vacuum and Oxide spacer technologies.

III. CORNER SPACER TECHNOLOGY

This is another approach which successfully reduces the capacitance, called as the “Corner Technology”. This consists of small high-k spacers present only at the gate-S/D (Source/ Drain) edges where they are needed to improve the „on“ and „off“ currents. The larger low-k spacer reduces the gate capacitance for improved speed and energy consumption. Suggested materials for high-k spacer could be Silicon Nitride or HfO₂ and low-k material may be silicon oxide or

even vacuum. The figure below shows the corner technology implementation (mono-layer).

Figure 2- Corner technology based device showing mono layer technology (inner layer)

The need for this technology came into focus when the long channel transistor started getting more and more obsolete. As the gate length began to scale down to proportions achieved never before, the need for Gate spacers to make Lightly Doped Drain (LDD) was felt. The gate spacer material suggested for the same is usually SiO₂. An improvement that can be suggested for this technology is to use „dual spacer technology“ which reduces the cell junction leakage current and uses lesser silicon in the cell array. Dual spacer technology involves two layers of material i.e. a thin SiO₂ spacer located beside the gate pattern (also referred to as the inner layer) and a thick Si₃N₄ spacer outside the inner spacer of SiO₂. A tradeoff, however, is that it increases the gate capacitance because of a relatively higher-k dielectric constant of the silicon nitride which leads to a loss in speed of the circuit.

IV. COMPARISON AMONG VARIOUS TECHNOLOGIES

1) For Devices In Low-Power Standby Mode. Low-Standby Devices

Spacer	Improvement in Corner spacer (speed)	Improvement in Corner spacer (power)
Silicon oxide	19% ↑	7% ↑
Silicon nitride	19% ↑	7% ↑
Hafnium oxide	11% ↑	25% ↑
Vacuum	33% ↑	2% ↓

2) For High Performance Devices. High Performance Devices

Spacer	Improvement in Corner spacer (speed)	Improvement in Corner spacer (power)
Silicon oxide	10% ↑	12% ↑
Silicon nitride	20% ↑	24% ↑
Hafnium oxide	32% ↑	43% ↑
Vacuum	4% ↑	6% ↓

Clearly as can be seen both vacuum and corner technologies devices are vastly superior to others and among the two, corner has a higher speed (lesser delay) than the vacuum device but also consumes more power. so based on ones priority one may choose between the two.

V. USING THE CHANNEL REGION OF THE MOS

The channel of the MOS is the core driver of the MOS characteristics and here we make an attempt to exploit the channel properties, namely channel depth and doping to improve the transition region of the standard CMOS inverter.

In other words we aim to push the „slope“ of the saturation region of the MOS device to as high a value as possible here enabling to obtain efficient switching for relatively smaller signal swings around a smaller switching voltage thereby leading to tremendous power savings.

Schematic of a CMOS inverter as processed on a p-type silicon substrate.
NBTI effect is mainly felt on the right-hand side (p MOSFET)

Figure 3- A CMOS inverter utilizing wells(below)

Note about the above figure - Fig 3: The p-channel MOSFET relies on an n-type substrate. As commonly p-type wafers are used for processing, an additional n-type well implant is necessary. In this well, which is a deep region of n-type doping, the p-channel MOSFET is placed. As the p-substrate and the n-well junction is reverse biased, no significant current flows between these regions and the two transistors are isolated.

We aim to, for the CMOS transistor shown above, to reduce the “thickness” of the transition region as shown in the steady state degradation figure below

and reduce the voltage level of input voltage where switching occurs.

Figure-4 Voltage characteristics of the inverter.

Voltage transfer characteristics of the CMOS inverter without degradation. The transition from $V_{out} = V_{high}$ to $V_{out} = V_{low}$ is symmetric and

The voltage transfer characteristics of the unstressed inverter can be seen in the figure. The transition from the „on“ to the „off“ state is very well aligned around $V_{dd}/2$. The DC response for a standard CMOS circuits showing inverted characteristics is shown below and it has been suitably demonstrated above that the switching region can be decreased by incorporating the suggested changes.

The DC-DC response above has a transition region which can be suitably compressed by choosing a vacuum spacer or a oxide spacer depending on one's needs and requirements.

In the figure below we have the DC current plotted versus DC voltage bias and have obtained a peak at about 0.7 volts whose characteristics can also be suitably modified by implementing the spacer technologies discussed above. The vacuum spacer will reduce the parasitic capacitance of the CMOS circuit and will tend to make the peak slimmer.

Negative Bias Temperature (NBT) stress has its highest impact on the p-channel MOSFET during low input $V_{in} = V_{low}$. At this condition the transistor has a gate to substrate voltage of approximately $-V_{dd}$. When the circuit is additionally subject to thermal stress, then the threshold voltage of the p-channel transistor is degraded. As the n-channel device has a much lower susceptibility to this type of stress the circuit loses its symmetry. The switching point of the output potential moved to a lower input voltage. An interface trap density, which is already a severely damaged interface, reduces the switching point by more than 1V. Another method to achieve the same is to increase the doping concentration of the channel which will lead to a faster inversion.

VI. CONCLUSION

Decreasing the parasitic capacitance improves switching speed and power consumption in CMOS technologies. Depending on the type of device needed we may choose the appropriate spacer technology. For high performance device, i.e. device wherein high speeds are desired, we choose corner spacer structure technology. On the other hand, for a low standby power consumption device, i.e. a device where speeds take lesser priority than power consumption, we can choose the vacuum spacer structure technology. If, however, both are of importance, corner spacer structure with vacuum and silicon oxide is the best option. We have also shown, graphically in the later part of the paper, that improving the saturation region

of the voltage characteristics of the inverter gives us a device capable of running at a much lower power.

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