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B. Chitti Babu

National Institute of Technology, Rourkela-769 008 (INDIA), bcbabu@nitrkl.ac.in

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Grid Synchronization Algorithm For DG Systems Using DSRF PLL

B. Chitti Babu

Department of Electrical Engineering, National Institute of Technology, Rourkela-769 008 (INDIA)
E-mail: bcbabu@nitrkl.ac.in

Abstract - Distributed Generation (DG) System is a small scale electric power generation at or near the user's facility as opposed to the normal mode of centralized power generation. In order to ensure safe and reliable operation of power system based on DS, grid synchronization algorithm plays a very important role. This paper presents a novel Double Synchronous Reference Frame (DSRF) PLL (based on synthesis circuit) for grid connected inverter system under grid disturbances. Due to flexible in characteristics, DSRF PLL can accurately detect the phase irrespective of the grid conditions. Further, it demonstrates how the PLLs track the phase angle during some of the major abnormal grid conditions like voltage unbalance, line to ground fault and voltage sag etc.

I. INTRODUCTION

The use of fossil fuels for electric power generation has imposed several problems on the environment. This along with the day by day increasing demands of power lead to a demand of power generation using renewable energy sources, which mainly include solar power, wind power, small hydel power etc. [1]-[2].

The power generation systems based on renewable energy systems are distributed near the user's facility. These Distributed Generation (DG) Systems needs to be controlled properly in order to ensure sinusoidal current injection into the grid. However, they have a poor controllability due to their intermittent characteristics. [3]. The major issue associated with DG system is their synchronization with utility voltage vector [4]. Henceforth the study of grid synchronization algorithms is essential

Few of the earliest known synchronization algorithms include Zero Crossing Detectors (ZCDs). The performance of ZCDs is badly affected by power quality problems, especially in the case of weak grid. The use of Phase Locked Loops (PLLs) for grid synchronization has shown much better results as it has been discussed in [5]. The Linear PLL is mainly used to detect phase for single phase supply. For balanced three phase supply, Synchronous Reference Frame (SRF) PLL is used. But it is found that this PLL fails to detect the phase for unbalanced supply [6]. Hence Decoupled Double Synchronous Reference Frame (DDSRF) PLL was proposed to deal with unbalanced grid conditions like voltage unbalance [7]. DDSRF PLL can detect the

positive sequence phase angle in such conditions. Double Synchronous Reference PLL based on synthesis circuit was proposed in [6] which is more frequency adaptive and can be easily implemented. Other PLL techniques used for grid synchronization include Enhanced PLL (EPLL) which does not use Synchronous Reference Frame but rather synchronizes each phase of a 3 phase system independently [8]. Other method used for detection of positive sequence is the use Second Order Generalized Integrator (SOGI) [9-10]. The harmonic rejection capacity of this method is very high

This paper presents a novel Double Synchronous Reference Frame (DSRF) PLL (based on synthesis circuit) for grid connected inverter system under grid disturbances. Due to flexible in characteristics, DSRF PLL can accurately detect the phase irrespective of the grid conditions along with decoupling of positive and negative sequence components. Further, it demonstrates how the PLLs can track the phase angle during some of the major abnormal grid conditions like voltage unbalance, line to ground fault and voltage sag etc.

II. DUAL SYNCHRONOUS REFERENCE FRAME PLL

From [6] the Dual SRF PLL (DSRF PLL) is a combination of two conventional SRF-PLLs. These two frames are separated by a synthesis circuit. The voltage vector v is decomposed into positive and negative sequence vectors and these components are denoted by v_+ and v_- respectively as shown in Fig. 1. As shown in

Fig. 3, the α - and β -axis components both contain the information of the positive sequence and negative sequence which makes it difficult to detect the positive sequence component. The two PLLs work independently, rotating with positive direction and negative direction respectively and detect the positive sequence and negative sequence simultaneously.

Fig. 1 : Voltage Vector Decomposition (unbalanced voltage) (taken from [6])

Fig. 2 : Dual SRF PLL structure (taken from [6])

Fig.3 Synthesis Circuit used in DSRF PLL (taken from [6]).

The d -axis component from the Park's transformation is fed to the synthesis circuit. This signal is actually the voltage amplitude in steady state. The synthesis circuit consists of a Low Pass Filter (L.P.F.), two multipliers, and two orthogonal trigonometric functions as shown in Fig. 3. The main objective of the orthogonal functions is to create orthogonal and in-

phase signals with respect to the input signal multiplying them with the amplitude. These signals are used as decoupling signals as shown in the Fig. 2.

The two PLLs are required to detect the positive and negative sequence at the same time. The signals generated by the synthesis circuit are used as feedback for the unbalanced input signal. The input to the Park's transformation, and is the difference of actual and and the generated signals from the other PLL. As the process goes on the input to the PLL cleans up and the distortion at the output is cancelled. The positive sequence is detected by the PLL with as the initial angular frequency and the negative sequence is detected by the one with as the initial angular frequency.

The behaviour of DSRF PLL is explained by the equations given below [6].

At initial state $\theta_+ = 0$, $\theta_- = 0$. Hence the output of the synthesis circuit is zero and decoupling circuit has no effect. Each PLL contains both positive and negative sequence information. In rotating reference frame, rotating with positive direction, the Park's transformation output is

$$\begin{bmatrix} v_{d+} \\ v_{q+} \end{bmatrix} = U_+ \begin{bmatrix} \cos(\theta_+ - \hat{\theta}_+) \\ \sin(\theta_+ - \hat{\theta}_+) \end{bmatrix} + U_- \begin{bmatrix} \cos(\theta_- - \hat{\theta}_-) \\ \sin(\theta_- - \hat{\theta}_-) \end{bmatrix} \quad (1)$$

at initial state, which is the approximate center angular frequency of positive sequence component. Then (5) becomes

$$(2)$$

As it can be seen, there are some ripples in the d -axis component which is attenuated using a low pass filter. This makes the PLL more stable. The LPF is defined as

$$LPF(s) = \frac{\omega_c}{s + \omega_c} \quad (3)$$

where ω_c is the cut off frequency of the LPF.

The PLL behaviour is analysed by using state variable model. The state equations can be derived as (taking 2 state variables, and as the state vectors):-

$$\begin{cases} \dot{x}_1 = \omega_c(U_+ - x_1 + (U_- - x_2) \cos(\theta_+ - \theta_-)) \\ \dot{x}_2 = \omega_c(U_- - x_2 + (U_+ - x_1) \cos(\theta_+ - \theta_-)) \end{cases} \quad (2)$$

where

At steady state and . This implies that the d -axis component will converge to input

voltage vector amplitude after sometime, and the decoupling of signals by the synthesis circuit begins. So each PLL input will be

$$\begin{cases} v_{\alpha+} = v_{\alpha} - U_{-} \cos \theta_{-} = U_{+} \cos \theta_{+} \\ v_{\beta+} = v_{\beta} - U_{-} \sin \theta_{-} = U_{+} \sin \theta_{+} \end{cases} \quad (5)$$

and

$$\begin{cases} v_{\alpha-} = v_{\alpha} - U_{+} \cos \theta_{+} = U_{-} \cos \theta_{-} \\ v_{\beta-} = v_{\beta} - U_{+} \sin \theta_{+} = U_{-} \sin \theta_{-} \end{cases} \quad (6)$$

III. RESULTS AND DISCUSSIONS

A. Dynamic Response of DSRF PLL Under unbalanced Grid voltages

The dynamic responses obtained from simulation for DSRF PLL under unbalance input voltage are shown in Fig. 4. The PI tuning used for these results are $K_p=67.5$ and $K_i=100$.

Fig.4 Dynamic response of DSRF PLL under unbalanced grid conditions (a) grid voltage waveforms (b) d-plus component of grid voltage (c) d-minus component of grid voltage (d) q-plus component of grid voltage (e) q-minus component of grid voltage (f) detected angular frequency of positive sequence component (g) detected angular frequency of negative sequence component (h) detected phase angle of positive sequence component (i) detected phase angle of negative sequence component

Figure 4(a) shows a 3 phase signal which is balanced up to time $t=0.4$ sec and then voltage amplitude of 2 of the phases reduces to 0.5 from their initial value of 1.5. With this kind of input the dynamic responses are observed.

The positive and negative sequence components are separately observed in case of DSRF PLL. As shown in Fig. 4(b) d axis voltage of positive sequence component is almost constant both during balanced and unbalanced period and negligible sinusoidal variations are observed other than the transient period (from $t=0.4$ to 0.5 sec). Similarly as shown in Fig. 4(c) the d axis component of negative sequence component is also almost constant having negligible variations. As shown in Fig. 4(d) the q axis voltage of the positive sequence component maintains a constant value both in balanced and unbalanced conditions. The transients are observed when there is sudden change in input voltage (at $t=0.4$ sec). The transient vanishes to give a nearly constant value (nearly at zero) of q axis voltage of positive sequence component. A similar nature is observed for q axis voltage for negative sequence component as can be seen in Fig. 4(e).

The angular frequencies of positive and negative sequence components are both similar to their respective q axis voltages and hence a nearly constant angular frequency is observed for positive and negative sequence components (Fig. 4(f) and Fig. 4(g) respectively). For these constant angular frequencies we observe perfectly triangular phase angle detection for positive sequence (Fig. 4(h)) and negative sequence (Fig. 4(i)). The detected phase angle varies linearly every cycle from 0 to 2π for positive sequence and 0 to -2π for negative sequence.

B. DSRF PLL Under line to ground fault

The results obtained from simulation for DSRF PLL under line to ground fault are shown in Fig. 5. The PI tuning used for these results are $K_p=67.5$ and $K_i=100$.

Fig. 5. Simulation results obtained for DSRF PLL under line to ground fault (a) grid voltage waveforms (b) d-plus component of grid voltage (c) d-minus component of grid voltage (d) q-plus component of grid voltage (e) q-minus component of grid voltage (f) detected angular frequency of positive sequence component (g) detected angular frequency of negative sequence component (h) detected phase angle of positive sequence component (i) detected phase angle of positive sequence component

Figure 5(a) shows the input to the system when line to ground fault occurs. The system was initially in balanced condition (having amplitude 1.5V). Line to ground fault occurs at time, $t = 0.4$ sec. At this instant the phase voltage of 2 of the phases reduces and remains at an amplitude of 1.3V. The system regains its balanced state at time, $t = 0.5$ sec. The d axis voltage of positive sequence component shown in Fig. 5(b) is constant at the amplitude of the signals during balanced input. During line to ground fault the d axis voltage reduces and some oscillations with very small amplitude are observed. The d axis voltage for negative sequence component (Fig. 5(c)) also maintains its constant value other than very small transients that occur at time $t = 0.4$ sec and 0.5 sec. The q axis voltages for positive sequence (Fig. 5(d)) and negative sequence (Fig. 5(e)) maintains their near zero value at all instants, with some oscillations at the instants when switching of voltages occur. The angular frequencies of positive sequence and negative sequence components maintain their constant value at 100π and -100π (Fig. 5(f) and Fig. 5(g) respectively). Therefore the detected phase angle is perfectly triangular for both positive (Fig. 5(h)) and negative sequence (Fig. 5(i)).

IV. CONCLUSIONS

The paper presents performance of Dual Synchronous Reference Frame PLL for phase detection under grid disturbances. The grid disturbances include, voltage unbalance, line to ground fault and voltage sag. From the above discussions, one can observe that, the proposed DSRF PLL can accurately detect the phase irrespective of grid condition. Moreover, the DSRF PLL can also decouple the positive and negative sequence components of grid voltages in order to ensure

sinusoidal current injection into the Grid. Further, the results clearly show that the DSRF PLL gives much better response to track the positive sequence component as compared to conventional SRF PLL which fails to track the phase angle whenever there is an unbalance in the grid. On the other hand DSRF PLL properly handles the abnormalities and the phase angle is perfectly detected in each case. The improvement in this study will be enhanced by implementing the proposed DSRF PLL in digital platform using FPGA in the future work.

REFERENCES

- [1] F. Blaabjerg, R. Teodorescu, M. Liserre, and A. V. Timbus, "Overview of Control and Grid Synchronization for Distributed Power Generation Systems," *Proc. of IEEE Trans. on Industrial Electronics*, vol. 53, no. 5, pp. 1398-1409, 2006.
- [2] R. Lawrence and S. Middlekauff, "The new guy on the block," *IEEE Ind. Appl. Mag.*, vol. 11, no. 1, pp. 54-59, Jan./Feb. 2005.
- [3] F. Blaabjerg, Z. Chen and S. Kjaer, "Power Electronics as Efficient Interface in Dispersed Power Generation Systems," *IEEE Trans. Power Electron.*, vol. 19, no. 5, pp. 1184-1194, Sep. 2004.
- [4] A. Timbus, R. Teodorescu, F. Blaabjerg and M. Liserre, "Synchronization Methods for Three Phase Distributed Power Generation Systems. An Overview and Evaluation," in *Proc. 2005 Power Electronics Specialists Conference, 2005. PESC '05. IEEE 36th*, pp. 2474-2481.
- [5] Francisco D. Freijedo, Jesus Doval-Gandoy, Oscar Lopez, Carlos Martinez-Penalver, Alejandro G. Yepes, Pablo Fernandez-Comesana, Andres Nogueiras, Jano Malvar, Nogueiras, Jorge Marcos and Alfonso Lago, "Grid-Synchronization Methods for Power Converters," *Proc. of IEEE 35th Industrial Electronics Society Annual Conference. IECON '09.* pp. 522 – 529, 2009.
- [6] FANG Xiong, WANG Yue, LI Ming, WANG Ke and LEI Wanjun, "A Novel PLL for Grid Synchronization of Power Electronic Converters in Unbalanced and Variable-Frequency Environment," *Proc. of IEEE International Symposium on Power Electronics for Distributed Generation Systems*: pp. 466-467, 2010.
- [7] P. Rodriguez, J. Pou, J. Bergas, J. I. Candela, R. P. Burgos and D. Boroyevich, "Decoupled Double Synchronous Reference Frame PLL for

- Power Converters Control,” *Power Electronics, IEEE Transactions on*, vol. 22, pp. 584-592, 2007.
- [8] M. Karimi-Ghartemani and M. R. Iravani, “A method for synchronization of power electronic converters in polluted and variable-frequency environments,” *Power Systems, IEEE Transactions on*, vol. 19, pp. 1263-1270, 2004.
- [9] P. Rodriguez, A. Luna, M. Ciobotaru, R. Teodorescu and F. Blaabjerg, “Advanced Grid Synchronization System for Power Converters under Unbalanced and Distorted Operating Conditions,” in *Proc. 2006 IEEE Industrial Electronics, IECON 2006 – 32nd Annual Conference on*, pp. 5173-5178.
- [10] P. Rodriguez, R. Teodorescu, I. Candela, A. V. Timbus, M. Liserre and F. Blaabjerg, “New Positive-sequence Voltage Detector for Grid Synchronization of Power Converters under Faulty Grid Conditions,” in *Proc. 2006 Power Electronics Specialists Conference, 2006. PESC '06. 37th IEEE*, pp. 1-7.