July 2014

SIMULATION AND ANALYSIS OF 3T AND 4T CNTFET DRAM DESIGN IN 32nm TECHNOLOGY

N. SOMORJIT SINGH

Muthayammal Engineering College, Rasipuram-637 408, Tamil Nadu, n.somorjitsingh@gmail.com

DR.M. MADHESWARAN

Depart.of ECE, Muthayammal Engineering College, Rasipuram-637 408,Tamil Nadu, dr_mmadheswaran@gmail.com

Follow this and additional works at: <https://www.interscience.in/ijess>

Part of the [Electrical and Electronics Commons](#)

Recommended Citation

SINGH, N. SOMORJIT and MADHESWARAN, DR.M. (2014) "SIMULATION AND ANALYSIS OF 3T AND 4T CNTFET DRAM DESIGN IN 32nm TECHNOLOGY," *International Journal of Electronics Signals and Systems*: Vol. 4 : Iss. 1 , Article 8.

DOI: 10.47893/IJESS.2014.1197

Available at: <https://www.interscience.in/ijess/vol4/iss1/8>

This Article is brought to you for free and open access by the Interscience Journals at Interscience Research Network. It has been accepted for inclusion in International Journal of Electronics Signals and Systems by an authorized editor of Interscience Research Network. For more information, please contact sritampatnaik@gmail.com.

SIMULATION AND ANALYSIS OF 3T AND 4T CNTFET DRAM DESIGN IN 32nm TECHNOLOGY

N.SOMORJIT SINGH¹, DR.M.MADHESWARAN²

¹M.E. VLSI Design, Muthayammal Engineering College, Rasipuram-637 408, Tamil Nadu

²M.E.,Ph.D., Professor/Depart.of ECE, Muthayammal Engineering College, Rasipuram-637 408,Tamil Nadu

Abstract- Carbon Nanotube Field Effect Transistors (CNTFETs) is a promising device alternative for future nanometers-scale technology. This paper presents 3TCNTFET & 4TCNTFET simulation and analysis of DRAM with metallic CNTFET using a CNTFET SPICE(HSPICE) model with 32ns technology have shown the DRAM cells in terms of leakage power, power dissipation, delay time, dynamic write and read power. Here, comparison between 4TDRAM and 3TDRAM memory cells is also shown which 3TDRAM has better performance in power dissipation and leakage power than 4TDRAM cell, but less delay in 4TDRAM.

Keywords- Carbon nanotube FET (CNTFET),Three-transistor(3T),Four-transistor(4T),dynamic random access memory(DRAM), metallic CNT.

I. INTRODUCTION

Semiconductor memory arrays capable of storing large quantities of digital information are essential to all digital system. The amount of memory required in a particular system depends on the type of application, but number of transistors required for storage function is larger than for logic operations and other application. For the past four decades, CMOS scaling has offering improved performance from one technology node to the next. However, as device scaling move beyond the 32-nm node, significant technology challenges will be faced. Currently, the two main challenges are the considerable increase of standby power dissipation and the increasing variability in the device characteristics which in turn affects circuit and system reliability [1]. The International Technology Roadmap for Semiconductors (ITRS) has identified Carbon-based nanotechnology is one among seven "Beyond CMOS" for accelerated development in future innovations [2].

Since the first CNTFET was reported in1998, great progress has been made during the past years in all the areas of CNTFET science and technology, including materials, devices, and circuits [3]. On the other hand, as the feature size of silicon semiconductor devices scales down to nano meter range, planar bulk CMOS design and fabrication encounter significant challenge. CNTFET among other new materials is promising due to the unique one-dimensional band-structure which reduces backscattering and makes near-ballistic operation. Exceptional electrical properties such as high speed, high-K compatibility, chemical stability, low SCEs have provided CNFETs with excellent characteristics which exceed those of the state of the art Si-based MOSFETs [4].The limits involve electron tunneling through short channels and thin insulator films, the

associated leakage currents, passive power dissipation, short channel effects, and variations in device structure and doping. These limits can be overcome to some extent and facilitate further scaling down of device dimensions by modifying the channel material in the traditional bulk MOSFET structure with a single carbon nanotube or an array of carbon nanotube [5]. The exceptional electrical properties of carbon nanotube arise from the unique electronic structure of graphene itself that can roll up and form a hollow cylinder [6]. From equation 1and 2, the circumference of such carbon nanotube can be expressed in terms of chiral vector: $\hat{C}_h = m\hat{a}_1 + n\hat{a}_2$ which connect two crystallographically equivalent sites of the two-dimensional graphene sheet. Here m and n are integers and $\hat{a}_1$ and $\hat{a}_2$ are the unit vectors of the hexagonal honeycomb lattice. Therefore, the structure of any integers (m ,n) that define its chiral vector.In terms of the integers (m ,n) , the nanotube diameter d_t and the chiral angle θ are given by:

$$d_t = \frac{\sqrt{3}a_{C-C}\sqrt{m^2 + mn + n^2}}{\pi} \quad (1)$$

$$\theta = \tan^{-1} \left(\frac{\sqrt{3}n}{2m + n} \right) \quad (2)$$

The differences in the chiral angle and the diameter cause the differences in the properties of the various carbon nanotubes. For examples, it can be shown that an (m ,n) carbon nanotube is metallic when $m = n$, has a small gap (i.e. semi-metallic) when $n - m = 3i$, where i is an integer, and is semiconducting when $n - m \neq 3i$ [7]. Metallic conduction occurs when one of these wave vectors passes through the k-point of graphene's 2D hexagonal Brillouin zone, where the valence and conduction bands are degenerate [8]. Dynamic random access memory (DRAMs) is very crucial to the performance of computer systems. They

are right in the middle of memory hierarchy consisting of cache (made of static random access memory), main memory, and hard drive (magnetic memory or solid state memory) [9]. The improvement of other system components' performance and speed, particularly for microprocessors, has outpaced the performance of DRAMs [10]. Thus, the DRAM has increasingly become a bottleneck for the performance of many computer systems. DRAMs however are continually used in many computing applications because of their ability to be densely packed.

Figure 1: Graphene atomic structure with a translational vector $\vec{T}$ and a chiral vector $\vec{C}_n$ of a CNT.

The current trend of miniaturization of devices and growing popularity of embedded systems, which employ DRAMs, increases the importance of DRAMs. The evolution of the DRAM has been an instrumental part to the advancement and performance of modern computer systems. DRAM chips are used in almost all types of computing systems because they are cheap, relatively fast, and possess high density storage [11]. This in essence serves the purpose of the memory hierarchy of computer systems which is making the "maximum possible and fast memory available to the users at a minimal possible cost." Static random access memory (SRAM) is another popular type of memory.

Figure 2: Schematic diagram for 4T DRAM cell.

It is faster than DRAM but more expensive and also has a lower memory density [12]. With the development and design of many memory intensive devices such as smart phones, media players, and other similar portable devices, the impact of DRAMs on electronic systems continues to grow. Therefore,

there is a large body of research on improving the performance of the DRAM and still maintain its cheap cost and high memory density.

II. 3T DRAM CELL OPERATION

The circuit diagram of a typical three-transistor dynamic RAM cell is shown in Fig. 3 without the column pull-up (pre-charge) transistors and the column read/write circuitry. Here, the binary information is stored in the form of charge in the parasitic node capacitance C1. The storage transistor M2 is turned on or off depending on the charge stored in C1, and the pass transistors M1 and M3 act as access switches for data read and write operations. The cell has two separate bit lines for "data read" and "data write," and two separate word lines to control the access transistors.

The operation of the three-transistor DRAM cell and its peripheral circuitry is based on a two-phase non-overlapping clock scheme. The pre-charge events are driven by 01, whereas the "read" and "write" events are driven by 02. Every "data read" and "data write" operation is preceded by a pre-charge cycle, which is initiated with the pre-charge signal PC going high. During the pre-charge cycle, the column pull-up transistors are activated, and the corresponding column capacitances C2 and C3 are charged up to logic-high level. With NCFET transistors and a power supply voltage of .9V, the voltage level of both columns after the pre-charge is approximately equal to .65 V.

Figure 3: Schematic diagram for 3T DRAM Cell.

All "data read" and "data write" operations are performed during the active 2 phase, i.e., when PC is low. Figure 4 & 5, depicts the typical voltage waveforms associated with the 3-T DRAM cell during a sequence of four consecutive operations: write "1," read "1," write "0," and read "0." The four pre-charge cycles are numbered 1, 3, 5, and 7, respectively. The transient currents charging up the two columns (Din and Dt) during a pre-charge cycle. The pre-charge cycle is effectively completed when both capacitance voltages reach their steady-state values. Note here that the two column capacitances C2 and C3 are at least one order of magnitude larger than the internal storage capacitance C.

For the write "1" operation, the inverse data input is at the logic-low level, because the data to be written onto the DRAM cell is logic "1." Consequently, the "data write" transistor M1 is turned off, and the voltage level on column Din remains high. Now, the "write select" signal WS is pulled high during the active phase of 02. As a result, the write access transistor M1 is turned on. With M1 conducting, the charge on C2 is now shared with C1 (Fig.3). Since the capacitance C2 is very large compared to C1, the storage node capacitance C1 attains approximately the same logic-high level as the column capacitance C2 at the end of the charge-sharing process [13].

After the write "1" operation is completed, the write access transistor M1 is turned off. With the storage capacitance C charged-up to a logic-high level, transistor M2 is now conducting. In order to read this stored "1," the "read select" signal RS must be pulled high during the active phase of 02, following a pre-charge cycle. As the read access transistor M3 turns on, M2 and M3 create a conducting path between the "data read" column capacitance C3 and the ground. The capacitance C3 discharges through M2 and M3, and the falling column voltage is interpreted by the "data read" circuitry as a stored logic "1." The active portion of the DRAM cell during the read "1" cycle is shown in Fig.3 Note that the 3-T DRAM cell may be read repeatedly in this fashion without disturbing the charge stored in C.

For the write "0" operation, the inverse data input is at the logic-high level, because the data to be written onto the DRAM cell is logic "0." Consequently, the data write transistor is turned on, and the voltage level on column Din is pulled to logic "0." Now, the "write select" signal WS is pulled high during the active phase of 02. As a result, the write access transistor M1 is turned on. The voltage level on C2, as well as that on the storage node C1, is pulled to logic "0" through M1 and the data write transistor, as shown in Fig. 4. Thus, at the end of the write "0" sequence, the storage capacitance C1 contains a very low charge, and the transistor M2 is turned off since its gate voltage is approximately equal to zero.

In order to read this stored "0," the "read select" signal RS must be pulled high during the active phase of 02, following a pre-charge cycle. The read access transistor M3 turns on, but since M2 is off, there is no conducting path between the column capacitance C3 and the ground (Fig.3). Consequently, C3 does not discharge, and the logic-high level on the column is interpreted by the data read circuitry as a stored "0" bit. The drain junction leakage current of the write access transistor M1 is the main reason for the gradual depletion of the stored charge on C1. In order to refresh the data stored in the DRAM cells before they are altered due to leakage, the data must be periodically read, inverted (since the data output level

reflects the inverse of the stored data), and then written back into the same cell location. This refresh operation is performed for all storage cells in the DRAM array every 2 to 4 ms. Note that all bits in one row can be refreshed at once, which significantly simplifies the procedure.

It can be seen that the three-transistor dynamic RAM cell examined here does not dissipate any static power for data storage, since there is no continuous current flow in the circuit [14]. Also, the use of periodic pre-charge cycles instead of static pull-up further reduces the dynamic power dissipation. The additional peripheral circuitry required for scheduling the non-overlapping control signals [15].

III. CNTFET DRAM PERFORMANCE

HSPICE simulations have been performed using a Berkeley 32-nm PTM HP model and CNTFETs parameter models by Stanford University's Nanoelectronics Group. HSPICE is the most accurate circuit simulation that is used in much semiconductor industry setting [16]-[18]. The nominal chirality of the CNTs is (19,0) and a pitch of 30nm, the length of doped CNT source/drain extension region (L_{sd}) = 32.0nm, Fermi level of the doped S/D tube (E_{fo}) = 0.6 eV the thickness of high-k top gate dielectric material (T_{ox}) = 4.0nm, Flatband voltage for n-CNTFET (V_{fbn}) = 0.0eV, the mean free path in intrinsic CNT (L_{ceff}) = 200.0nm, the mean free path in p+/n+ doped CNT = 15.0nm, the work function of Source/Drain metal contact = 4.6eV CNT work function = 4.5eV.

IV. SIMULATION RESULTS

We have simulated read and write operation of 3T and 4T NCNTFET DRAM cells. Their results are as shown below, Simulation of read and write operation of two transistor DRAM cell is successfully done. So we have included its simulation result. The simulations assume DRAM memory with 3T cells and 4T cells to evaluate performance with significant capacitive loading on the bit lines. The number of CNTs per transistor for 3T DRAM cell are T1 (5), T2 (5) both as precharge transistor, T3 (3), T5 (3) as pass transistor, T4 (3) as storage transistor and T6(3) as data input transistor. The number of CNTs per transistor for the 4T cell is T1(5),T2(5),T3(3),T4(3),T5(3),T6(3), T7(3) and T8(3). The number of CNTs per transistor is set to be optimizing DRAM cell performance and functionality. The operation for both 3T DRAM cells and 4T DRAM cells are same, in these paper explained 3T DRAM cells only and four different operations for both cells are included in last page after references. In "Read 1" operation, charge store in bit line bar capacitor has fully discharge through the M4 transistor called as store transistor due to the

store capacitance has able on the M4 transistor switch on state by act as supply voltage has shown in the above figure 5(last page,no.6).In the “Write 0” operation, the charge capacitor (c6) has initialized .9v, and the complement of input “data in” has supplied logic 1(.9v pulse) then the bit line capacitor (c3) has discharging completely with storage capacitor, has shown in above figure 6.For the “Read 0” operation, the storage capacitor has not been recharged, due to flow to the M7 transistor’s ground during “Write 0” operation. There is no gate supply voltage to M4, so M4 transistor is in open state; the charge present in bit line bar is not discharge, still in the capacitor itself.

The overall 3T DRAM memory cell operation has shown below graph with precharge pulse, word line pulse, inverter input, storage capacitive output result and read line.

Fig. 4: Write and Read waveform for 3TDRAM CNTFET.

We have simulated read and write operation of 4 transistor NCNTFET DRAM cell. Their powers results are as shown below, Simulation of read and write operation of two transistor DRAM cell is successfully done. In 4TDRAM write and read line are common and there is two storage capacitance c(3) and c(4), charge store in these two capacitor has been compliment to each other like when c(3) is store high(store charge) then c(4) will not store charge as via versa. Similarly, input data supply in M3 and M4 transistor are also complement that Vdatabar is supply in gate terminal of M3 and Vdata is supply in gate terminal of M4.

Fig. 5: Write and Read waveform for 4TDRAM NCNFET.

CNTFET transistors are very power-efficient because they dissipate nearly zero power while idle, Static dissipation due to subthreshold conduction through OFF transistors, tunneling current through gate oxide, and leakage through reverse-biased diode. Dynamic dissipation due to charging and discharging of load capacitances, supply voltage (Vdd). Leakage current is a growing problem as technology scales, recall leakage arise from subthreshold conduction, gate tunneling and reverse biasing. Sub threshold conduction is presently the most important because V_t is low and getting lower, but gate tunneling will become profoundly important too as oxide thickness dimensions. The threshold voltage V_t is defined as the value of V_{gs} below which I_{ds} become zero, subthreshold current continues to flow for $V_{gs} < V_t$ so measuring or even defining the threshold voltage becomes problematic, the threshold voltage varies with L, number of tubes, V_{ds} and V_{bs} .

Results for 3-transistotr CNTFET DRAM designed in the project Vdatain from time 0 to 150e-009:

TABLE 1: LEAKAGE POWER FOR 3TDRAM CELL.

Leakage	1	0
Write 0	31nw	12uw
Read 0	31nw	12uw
Write 1	31nw	12uw
Read 1	31nw	13uw

TABLE 2: AVERAGE POWER DISSIPATION 3TDRAM.

Dissipation	Value
Write 0	81nw
Read 0	81nw
Write 1	81nw
Read 1	85nw

TABLE 3: DELAY TIME FOR 3TDRAM CELL.

Delay	Value
Write 0	2.4ns
Read 0	2ns
Write 1	.9ns
Read 0	1ns

TABLE 4: DYNAMIC POWER FOR 3TDRAM CELL.

Power	Value
Write 0	81nw
Read 0	81nw
Write 1	81nw
Read 1	85nw

Results for 4-transistr CNTFET DRAM designed in the project Vdatain from time 0 to 150e-009:

TABLE 5: LEAKAGE POWER FOR 4TDRAM.

Leakage	1	0
Write 0	31nw	.3mw
Read 0	31nw	13uw
Write 1	31nw	13uw
Read 1	31nw	13uw

TABLE 6: AVERAGE POWER DISSIPATION FOR 4TDRAM CELL.

Dissipation	Value
Write 0	2uw
Read 0	86nw
Write 1	86nw
Read 1	86nw

TABLE 7: DELAY TIME FOR 4TDRAM CELL.

Delay	Value
Write 0	.9ns
Read 0	1.1ns
Write 1	.9ns
Read 1	.98ns

TABLE 8: DYNAMIC POWER FOR 4TDRAM.

Power	Value
Write 0	2uw
Read 0	86nw
Write 1	86nw
Read 1	86nw

V. CONCLUSION

Comparison the same operation has also take place in 3T NCNFET DRAM and 4T NCNFET DRAM, here we are plot the related figures. The threshold voltage (V_{th}) in 32-nm technology is less than 25% of V_{dd} supply voltages (.9v) which is much lower than CMOS DRAM. The power dissipation, leakages power is better performance in 3T DRAM CNTFET than 4T DRAM, but delay has comparatively less delay time in 4T DRAM.

There is some glitches are found in 4TDRAM in storage capacitance switching because of input rise/falls time is greater than zero, both transistors will be ON for a short of time while the input is between V_{th} of V (3), word line voltage and ($V_{DD} - V_{th}$) of V (4), input voltage that makes more dissipation power in "Write 0". Lastly, the entire transistor in my project is N type transistor use like NCNFET. HSPICE simulator tool has used to plot the related graphs and values.

ACKNOWLEDGMENT

The authors would like to thank many people for useful discussions: Dr. S. Dasgupta, Associate Professor ,Naushad and Manoj kumar, PhD scholar (IIT Roorkee) for their guide and technical support.

REFERENCES

- [1] Zhe Zhang,"Carbon nano tube SRAM design with Metallic CNT or Removed Metallic CNT Tolerant Approaches" IEEE Trans. on Nanotechnology, vol. 11, pp. 788-798, July 2012.
- [2] Balwant Raj, Anita Suman, and Gurmohan Singh, "Analysis of power dissipation in DRAM cells design for nanoscale memories," International journal of information technology and Knowledge Management, vol. 2, No. 2, pp. July/dec. 2009.
- [3] P. L. McEuen, M. S. Fuhrer, and Park Hongkun, "Single-walled carbon nanotubeelectronics," IEEE Trans. on Nanotechnology, Vol. 1, No.1, pp. 78-85,2002.
- [4] R. Saito, G. Dresselhaus, and M. Dresselhaus, "Physical Properties of Carbon Nanotubes," Imperial College Press, 1998.
- [5] R. Martel, T. Schmidt, H. R. Shea, T. Hertel, and P. Avouris, "Single- and multi-wall carbon nanotube field-effect transistors," Applied Physics Letters, Vol. 73, pp. 2447-2449, 1998.
- [6] Desmond C.Y.Chek, Michael L.P. Tan, Mohammad Taghi Ahmadi, and Razali Ismail, "Analytical modeling of high performance single-walled carbon nanotube field-effect-transistor",ELSEVIER Microelectronics Journal 41 (2010) pp. 579-584.
- [7] J.Deng and H.-S.P. Wong, "A compact SPICE model for carbon nanotube field effect transistors including non-idealities and its application," IEEE Trans. Electron Devices, vol. 54, no. 12 , pp. 3195 – 3205, Dec. 2007 .
- [8] Övünç Polat and Ali Manzak,"Evaluation of Low Power Carbon Nanotube Field Effect Transistor (CNTFET) Master-Slave Latches," in Proc.2012 ICICA,IPCSIT vol.32. 2008, pp.1543-1551.

- [9] Alan C.Seabaugh,"Low-voltage Tunnel transistors for Beyond CMOS logic"Proceedings of IEEE , vol. 98, pp. 2095-2110, Dec., 2010.
- [10] Jae-yoon Sim, " Circuit Design of DRAM for Mobile Generation," Journal of semiconductor technology and science, vol. 7, No.1, March,2007.
- [11] Mariya Lyubomirova Spasova, George Vasilev Angelov and Marin Hristov Hristov, "Simulation of 1T DRAM memory cell with Verilog-A Model of CNTFET in Cadence," Annual Journal of Electronics, 2012, ISSN 1314-0078.
- [12] Rajendra Prasad, B.K. Madhavi, and K.Lal Kishore, " Design of low Write-power consumption SRAM cell based on CNTFET at 32nm technology," International Journal of VLSI design & Communication Systems(VLSICS), Vol.2, No.4, Dec.2011.
- [13] Sung-Mo Kang, Yusuf Leblebici, "CMOS Digital Integrated Circuits Analysis and Design," 3rd Ed. New York: McGraw-Hill, 2003, ch. 10.
- [14] Albert Malvino, David J Bates, "Electronic Principles," seventh edition. New delhi: Tata McGraw Hill Education Private limited.2007.ch.7, 14.
- [15] Neil H.E. Weste, David Harris and Ayan Banerjee, "CMOS VLSI Design, a circuits and systems perspective," Third Edition. Dorling Kindersley(India) Pvt. Ltd.,2007
- [16] International Technology Roadmap for Semiconductors.(2010).[Online]. Available: <http://www.itrs.net/>.
- [17] Berkeley Predictive Technology Model. (2011). [Online]. Availability: <http://www.ead.asu.edu./ptm/>.
- CNTFET Models.(2011). [Online] .Availabile:[http:// nano.stanford.edu/ models](http://nano.stanford.edu/ models).

Write 1" operation of 3TDRAM

"Read 1" operation of 3TDRAM.

"Write 0" operations in 3TDRAM

"Read 0" operation in 3TDRAM

Figure 6: Waveform for 3tdram Operations
"Write 1" operation of 4TDRAM.

"Read 1" operation of 4TDRAM.

"Write 0" operations in 4TDRAM.

"Read 0" operation in 4TDRAM.

Figure 7: Waveform for 4tdram Operations