April 2013

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Recommended Citation

AMALA MINU, C K. (2013) "SIMULINK/MODELSIM CO-SIMULATION AND FPGA REALIZATION OF SPWM CONTROLLER FOR THREE PHASE MULTILEVEL INVERTER," *International Journal of Electronics Signals and Systems*: Vol. 2 : Iss. 4 , Article 6.

DOI: 10.47893/IJESS.2013.1117

Available at: <https://www.interscience.in/ijess/vol2/iss4/6>

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SIMULINK/MODELSIM CO-SIMULATION AND FPGA REALIZATION OF SPWM CONTROLLER FOR THREE PHASE MULTILEVEL INVERTER

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Abstract- In this project a design of application-based adaptable level three-phase diode clamped multilevel voltage source inverter is proposed. The inverter is designed in a fussy manner, that different levels of the inverter can be designed and simulated in a single circuit. Using select input he level switching of inverter is done. A Mat lab/Simulink model of the proposed design is modeled and simulated, with the gating signals generated using FPGA. A Phase opposition disposition sinusoidal PWM (PODSPWM) algorithm is used for generation of gating signals. The harmonic analysis of the output voltage waveform for each levels of inverter is done separately and using proposed model, verified the result. A comparison of total harmonic distortion of different levels of inverter is done. The total harmonic distortion is very low for higher level inverter. The FPGA implementation of gating signals for the proposed model is done using Xilinx Spartan 3 XCS400PQ208.

Keywords- Inverter, Multilevel inverter, Carrier Disposition Pulse Width Modulation, Total Harmonic Distortion.

I. INTRODUCTION

The term power quality has been used to describe the variation of the voltage, current and frequency on the power system. Most of the power system equipment has been able to operate successfully with relatively wide variation of these three parameters. However within the last five to ten years large amount equipment has been added to the power system which is not so tolerant of these variations. This has included a large amount of equipment which is controlled by power electronics devices, such as AC drives and switch mode power supplies. With the use of these power electronics devices non sinusoidal current/voltage are produced and it contains harmonics.

An inverter is commonly used in variable speed AC motor drives to produce a variable three phase AC output voltage from a constant DC voltage source, which has two voltage level(+Vdc ,-Vdc).The output waveform of the inverters should be sinusoidal for efficient operation. But the output of the conventional two level PWM inverters would be a square wave or quasi square wave. The square wave is rich in harmonic content. To minimize the output voltage distortion with improves fundamental voltage, the multilevel concept has been implemented. The multilevel inverters are suitable for high voltage and high power application due to their ability to synthesis waveforms with better harmonic spectrum. Multilevel pulse width modulation (PWM) inverters are gaining importance due to the fact that lower order harmonics in the output waveform can be eliminated without any increase in the higher order harmonics. Also as the number of voltage level reaches infinity, the output total harmonic distortion

(THD) approaches to zero. Pulse Width Modulation (PWM) has now become an integral part of almost all power electronics systems. It has been widely accepted as control technique in most of the electronic appliances. These techniques have been extensively researched during past few years. Their design implementation depends upon application type, power consumption, semiconductor devices and performance all determining the PWM method. One of the most important application of PWM lies in power electronics applications for controlling power converters like DC to AC converters , DC to DC converters, etc.PWM Inverters are one of those power converters which extensively use concept of PWM for its operation. Carrier PWM techniques require a carrier signal which is modulated with modulating signal to produce desired PWM signal.

In this project, dynamically partially reconfigurable pulse width modulation (DPRPWM) controller for three-phase voltage-source inverters (VSI) in a single Xilinx Spartan3 XCS400PQ208 field programmable gate array (FPGA) has designed. The DPRPWM controller is designed such that it switches between the popular PWM The PWM control is simulated and experimentally verified using a low-cost Xilinx Spartan FPGA. For the design and study of multilevel of inverter and various PWM technology, to reduce THD, an adaptable level three-phase diode clamped inverter has been designed using Simulink and various PWM signals has been generated using ModelSim 6.2c. In this adaptable level three-phase diode clamped inverter switch between different levels up to level 7 can be done as shown in the figure 1. The FPGA implementation of PWM signals for the

adaptable level inverter is done using SPARTAN3 XS3400PQ208 with Xilinx. The model is simulated for different levels of inverter. The harmonic analysis is done for each levels of the inverter. A comparison of total harmonic distortion was done for different levels of the inverter

Figure 1 Block Diagram of Proposed Design

II. MULTILEVEL INVERTER

Multilevel power conversion technology is a very rapidly growing area of power electronics with good potential for further development. The most attractive application of this technology is in the medium-to-high-voltage range, motor drives, power distribution, and power conditioning applications.

Figure 2: Multilevel inverter system

A. Diode Clamped Inverter

The most commonly used multilevel inverter topology is the diode clamped inverter. Here diodes are used as the clamping device to clamp the dc bus voltage so as to achieve steps in the output voltage. In general for a N level diode clamped inverter, for each leg 2 (N-1) switching devices, (N-1) * (N-2) clamping diodes and (N-1) dc link capacitors are required. When N is sufficiently high, the number of diodes and the number of switching devices will increase, makes complex circuit. The efficiency is high because all devices are switched at the fundamental frequency.

Figure 3 :Three phase three level NPC inverter

Table 1 Valid Switch states for Three phase three level NPC inverter

Switch State			
Sa1	Sa2	Sa1n	Sa2n
1	1	0	0
0	1	1	0
0	0	1	1

The figure 3 shows a three level NPC inverter and its switching conditions are shown in table I. The figure 4 shows a five level NPC inverter and its switching conditions are shown in table II.

Figure 4 :Three phase five level NPC inverter

Table II Valid Switch states for Three phase five level NPC inverter

Switch State							
Sa1	Sa2	Sa3	Sa4	Sa1n	Sa2n	Sa3n	Sa4n
1	1	1	1	0	0	0	0
0	1	1	1	1	0	0	0
0	0	1	1	1	1	0	0
0	0	0	1	1	1	1	0
0	0	0	0	1	1	1	1

The figure 5 shows a seven level NPC inverter and its switching conditions are shown in table III.

Figure 5 :Three phase seven level NPC inverter

Table III Valid Switch states for Three phase seven level NPC inverter

Switch State												Output Volt (Van)
Sa1	Sa2	Sa3	Sa4	Sa5	Sa6	Sa1n	Sa2n	Sa3n	Sa4n	Sa5n	Sa6n	
1	1	1	1	1	1	0	0	0	0	0	0	$V_{dc}/2$
0	1	1	1	1	1	0	1	0	0	0	0	$V_{dc}/3$
0	0	1	1	1	1	1	1	0	0	0	0	$V_{dc}/6$
0	0	0	1	1	1	1	1	1	0	0	0	0
0	0	0	0	1	1	1	1	1	1	0	0	$-V_{dc}/6$
0	0	0	0	0	1	1	1	1	1	1	0	$-V_{dc}/3$
0	0	0	0	0	0	1	1	1	1	1	1	$-V_{dc}/2$

III. CONTROL AND MODULATION STRATEGIES

The modulation methods used in multilevel inverters can be classified according to switching frequency. The figure 6 shows different modulation strategies with high switching frequency and low switching frequency.

A. Sinusoidal Pulse Width Modulation

The Sinusoidal PWM is the simplest technique the width of each pulse is varied in proportion to the amplitude of a sine wave evaluated at the centre of the same pulse. The distortion factor and lower order harmonics are reduced significantly. The gating signals are generated by comparing a sinusoidal reference signal with a triangular carrier wave of frequency f_c . The frequency of reference signal f_r , determines the inverter output frequency and its peak amplitude A_r , controls the modulation index M . The number of pulses per half cycle depends on carrier frequency.

Figure 6: Block diagram of modulation strategies

B. Multicarrier pulse width modulation

Multi-carrier PWM techniques entail the natural sampling of a reference waveform typically being sinusoidal, through several carrier signals typically being triangle waveforms. The carrier based PWM technique used for the multilevel inverter is based on carrier disposition technique. In the carrier disposition technique the reference is sampled through a number of carrier waveforms displaced by contiguous increment of reference waveform amplitude. The carrier disposition methods used here is Phase Opposition Disposition Sinusoidal Pulse Width Modulating (PODSPWM) technique. The carrier waveforms are all in phase above and below the zero reference value, there is 180° phase shift between the ones above and below zero respectively as shown in figure 7,8 and 9. The significant harmonics are located around the carrier frequency for both the phase and line voltage waveforms.

Figure 7: PODSPWM with two triangle for three level inverter

Figure 8 :PODSPWM with four triangle for five level inverter

Figure 9:POD SPWM with six triangle for seven level inverter

IV. TOTAL HARMONIC DISTORTION

Total harmonic distortion (THD) is an important

figure of merit used to quantify the level of harmonics in voltage or current waveforms, can be defined as the harmonic content of a waveform is compared to its fundamental.

Figure 10 :Waveform with harmonic component

One of the ways of expressing the "goodness" of an device is to use a number, based on measurements at a given power output level, expressing its Total Harmonic Distortion. There will always be some deviation in the shape of the waveform, which can be expressed as a series of "harmonics" of the fundamental frequency as shown in figure 10.

V. PROPOSED TECHNIQUE

A new model for a seven level inverter is designed such that other levels such as level five, level three, level two are in cooperated in the same circuit. By a manual switching inverter can be switched to different levels. The different levels are built in single circuit with the help of a circuit breaker. For each level the corresponding circuit breaker will be active and the corresponding level of inverter will be formed in the circuit. The Harmonic analysis is done for all the levels are done separately using different multi-level inverters by linking ModelSim with MATLAB/Simulink. The block diagram of the proposed model is shown in the Fig 1.

VI. WORK DONE AND SIMULATION

The gating signal generated in the modelsim is shown in figures given below. The input signal and the output signal for level 2, level 3, level 5, level 7 inverter is shown in figure 11, figure 12, figure 13 and figure 14 respectively.

Figure 11 ModelSim simulated PWM signals for seven level inverter

Figure 12 ModelSim simulated PWM signals for seven level inverter

Figure 13 ModelSim simulated PWM signals for seven level inverter

Figure 14 ModelSim simulated PWM signals for seven level inverter

The Simulink model of the proposed design using a Simulink/Modelsim cosimulation is shown in figure 11. This model can be extended to any level upon application. To evaluate the effectiveness and correctness of the proposed technique, a co-simulation work performed by Matlab/Simulink and Modelsim is firstly conducted. Then, an experimental system by FPGA chip, Spartan3 XCS400PQ208 is set up to further validate the performance of the proposed technique.

Finally, the results in simulation and in experiment will be compared and discussed. The Line voltage, phase voltage, FFT analysis of two level inverter is shown in figure 12. The Line voltage, line to ground voltage, FFT analysis of three level inverter is shown in figure 13. The Line voltage, line to ground voltage, FFT analysis of five level inverter is shown in figure 14. The Line voltage, line to ground voltage, FFT analysis of seven level inverter is shown in figure 15.

Figure 11: Simulink model for the adaptable inverter

Figure 12 :Line voltage, line to ground voltage, FFT analysis of two level inverter

Figure 13: Line voltage, line to ground voltage, FFT analysis of three level inverter

Figure 14: Line voltage, line to ground voltage, FFT analysis of five level inverter.

Figure 15: Line voltage, line to ground voltage, FFT analysis of seven level inverter

Figure 16: Total harmonic distortion comparison for different levels of inverter.

The comparison chart for different levels of inverter is shown in figure 16. The THD comparison value for different level of inverter is shown in table IV.

Table IV THD comparison for different levels of inverter

LEVEL OF INVERTER	THD %
2	16.58
3	11.34
5	7.66
7	3.84

VII. HARDWARE SETUP AND RESULT

The hardware implementation of PWM signals for the adaptable level inverter is done using Xilinx Spartan 3XCS4PQ208 FPGA(Field Programmable Gate Array). The figure 17 shows PWM signal .

Figure 17:PODSPWM signal in CRO.

VIII. CONCLUSION

The thesis focus on design and development of an adaptable level inverter circuit and generation of adaptable level gating signal using phase opposition disposition pulse width modulation. The comparison of total harmonic distortion (THD) for different levels of inverter was done and the lowest THD obtained is 3.68%. Considerable reduction of harmonics can be done by increasing the number of levels of the inverter. The possibility of the practical implementation of reconfigurable architecture for power-electronic converter control is experimentally verified with a low-cost FPGA from Xilinx. The capability of reconfigurable architecture can also adopt all major PWM techniques by storing all the PWM schemes in the configuration RAM. The concept of the adaptable level inverter can be extended for multiphase modulators and other multilevel inverter topologies. The proposed technique finds important application in the modern

developing era of technology where constant controlled power supply is continuously required. This concept can be extensively used in automated environment, industrial control, power electronic converter and power system control applications intelligently.

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