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B. DILIP

Dept. of ECE, MVGR college of Engineering, Vizianagaram, AP, India, dil.bagadi@gmail.com

P. SURYA PRASAD

Dept. of ECE, MVGR college of Engineering, Vizianagaram, AP, India, suryaprasadp@yahoo.com

R. S. G. BHAVANI

Dept. of ECE, JNTU Kakinada, AP, India, bhavani.rsg@gmail.com

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LEAKAGE POWER REDUCTION IN CMOS CIRCUITS USING LEAKAGE CONTROL TRANSISTOR TECHNIQUE IN NANOSCALE TECHNOLOGY

B. DILIP¹, P. SURYA PRASAD² & R. S. G. BHAVANI³

^{1&2}Dept. of ECE, MVGR college of Engineering, Vizianagaram, AP, India

³Dept. of ECE, JNTU Kakinada, AP, India

E-mail : dil.bagadi@gmail.com¹, suryaprasadp@yahoo.com², bhavani.rsg@gmail.com³

Abstract – In CMOS circuits, as the technology scales down to nanoscale, the sub-threshold leakage current increases with the decrease in the threshold voltage. LECTOR, a technique to tackle the leakage problem in CMOS circuits, uses two additional leakage control transistors, which are self-controlled, in a path from supply to ground which provides the additional resistance thereby reducing the leakage current in the path. The main advantage as compared to other techniques which involves the sleep transistor is that LECTOR technique does not require any additional control and monitoring circuitry, thereby limits the area increase and also the power dissipation in active state. Along with this, the other advantage with LECTOR technique is that it does not affect the dynamic power which is the major limitation with the other leakage reduction techniques.

Keywords - subthreshold leakage current; transistor stacking; self-controlled LCTs; deep-submicron.

I. INTRODUCTION

The rapid progresses in semiconductor technology have led the feature sizes to be shrunk through the use of deep-submicron processes; thereby the extremely complex functionality is enabled to be integrated on a single chip. In the growing market of mobile hand-held devices used all over the world today, the battery-powered electronic system forms the backbone. To maximize the battery life, the tremendous computational capacity of portable devices such as notebook computers, personal communication devices (mobile phones, pocket PCs, PDAs), hearing aids and implantable pacemakers has to be realized with very low power requirements. With miniaturization and the growing trend towards wireless communication, power dissipation has become a very critical design metric. The longer the battery lasts, the better is the device.

The power dissipation has not diminished even with the scaling down of the supply voltage. The problem of heat removal and power dissipation is getting worse as the magnitude of power per unit area has kept growing. For the rapid increase in power consumption of present day chips, the innovative cooling and packaging strategies are of little help. Also, the cost associated with the packaging and the cooling of such devices is becoming prohibitive. In addition to cost, the issue of reliability is a major concern. Component failure rate roughly doubles for every 10°C increase in operating temperature. With the on-chip devices doubling every two years, minimizing the power consumption has become currently an extremely challenging area of research.

Leakage power of a CMOS transistor depends on gate length and oxide thickness [4]. To decrease the dynamic power, the supply voltage is decreased which leads to the performance degradation. To speed up the device, the threshold voltage should also be scaled down along with the supply voltage, which results in exponential increase in the sub-threshold leakage current, thereby increase in the static power dissipation. The main components of leakage current in a MOS transistor are shown in Figure 1.

Fig. 2 : Reverse current in CMOS inverter

The leakage power in a CMOS is due to sub-threshold leakage current; which is the reverse current flowing through the OFF transistor, indicated with arrows in Figure 2. As the technology scales down which is the shrinking of feature size of transistor, the channel length decreases, thereby increasing the amount of leakage power in the total power dissipated as shown in Figure 3.

Fig. 3 : Technology Vs Leakage Power.

II. LIMITATIONS WITH RELATED WORK

A. MTCMOS

A high-threshold NMOS gating transistor is connected between the pull-down network and the ground, and low-threshold voltage transistors are used in the gate. The reverse conduction paths exist, which tends the noise margin to reduce or may result in complete failure of the gate. There also exists a performance penalty due to the high-threshold transistors in series with all the switching current paths.

Dual V_T technique is a variation in MTCMOS, in which the gates in the critical path use low-threshold transistors and high-threshold transistors for gates in non-critical path [3], [7]. Both the methods requires additional mask layers for each value of V_T in fabrication, which is a complicated task depositing two different oxides thickness, hence making the fabrication process complex. The techniques also suffer from turning-on latency i.e., the idle subsections of circuit cannot be used immediately after reactivated since some time is needed to return to normal operating condition. The latency is typically a few cycles for former method, and for Dual technology, is much higher. When the circuit is active, these techniques are not effective in controlling the leakage power.

B. SLEEP Transistor Technique

This is a State-destructive technique which cuts off either pull-up or pull-down or both the networks from supply voltage or ground or both using sleep transistors. This technique is MTCMOS, which adds high- V_{th} sleep transistors between pull-up networks

and V_{dd} and pull-down networks and gnd while for fast switching speeds, low- V_{th} transistors are used in logic circuits [8]. Isolating the logic networks, this technique dramatically reduces leakage power during sleep mode. However, the area and delay are increased due to additional sleep transistors. During the sleep mode, the state will be lost as the pull-up and pull-down networks will have floating values. These values impact the wakeup time and energy significantly due to the requirement to recharge transistors which lost state during sleep.

C. Forced Stack

In this technique, every transistor in the network is duplicated with both the transistors bearing half the original transistor width [6]. Duplicated transistors cause a slight reverse bias between the gate and source when both transistors are turned off. Because sub-threshold current is exponentially dependent on gate bias, it obtains substantial current reduction. It overcomes the limitation with sleep technique by retaining state but it takes more wakeup time.

D. ZIGZAG Technique

Wake-up cost can be reduced in zigzag technique but still state losing is a limitation. Thus, any particular state which is needed upon wakeup must be regenerated somehow. For this, the technique may need extra circuitry to generate a specific input vector.

E. SLEEPY STACK Technique

This technique combines the structure of the forced stack technique and the sleep transistor technique. In the sleepy stack technique, one sleep transistor and two half sized transistors replaces each existing transistor [10]. Although using of $W/2$ for the width of the sleep transistor, changing the sleep transistor width may provide additional tradeoffs between delay, power and area. It also requires additional control and monitor circuit, for the sleep transistors.

F. LEAKAGE FEEDBACK Technique

This technique is based on the sleep approach. To maintain logic during sleep mode, the leakage feedback technique uses two additional transistors and the two transistors are driven by the output of an inverter which is driven by output of the circuit implemented utilizing leakage feedback. Performance degradation and increase in area are the limitations along with the limitation of sleep technique.

G. SLEEPY KEEPER Technique

This technique consists of sleep transistors connected to the circuit with NMOS connected to V_{dd} and PMOS to Gnd. This creates virtual power and ground rails in the circuit, which affects the switching speed when the circuit is active [9]. The identification of the idle regions of the circuit and the generation of the sleep signal need additional hardware capable of predicting the circuit states accurately, increasing the area requirement of the circuit. This additional circuit consumes power throughout the circuit operation to continuously

monitor the circuit state and control the sleep transistors even though the circuit is in an idle state.

III. LECTOR TECHNIQUE

The effective stacking of transistors in the path from supply voltage to ground is the basic idea behind the LECTOR technique for the leakage power reduction. This is stated based on the observation from [1], [2] and [5] that “a state is far less leaky with more than one OFF transistor in a path from supply voltage to ground compared to a state with only one OFF transistor in the path”. The number of OFF transistors is related to leakage power as shown in Figure 4.

Fig. 4 : Transistor-stacking Vs Leakage Power.

In this technique, two leakage control transistors are introduced between pull-up and pull-down network within the logic gate (one PMOS for pull-up and one NMOS for pull-down) for which the gate terminal of each leakage control transistor (LCT) is controlled by the source of the other. This arrangement ensures that one of the LCTs always operates in its near cutoff region.

Fig. 5. LECTOR CMOS Gate

The topology of a LECTOR CMOS gate is shown in Figure 5. Two LCTs are introduced between nodes N1 and N2. The gate terminal of each LCT is controlled by the source of the other, hence termed as self-controlled stacked transistors. As LCTs are self-controlled, no external circuit is needed; thereby the limitation with the sleep transistor technique has been overcome. The introduction of LCTs increases the resistance of the path from Vdd to Gnd, thus reducing the leakage current.

Leakage Control Transistor (LECTOR) technique is illustrated in detail with the case of an inverter. A LECTOR INVERTER is shown in Figure 6. A PMOS is introduced as LCT1 and a NMOS as LCT2 between N1 and N2 nodes of inverter. The output of inverter is taken from the connected drain nodes LCT1 and LCT2. The source nodes of LCT1 and LCT2 are the nodes N1 and N2 respectively of the pull-up and the pull-down logic. The gates of LCT1 and LCT2 are controlled by the potential at source terminal of LCT2 and LCT1 respectively. This connection always keeps one of the two LCTs in its near cutoff region for any input.

Fig. 6 : LECTOR based CMOS Inverter

When $V_{dd} = 1V$, input $A = 0$, the voltage at the node N2 is 800 mV. LCT1 cannot be completely turned OFF as the voltage is not sufficient. Hence, the LCT1 resistance will be near to but slightly lesser than its OFF resistance, allowing conduction. The resistance provided by LCT1, even though not equal to the OFF resistance, increases the resistance in the path of supply voltage to ground, thereby reducing the sub-threshold leakage current, attaining reduction in leakage power. Similarly, when input $A = 1$, the voltage at the node N1 is 200 mV; hence LCT2 will be operated in near cutoff state. The states of all the transistors in the LECTOR inverter for all possible inputs are tabulated in Table I.

TABLE I. STATE MATRIX OF LCT INVERTER

Transistor Reference	Input Vector (A)	
	0	1
M1	ON State	OFF State
M2	OFF State	ON State
LCT1	Near Cut-OFF State	ON State
LCT2	ON State	Near Cut-OFF State

Along with the resistance in the path, the propagation delay of the gate also gets increased. The transistors of LCT inverter are sized such that the propagation delay is reduced or equal to its base case.

In the sleep related technique, the sleep transistors have to be able to isolate the power supply and/or ground from the rest of the transistors of the gate. Hence, they need to be made bulkier dissipating more dynamic power. This offsets the savings yielded when the circuit is idle. Sleep transistor technique depends on input vector and it needs additional circuitry to monitor and control the switching of sleep transistors, consuming power in both active and idle states. In comparison, LECTOR generates the required control signals within the gate and is also vector independent.

Two transistors are added in LECTOR technique in every path from V_{dd} to gnd irrespective of number of transistors in pull-up and pull-down network. Whereas, forced stacks have 100% area overhead. The loading requirement with LCTs is a constant which is much lower. Whereas, the loading requirements with forced stacks depend on number of transistors added and are huge. Hence, the performance degradation is insignificant in the case of LECTOR, and we overcome the drawback faced by forced stack technique.

IV. APPLYING LECTOR TO CMOS CIRCUITS

Various circuit applications of the LECTOR technique are explored in this section. The LECTOR technique is applied to the following CMOS circuits and also their respective base case are implemented to calculate the amount of leakage power reduced in LECTOR technique.

A. LECTOR based NAND gate

Fig. 7 : 2-input LCT NAND

Fig. 8 : Simulation waveforms of LECTOR NAND

The 2-input CMOS NAND gate is shown in Figure 7 with the two LCTs added to pull-up and pull-down network between the V_{dd} and gnd path. The simulation waveforms of LECTOR NAND from Figure 8 show that the basic characteristics of NAND are retained by LECTOR NAND.

B. 4-input AND-OR-Invert

Fig. 9 : Four input AOI

The SCCG (static CMOS complex gate) implementation of a 4-input AOI is shown in Figure 9, through which the area overhead can be reduced. The LECTOR implementation here needs only two additional transistors to be placed between the pull-up and pull-down network at the node from which the output is taken.

Fig. 10 : Simulation waveforms for LECTOR AOI

Through the simulation waveforms shown in Figure 10, the characteristics of LECTOR AOI resemble the base case.

C. 4:1 Multiplexer

Fig. 11: A 4:1 Multiplexer

The gate level schematic of 4:1 multiplexer is shown in Figure 11. The LECTOR implementation involves the addition of two LCTs in each gate between the supply and ground path.

Fig. 12: Simulation waveforms for LECTOR MUX

The simulation waveform shown in Figure 12 represents the LECTOR Multiplexer through which it can be observed that its characteristics resemble that of the conventional case.

D. Full Adder

Fig. 13: A Full Adder

The Gate level schematic of Full Adder is shown in Figure 13. The LECTOR implementation involves the addition of two LCTs for each gate. The transistor level schematic for ex-or gates is similar to that of And-Or-Invert.

Fig. 14 : Simulation waveforms for LECTOR Full Adder

The simulation waveforms for full adder as shown in Figure 14, resembles the characteristics of conventional full adder.

V. EXPERIMENTAL RESULTS

The leakage power is measured using the HSPICE simulator. The results obtained through the technique for 2-input NAND gate is shown in Table III. Simulation for the 2-input NAND is performed by taking four different process parameters Viz. 180nm, 90nm, 65nm and 45nm.

TABLE II. SUPPLY VOLTAGES AND THRESHOLD VOLTAGE VALUES

Technology	180nm	90nm	65nm	45nm
Supply Voltage	1.8V	1.2V	1.1V	1V
NMOS V_T (V)	0.3999	0.2607	0.22	0.1711
PMOS V_T (V)	-0.42	-0.303	-0.22	-0.1156

The supply voltages to be considered for the four process parameters (technologies) along with the threshold voltages for NMOS and PMOS in the respective technologies are as shown in Table II.

TABLE III. 2-INPUT NAND RESULTS FOR VARIOUS TECHNOLOGIES

Technology	Leakage power (nW)		%age decrease in power dissipation
	Base case	LECTOR	
180nm	1.158	0.937	19.035
90nm	2.884	1.647	42.883
65nm	13.977	11.837	15.313
45nm	1503.66	1135.05	24.514

Table IV gives the results for 4-input AOI for 90nm and 45nm technologies. Table V gives the results for 4:1 Multiplexer and Full Adder under 90nm process parameters.

TABLE IV. RESULTS FOR 4-INPUT AOI

		4-input AOI	
		90nm	45nm
Leakage Power(W)	CONVENTIONAL	3.76E-09	2.13E-06
	LECTOR	2.45E-09	1.65E-06
Percentage decrease in Power Dissipation		34.914	22.223

TABLE V. RESULTS FOR 4:1 MULTIPLEXER AND FULL ADDER

		4:1 Multiplexer	Full Adder
Leakage Power(nW)	CONVENTIONAL	38.558	42.37
	LECTOR	21.354	24.248
Percentage decrease in Power Dissipation		44.618	42.771

Leakage power dissipation is taken as the average of power dissipations obtained at all the possible input vectors of the CMOS circuit. There are 4 possible combinations for 2-input NAND, hence the average of the four power dissipations gives the leakage power. In the case of 4-input AOI, power dissipations corresponding to all the 16 combinations are averaged. For Multiplexer, the average of 64 power dissipations is considered and for full adder, the average of 8 power dissipations is considered to be as the static power dissipated. In each case, the leakage power is measured by exciting both the circuits (Conventional and LECTOR) with same set of input vectors.

VI. CONCLUSION

The increase in leakage power because of the scaling down of device dimensions, supply and

threshold voltages in order to achieve high performance and low dynamic power dissipation, becomes more with the deep-submicron and nanometer technologies and thus it becomes a great challenge to tackle the problem of leakage power. LECTOR uses two LCTs which are self-controlled transistors. LECTOR achieves the reduction in leakage power like other leakage reduction techniques, such as sleepy stack, sleepy keeper, etc, along with the advantage of not affecting the dynamic power, since this technique does not require any additional control and monitor circuitry and also in this technique, the exact logic state is maintained.

The LECTOR technique when applied to generic logic circuits achieves up to 40-45% leakage reduction over the respective conventional circuits without affecting the dynamic power. A tradeoff between Propagation delay and area overhead exists here as the delay reduction by sizing the transistors will increase the area overhead.

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