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A TRANSISTOR LEVEL ANALYSIS FOR A 8-BIT VEDIC MULTIPLIER

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Abstract: Power and area efficient multiplier using CMOS logic circuits for applications in various digital signal processors is designed. This multiplier is implemented using Vedic multiplication algorithms mainly the "Urdhvatiyakbhyam sutra", which is the most generalized one Vedic multiplication algorithm [1]. A multiplier is a very important element in almost all the processors and contributes substantially to the total power consumption of the system. The novel point is the efficient use of Vedic algorithm (sstras) that reduces the number of computational steps considerably compared with any conventional method. The schematic for this multiplier is designed using TANNER TOOL. The design is then verified in T-SPICE using 0.18 μm CMOS technology library file. The analysis is made for various voltages across a range of 2.5V to 5V, to validate the design. A CMOS digital multiplier, with low power consumption and high linearity is proposed. The results prove that the proposed multiplier consumes 80% less power compared to the gate level analysis done earlier. The core area of the proposed multiplier is 737 μm^2 . Paper presents a systematic design methodology for this improved performance digital multiplier based on Vedic mathematics.

Keywords: Multiplier, Vedic algorithms, Vedic Mathematics, UrdhvaTiryakBhyam sutra.

1. INTRODUCTION

A Multiplier, no doubt, is one of the most important block in any processor now a days. A binary multiplier is an electronic circuit used in digital electronics, such as a computer, to multiply two binary numbers. A variety of computer arithmetic techniques can be used to implement a digital multiplier. Most techniques involve computing a set of *partial products*, and then summing the partial products together [2]. This process conducting long multiplication on base-10 integers, but has been modified here for application to a base-2 (binary) number system. As more transistors per chip became available due to larger-scale integration, it became possible to put enough adders on a single chip to sum all the partial products at once, rather than reuse a single adder to handle each partial product one at a time.

As the common digital signal processing algorithms spend most of their time multiplying, the processors spend a lot of chip area in order to make the multiplication as fast as possible. Hence a non conventional yet very efficient Vedic mathematics is used for making a high performance multiplier. Vedic Mathematics deals mainly with various Vedic mathematical formulae and their applications for carrying out large arithmetical operations easily [3].

To evaluate the performance of the new multiplier, the multiplier is compared with the already existing digital multipliers on various parameters as power consumption and speed of operation.

2. VEDIC MULTIPLICATION ALGORITHM

2.1 The Vedic Sstras

Depending on the various branches of mathematics, Vedic algorithms are divided into 16 sstras (algorithms) [4], out of which two sstras are for multiplication as:

1. Nikhilam Navatashcaramam Dashatah – All from 9 and the last from 10.
2. Urdhva-Tiryagbhyam – Vertically and crosswise.

This paper is based on Urdhva-Tiryagbhyam sutra of Vedic multiplication, which is the most generalized method for multiplication. This sutra is used for binary multiplication for making the digital multiplier. It can be synonymously called as "Vertically and Crosswise" method of multiplication. An illustration of this multiplication algorithm is shown in the figure 1 below. Considering a digital hardware, a Vedic multiplier will be more power efficient and more faster also as less number of steps are required for multiplication. Also there is hardly any limitations attached to this multiplication algorithm.

2.2 Binary multiplication using Urdhva-Tiryakbhyam Sutra

Figure 1 below shows the generalized line-diagram structure of the Urdhva-Tiryakbhyam algorithm. This algorithm is applicable in all cases (binary multiplication, decimal multiplication etc.) and may be applied even in the case of division of two numbers [4],[5]. All the multiplications being done here are in vertical and crosswise directions,

requiring only 7 steps for multiplication of two , 4 bit numbers .

Fig.1 Line-Diagram for Urdhva-Tiryagbhyam Sutra multiplication

3. VLSI TECHNOLOGY USING CMOS LOGIC

Large integrated circuits can be constructed using CMOS logic with very low static power consumption. The increasing demand for low-power very large scale integration(VLSI) can be addressed at different design levels, such as the architectural, circuit, layout, and the process technology level .At the circuit design level, considerable potential for power savings exists by means of proper choice of a logic style for implementing combinational circuits. This is because all the important parameters governing power dissipation—switching capacitance, transition activity, and short-circuit currents—are strongly influenced by the chosen logic style. Depending on the application, the kind of circuit to be implemented, and the design technique used, different performance aspects become important. In the past, the parameters like high speed, small area and low cost were the major areas of concern, whereas power considerations are now gaining the attention of the scientific community associated with VLSI design. In recent years, the growth of personal computing devices (portable computers and real time audio and video based multimedia applications) and wireless communication systems has made power dissipation a most critical design parameter [6] .In the absence of low-power design techniques such applications generally suffer from

very short battery life, while packaging and cooling them would be very difficult and this is leading to an unavoidable increase in the cost of the product.

In multiplication, reliability is strongly affected by power consumption. Usually, high power dissipation implies high temperature operation, which, in turn, has a tendency to induce several failure mechanisms in the system [7]. Power dissipation is the most critical parameter for portability & mobility and it is classified in to dynamic and static power dissipation. Dynamic power dissipation occurs when the circuit is operational, while static power dissipation becomes an issue whether circuit is inactive or is in a power-down mode. There are three major sources of power dissipation in digital CMOS circuit which are summarized in equation (1)

$$P_{avg} = P_{switching} + P_{short\ circuit} + P_{leakage} \quad (1)$$

The first term represents the switching component of power, The second term is due to the direct-path short circuit current, I , which arises when both the NMOS and PMOS transistors are simultaneously active, conducting current directly from supply to ground. Finally, leakage current, which can arise from substrate injection and sub-threshold effects, is primarily determined by fabrication technology considerations.

The switching power dissipation in CMOS digital integrated circuits is a strong function of the power supply voltage (V) and emerges as a very effective means of limiting the power consumption. However, the saving in power Therefore, reduction of dissipation comes at a significant cost in terms of increased circuit delay. Since the exact analysis of propagation delay is quite complex, a simple first order derivation can be used to show the relation between power supply and delay time [8].

$$\frac{1}{2} C_L V^2 \quad (2)$$

K - Transistor's aspect ratio (W/L)

V_{th} - Transistor threshold voltage

4. 8-BIT MODULAR VEDIC MULTIPLIER

A 8-bit VEDIC multiplier is made using four, 4 bit vedic multipliers and three, 16 bit adders. The design is then simulated in Tanner tool. This design consists of 1638 MOSFETS with a total of 1593 nodes. The smallest sub-circuit instance being used here is of a

full adder. The systematic design flow then includes a 4-bit Vedic multiplier and finally the 8-bit Vedic multiplier.

Module 1:- A 14-T full-adder cell [9] :

The full adder being used here is a 14 transistor adder based on complementary pass-transistor logic (CPL) [11]. The general structure of the 14 transistor adder is shown in the figure2(a) below. It is composed of XOR/XNOR gate instances combined together to make a low power full-adder cell with high node voltage swings [9],[10]. The sum and carry (Cout) outputs are generated from the binary inputs A, B, Cin and expressed as

$$\text{Sum} = A \text{ XOR } B \text{ XOR } \text{Cin} \quad (3)$$

$$\text{Cout} = A \cdot B + \text{Cin} \cdot (A \text{ XOR } B) \quad (4)$$

Fig. 2(a) and Fig. 2(b) below shows the respective schematic and simulation results on Tanner .

Fig. 2(a) 14-T cell using CMOS logic

Simulation in tanner tool :

Fig. 2(b) Schematic for 14 transistor full-adder in tanner tool.

The simulation result of the full-adder cell is shown in the Fig. 2(c) below. This design is simulated in 180nm library file (.md file) and the cell instance is made. Here binary 1 is shown in volts (2.5v) and binary 0 in milli-volts (around 40mv). Using this full-adder cell instance , a 5-bit adder is made which will be used in 4-bit Vedic multiplier design.

Simulation results for the 14 transistor full-adder cell:

Fig. 2(c). Input stimulus for a full-adder cell. The bottom three are inputs A, B, and Cin and the remaining two are outputs (Cout and Sum)

MODULE 2 :- 4-bit Vedic multiplier

Fig.3(a) 4-bit Vedic multiplier design

The 4-bit Vedic multiplier design using adders and gate instances is shown in the figure 3(a) above. Two 4-bit inputs VA and VB are multiplied here. The first input is a3a2a1a0 and second b3b2b1b0. All the instances used here are made using CMOS logic.

This design is now simulated using T-SPICE as shown in Fig. 3(b) below.

Simulation in tanner tool :

Fig. 3(b) Schematic for 4-bit Vedic multiplier in tanner tool.

Simulation results: inputs : VA= a3a2a1a0 (MSB TO LSB)

VB= b3b2b1b0 (MSB TO LSB)

Fig.3(c) Input values for multiplier as VA= 1001 & VB=1010

In the Fig. 3(c) the upper four values denote the first input VA as 1001 i.e. a3a2a1a0 and lower four bits denote the second input value VB as 1010 i.e. b3b2b1b0. The 1's are shown in volts (5v) and 0's in fermivolts.

In the figure 3(d) the uppermost bit shows the MSB of the result (c6) and descending towards the bottom, figure shows the lower bits till the LSB (r0) as the last bit. The complete output bit pattern is thus c6r6r5r4r3r2r1r0 which comes out to be 01011010.

The 1's at the output are shown in volts(4.6 v) and 0's at the output are shown in mili-volts (5.6 mv). This design is simulated in 180nm model file which has a threshold value of .36v (for both nmos and pmos transistors) so the zero's (shown in mv) are not going to affect the switching characteristics of the transistors.

Simulation Output : c6r6r5r4r3r2r1r0 (MSB TO LSB)

Fig. 3(d) Output value of the multiplier, 01011010

Module 3 :- Modular 8-bit digital Vedic multiplier using four, 4-bit multipliers

Now using the results of the 4-bit Vedic multiplier obtained above a 8-bit multiplier is designed. In this 8-bit multiplier the 8-bit input is divided into two halves of 4 bit each [12]. Considering two 8-bit inputs as VX and VY as shown in figure 4(a) below, VX is divided as "a" and "b" where "a" represents the upper 4 bits and "b" represents the lower 4 bits. Similarly VY is also divided as upper half and the lower half and denoted by "c" and "d" respectively. The multiplication steps for this modular multiplier is shown below.

Fig.4(a) Two 8-bit inputs VX and VY

Steps for designing a 8-bit multiplier :-

Step1 : $b*d$

Step2 : $a * d$ and shifting the result by 4 bits

Step3 : $b * c$ and shifting the result by 4 bits

Step4 : $a * c$ and shifting the result by 8 bits

Step5: Adding the results obtained from step1, step2, step3 and step4

Simulation in tanner tool :

Fig. 4(b) Schematic design for the 8-bit Vedic multiplier .

Simulation result :

Fig. 4(c) output value of the multiplication obtained after random input values

VX = 10001

VY = 100,

giving the output value as 1000100.

In the simulated circuit of the 8-bit Vedic multiplier four instances of 4-bit Vedic multiplier, and 3 instances of 16- bit adder are used. At the output the 1's are shown in volts (5v) and zero's in mv. The circuit is simulated in T-SPICE using 180-n model file .

5. SIMULATION RESULT ANALYSIS

The multiplier blocks are simulated using T-SPICE netlist and the results are verified for both the 4-bit and 8-bit multiplier.

(i) For the 4-bit Vedic multiplier :

Measurement result summary

avgpower = 1.3714e-002 W

Core Area = 108 μm^2

Processor time required = 4.43 Seconds

(ii) For the 8-bit Vedic multiplier:

Measurement result summary

avgpower = 9.3868e-002 W

Core Area = 737 μm^2

Processor time required = 14.13 Seconds

Both for a transition time of 100ns. When compared with the results obtained in [13] , the power consumption and processor time required is found to be very less. The power consumption using the gate level analysis in [13] for a 4-bit multiplier is found to be 0.45W whether the results obtained in this paper using transistor level analysis , gives it to be around 13 mW . The power consumption for the 8-bit multiplier structure here using four , 4-bit multipliers is found to be around 93 mW The processor time required in the gate level analysis in [13] is 6.42 Seconds for the 4-bit multiplier against the 4.43 seconds obtained in the Vedic multiplier designed above using CMOS VLSI technology. Again the computational steps are also reduced and hardware implementation required will also be less as compared to the conventional methods and hence enhancing the performance of the overall system.

6. CONCLUSION

This paper represents a efficient Vedic multiplier design using VLSI technology. Almost 80% power reduction at 2.5 volts can be achieved using this Vedic multiplier as compared to its earlier counterparts using gate level analysis or the conventional ways of multiplication. The processor's time consumption is reduced from 6.42 Seconds to 4.43 Seconds for the 4-bit Vedic multiplier and the computational complexity is also less as it is requiring fewer number of steps as compared to conventional multiplication methods. For a real world application of this multiplier, it is implemented for finding out the determinant of a 2 X 2 matrix which will be having two, 8-bit multipliers and

finding the difference of both using two's compliment.

All the circuits have been designed using TANNER EDA [14]. The total power consumption estimation depends on various parameters [15]. This multiplier can be implemented in digital signal processing and VLSI signal processing applications for getting high performance of the system. But as the multiplier is using large number of MOSFETS so the transistor's switching characteristics also needs to be kept in mind and buffers will be required at various nodes inside the circuit for avoiding the voltage drop inside the circuit [16]. The design algorithm and the results show that this Vedic multiplier requires less area and consumes less power as compared to the conventional multipliers.

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