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Design & Implementation of Low Power 3-bit Flash ADC in 0.18 μ m CMOSPradeep Kumar¹, Amit Kolhe²

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Abstract- This paper describes the design and implementation of a Low Power 3-bit flash Analog to Digital converter (ADC). It includes 7 comparators and one thermometer to binary encoder. It is implemented in 0.18 μ m CMOS Technology. The pre-simulation of ADC is done in T-Spice and post layout simulation is done in Microwind3.1. The response time of the comparator equal to 6.82ns and for Flash ADC as 18.77ns. The Simulated result shows the power consumption in Flash ADC as 36.273mw. The chip area is for Flash ADC is 1044 μ m².

Keywords- CMOS, Flash ADC, Comparator

I. INTRODUCTION

Applications such as wireless communications and digital audio and video have created need for cost-effective data converters that will achieve higher speed and resolution. The needs required by digital signal processors [1] continually challenge analog designers to improve and develop new ADC and DAC architectures. There are many different types of architectures, each with unique characteristics and different limitations[2]. Figure.1. shows the general block diagram of ADC. Flash analog-to-digital converters, also known as parallel ADCs, are the fastest way to convert an analog signal to a digital signal. Flash ADCs are ideal for applications requiring very large bandwidth; however, they typically consume more power than other ADC architectures and are generally limited to 8-bits resolution.

II. ARCHITECTURE

Fig.2. shows a typical flash ADC block diagram. For an "N" bit converter, the circuit employs 2^{N-1} comparators. A resistive divider with 2^N resistors provides the reference voltage. The reference voltage for each comparator is one least significant bit (LSB) greater than the reference voltage for the comparator immediately below it. Each comparator produces a "1" when its analog input voltage is higher than the reference voltage applied to it. Otherwise, the comparator in Fig.3.output is "0". Comparatator design specification is shown in Table I Thus, if the analog input is between vx4 and vx5,

Fig. 1. Block for 3 Bit Flash ADC

comparators x1 through x4 produce "1"s and the remaining comparators produce "0"s. The point where the code changes from ones to zeros is the point where the input signal becomes smaller than the respective comparator reference voltage levels.

Fig. 2. Circuit for a 3 Bit Flash ADC

A. Comparator Circuit & Design Specification

Fig.3. Low power Comparator circuit used in proposed Flash ADC

TABLE I

DESIGN SPECIFICATION FOR COMPARATOR

Technology	0.18u CMOS Technology
Supply Voltage	$\pm 1.3V$
Resolution	3-bit
Voltage Gain	>10000
Slew Rate	20v/us
C_L	1.25pf
Vout Range	$\pm 2.0V$
Gain Bandwidth	30MHz _z

B. Thermometer to Binary Encoder Design

Below table II show the two digital codes. This table can be used to design a suitable combinational circuit as Fig.4. From the above table using K' map technique below equations are derived.

$$O1 = C1$$

$$O2 = D2 + C1'B1 + B1'A2$$

$$O3 = E1D2 + D2'D1 + C1'B1 + A2'A1$$

Fig.4. Thermometer to Binary Encoder

TAB
LE
II
THERMOMETER TO BINARY ENCODER

Thermometer code							Binary Code		
E1	D2	D1	C1	B1	A2	A1	O1	O2	O3
0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	0	0	1
0	0	0	0	0	1	1	0	1	0
0	0	0	0	1	1	1	0	1	1
0	0	0	1	1	1	1	1	0	0
0	0	1	1	1	1	1	1	0	1
0	1	1	1	1	1	1	1	1	0
1	1	1	1	1	1	1	1	1	1

ENCODER

III. SIMULATION RESULTS

Pre-layout and Post-layout Simulation Results prepared with 220 dpi resolution and saved with no compression, 8 bits per pixel (256 color or grayscale)

A Pre-layout Simulation Results

1. Comparator Output Waveform

As shown in fig.4, a sine wave signal is applied to the noninverting terminal of the comparator and a reference signal is applied to the inverting terminal of the comparator. We have got the following waveform.

Fig.4. Comparator output

2. Comparator Response Time

We have got the response time of the comparator equal to 6.82ns. Below fig.5 shows the response time of the comparator.

Fig.5. Comparator Response time

Fig.7. ADC Response Time

3.ADC Output Waveform

Fig.6. Flash ADC Output

As shown in the Fig.6., as the input signal's amplitude increases output signal in digital format also increases. Here output is swing from 0v to 1.3v.

4.ADC Response Time

We have got the response time of the ADC comparator equal to 18.77ns. Below fig.7 shows the response time of the Flash ADC

B.Post Layout Simulation Results

1.Layout of Comparator

Fig.8. Comparator Layout

2.Layout of ADC

Below figure shows the layout of the complete flash ADC. It includes seven comparators and one thermometer to binary encoder.

Fig.9. ADC layout

3. Comparator Output Waveform

Fig.10. Comparator Output

Above fig.8 and fig.9.layout simulated to have fig.10. And 11 shows the output of comparator when the sine wave signal is applied to the non-inverting terminal of the comparator in fig.10.

4. ADC Output Waveform

Bellow fig.11. shows the output of the 3-bit Flash ADC taken in the microwind3.1. here the total power dissipation of the ADC is 36.273mw.

Fig.11. ADC Output

IV. RESULTS

The 3-bit ADC based on flash type is designed in standard CMOS 0.18 μ m technology and the simulations are done by using Hspice. The supply voltage is given as 1.3V and the input range is set as 1.5V. The pre-simulation of ADC is done in T-Spice and post layout simulation is done in Microwind3.1. The various aspects of the ADC are summarized in Table III as follows.

TABLE III
SPECIFICATION SUMMARY FOR FLASH ADC

Technology	0.18 μ m
Resolution	3-bit
Power supply	1.3 v
Input Voltage Range	0 to 1.5V
Frequency	20 MHz
Resolution time	18.77ns
Power Dissipation	36.237mw
Chip area	1044 μ m ²

V. CONCLUSIONS AND FUTURE WORKS

In this paper, a 3 Bit flash ADC architecture with low hardware complexity and low latency is proposed. This 3bit flash type Analog to digital converter have limitations such as this device is accurate for the conversion of analog voltage to digital form from 0 to 3 voltage in amplitude and for accurate result the input voltage should be greater or lesser than the reference voltage of the comparator about ± 0.05 volt. Moreover, this architecture can be extended to medium-to-high resolution applications because this simplicity of the circuit.

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