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AUTOMATIC SYNCHRONISED FSM BASED TRAFFIC LIGHT CONTROLLER

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ABSTRACT: Traffic light controller is designed to show the behavior of the traffic lights system and also a kind of good sequential circuit. Xilinx vivado is a tool which is being used to Annalise the heavy traffic by analyzing it through the various tools such as NEXYS-4, ARTIX -7, FPGA Board. The approach can be success by allowing a proper access to the areas shared through the multiple intersections and allocating effective time between various users, on or off the peaking hours. Theoretically the waiting times for drivers during peak hours has been reduced further, therefore this is system is better than the one which is being used at the moment. Further improvements include addition of other function to the designed circuit which suits to the various upcoming traffic conditions at different location. Traffic is the one of the biggest problem in this modern world due to this problem so many people are suffering even ambulances are not getting out of traffic in cities. This is our small initiation to make easy flow and control of traffic.

Keywords: NEXYS-4, ARTIX -7, FPGA Board

1. INTRODUCTION

One of the busiest traffic lights in Hyderabad city, Telangana known and used as the reference model for the planning road construction of the traffic intersection .there are three square measures and six traffics represented by t1, t2, t3, t4, t5 and t6 to be controlled. t1 and t2 have been identified as the main road for the first junction while t4 and t6 are the second junction. The last two traffic lights t3 and t5 are the smallest roads .the traffic flows are symbolized by arrows.

Traffic lights contain completely 3 different colors of lights they're Red, Yellow and Green.

If Red light on: This suggests driver should stop.

If yellow on: This suggests driver to form his vehicle slow, signal is near to amendment.

If Green on: This means driver can start driving from signal.

The heart of the system could be a Finite State Machine that directs the unit to light the main and side street lights at appropriate times for the specified time intervals. This unit depends on many inputs that square measure generated outside the system like sensors output that shows the density of vehicles at different sides of the roads, Time waited by the vehicles at different sides of road.

2. BLOCK DIAGRAM

Block diagram consists of clock divider and traffic light controller. Traffic light controller relies on intensity of Traffic that is directly depends on the number of vehicles i.e., load density that is mentioned in our project.

STATE DIAGRAM:

Below figure shows the state diagram illustration of traffic light controller. During this state diagram the output depends upon gift state as well as present input so we considered Mealy FSM technique instead of Moore's technique in order to progress further.

3. COMPUTER CODE DISCRIPTION

In this project, we have a tendency to square measure planning association Intelligent Transport System application for Traffic Light Controller (TLC) by victimization Field Programmable Gate Array (FPGA). FPGA are used for a colossal vary of applications. After the introduction of the FPGA, the sector of programmable logic has expanded exponentially. Because of its easy style and maintenance, implementation of custom made chips has shifted.

The integration of FPGA and all the small devices will be done integrated by using Very Large Scale Integration (VLSI).

The code is written in Verilog HDL design pattern and synthesis is done in XILINX of version 14.5.

FPGA:

Normally FPGAs comprise of:

- Programmable logic blocks that implement logic functions.
- Programmable routing that connects these logic functions.
- I/O square measure organized in a logic blocks through routing interconnect and that make off-chip connections.

A generalized example of an FPGA is shown in figure where configurable logic blocks are arranged in a two dimensional grid and are interconnected by programmable routing resources. I/O blocks are arranged at the periphery of the grid and they are also connected to the programmable routing interconnect. The “programmable/reconfigurable” term in FPGAs indicates their ability to implement a new function on the chip after its fabrication is complete. The reconfigurability/programmability of the FPGAs based on an underlying programming technology, which might cause the amendment in behavior of a pre-fabricated chip once it is fabrication.

FPGA

To create a project

Project Navigator allows you to manage your FPGA and CPLD designs using an ISE. First, we must create a project and then, add source files, and set process properties. After you create a project, you can run processes to implement, constrain, and analyze your design.

Project Navigator provides a wizard to help you create a project as follows.

Creating a Project:

- Select **File > New Project** to launch the New Project Wizard.
- In the Create New Project page, set the name, location, and project type, and click **Next**.
- For EDIF or NGC/NGO projects only: In the Import EDIF/NGC Project page, select the input and constraint file for the project, and click **Next**.

In the Project Settings page, set the device and project properties, and click **Next**. In the Project Summary page, review the information, and click **Finish** to create the project.

In the project we have done coding in python language for easy understanding and access of resources.

4. WORKING

Initially we have a tendency to reset the system and subsequently support the traffic intensity it starts operating first on one side it gives green light rest all lights of the traffic system will be red. once traffic is moderate and nearly equal from all direction of road it will give signal lights one after the other in a clockwise direction. When traffic is heavy at one side and moderate at other side it gives more time of green light for that road and less time for the road which has less traffic.

Here we classified signal changing by states state- 1, 2, 3, 4.

1. Signal on other faces goes to red and once side it will be green.
2. After certain time signal goes to yellow and red and moves to state2
3. Where light changes to red in all lights
4. Once again the red signal turns into green after some time it comes back to yellow and red.

SIMULATION RESULTST:

In this stimulated result we can clearly observe that once input switch varies then output time delay also varies according to the input.

We can built enhancement to the current system by adding solar power supply and some other improvements for pedestrian crossing and help assist for physically handicapped people and for senior citizens while crossing road.

5. CONCLUSION AND FUTURE SCOPE

The greatest benefit of this traffic light controller is accident free transportation routes at junction of many roads. This controller allows the traffic to move smooth without any disturbance between road junctions. All this programming is done in Xilinx Vivado Tool. We had done synthesis and analysis of the project in Vivado.

We can make improvements to this system by solar power supply and some other improvements for pedestrian crossing and help assist for physically handicapped people and for senior citizens while crossing road.

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