Design of a Fully-Differential CMOS OTA Folded-Cascode for $\Sigma\Delta$ Modulation

F. Sandoval-Ibarra¹, V. H. Arzate-Palma², S. D. Cárdenas-Castellón³

¹*Cinvestav-Guadalajara Unit, Av. Del Bosque 1145, 45017 Zapopan, Mexico*

Abstract— In this paper, the design and experimental results of a fully-differential folded-cascode operational amplifier of transconductance (OTA) is presented. This active circuit is for the use in a $\Sigma\Delta$ low-pass modulator. The structure of the OTA is for obtaining a transition frequency of 1.0GHz. From the circuit synthesis, the OTA can handle the signals with the peak-to-peak amplitude of 300mV, and consumes 1.5mA from 1.2V supply. The OTA is fabricated in 130nm standard CMOS technology.

Keywords—Active circuits, analog integrated circuits, circuit synthesis, circuits analysis, CMOS integrated circuits, operational amplifiers.

I. INTRODUCTION

A sigma delta ($\Sigma\Delta$) modulator is a linear encoder (typically one bit) that shape the quantization noise, and transforms an analog signal into an oversampled frame of bits. The $\Sigma\Delta$ modulator is a feedback system with a quantizer that operates in discrete time. Its name is because it adds (sigma) the difference (delta) between the input signal and the output response. A first-order modulator includes three basic blocks: a quantizer, a Digital-to-Analog Converter (DAC), and a filter. Although the modulator is a non-linear system, a linear model approximates it in order to understand its basic behavior. For the purposes of circuit analysis, the quantizer is usually modeled as a white noise error source $E_Q(s)$. The DAC, on the other hand, is modeled as a unity gain stage and the modulator response, in the Laplace domain, is given by

$$Y(s) = X(s)STF(s) + E_Q(s)NTF(s) \quad (1)$$

Where $X(s)$ represents the input signal. Note that the input signal and the quantization noise are associated with the signal transfer function $STF(s)$ and the noise transfer function $NTF(s)$, respectively [1]. As seen in (1), it is desirable that $H(s)$ be a high-gain function so that both properties $STF(s)=1$ and $NTF(s)=0$ are fulfilled:

$$Y(s) = X(s) \frac{H(s)}{1 + H(s)} \left[1 + \frac{E_Q}{X(s)H(s)} \right] \quad (2)$$

Where the expected response is a signal without quantization noise. In practice, the quantization error is present when converting the analog signal to the digital domain. The quantization error is defined as $e_Q = x_Q - x$, where x_Q has finite precision and is a multiple of the quantization step, while x is the input signal with infinite precision. Now, to minimize the effect of noise on the bandwidth of interest, the design focus should be on the loop filter. An option to implement the filter is an integrator circuit, and to establish its design specifications, in this work it is of interest to design a Continuous-Time (CT) Low-Pass (LP) modulator in a standard 130nm CMOS technology, N-well, $\pm 0.6V$. Consequently, it is of interest to attend to two unwanted phenomena: the effect of parasitic capacitances, and the effect due to the channel length. Parasitic limit the transition frequency f_T of the transistor:

$$f_T = \frac{g_m}{2\pi C_{gs}} = \frac{3\mu}{4\pi} \cdot \frac{V_{DS,sat}}{L^2} \quad (3)$$

Where, in order to increase the frequency f_T the saturation voltage $V_{DS,sat}$ must be increased or alternatively the channel length L reduced [2]. The first option is not the best one because modifies the operating point, while the second one has much more implications. In nanometric technologies, it is known that by reducing the value of L , the threshold voltage V_{TH} increases. This effect is called the Reverse Short Channel Effect (RSCE), which is widely described in [3]. In 130nm CMOS technology, this effect must be considered when designing any active circuit. Furthermore, if L is small the voltage V_{TH} increases and then the frequency f_T will not be the expected one. Therefore, (3) is valid only for large-channel technologies. So, to determine the architecture of the loop filter, and taking into account the effect of the L value, in this work the main objective focuses on designing an OTA, so that the modulator noise E_Q be highly eliminated.

This work is organized as follows. Section II presents the integrator and a review of proposals available in the literature.

The design and simulation of the OTA is described in section III where three alternatives are discussed, a single-ended NMOS- and PMOS-input topology and a fully differential PMOS-input OTA. Section IV offers a discussion of preliminary results of the OTA. The conclusions are given in section V.

II. THE INTEGRATOR CIRCUIT

The simplest of integrators is the so-called $g_m C$ integrator consisting of an OTA and a C_0 capacitor. It is common practice to assume that the OTA can be modeled as an ideal current source, in parallel with an infinite output resistance r_{out} . In a real OTA, r_{out} is finite and there is a parasitic capacitance C_p at the output node (see Fig. 1). Thus, the transfer function of the integrator is given by

$$\frac{v_{out}(s)}{v_{in}(s)} = - \frac{g_m}{\frac{1}{r_{out}} + s(C_p + C_0)} \quad (4)$$

Where the useful performance range is determined by the time constant $\tau_0 = r_{out}(C_p + C_0)$. That is, the integration function occurs when $|s| > 1/\tau_0$:

$$\frac{v_{out}(s)}{v_{in}(s)} \approx - \frac{g_m}{sC_p} \quad (5)$$

with $C_0 \gg C_p$, and that is the result commonly reported in the literature [5]-[7], where the positive input port is usually ground connected. The basic OTA is the differential pair, which provides a gain slightly less than 40dB (see Fig. 1) with r_{out} approximately 80k Ω . Optimizing the design for higher gain can be achieved up to 46 dB, but the differential pair is not a high gain circuit [8]. One option to increase the gain is by using two amplification stages (see Fig. 2). Traditionally, this OTA is said to be unstable, and therefore requires a compensation stage [9]-[13]. In practice, that statement is true as long as the output stage is a simple amplifier. When the output stage is an amplifier with source degeneration, it does not require compensation because the phase function satisfies the Nyquist criterion [14]. Their disadvantage, in addition to power consumption, is lower bandwidth. Thus, an option for high gain and higher bandwidth, are the telescopic OTA and the folded cascode design [15].

Fig. 1 Basic OTA open loop gain.

Fig. 2 Two stage OTA open loop gain.

Of both proposals, the folded cascode OTA requires fewer transistors, which means reducing the space of design variables. The analog design, on the other hand, is custom design, meaning that basic processing blocks are designed to meet the minimum performance requirements of the system under design. Regarding the sigma-delta modulator, it is of interest in this contribution to design an OTA with a transition frequency $f_T > 100\text{MHz}$ with $C_L = 1\text{pF}$. In practice, to achieve low power consumption and control the transition frequency f_T , the option is to use nanometer technologies. In this contribution, the facilities of a standard manufacturing process 130nm CMOS, 1.2V, are used.

TABLE II
TRANSISTOR SIZES, NMOS-INPUT FOLDED-CASCODE OTA

Transistor	g_m/I_D	W
$W_{1,2}$	12.56	28 μm
$W_{3,4}$	6.0	28 μm
$W_{5,6}$	20.0	45 μm
$W_{7,8}$	6.0	2 μm
$W_{9,10}$	6.0	1.61 μm
W_0	6.0	3.23 μm

C. Fully-differential PMOS-input folded-cascode

Figure 5 shows the topology to be designed, where $I_b=300\mu\text{A}$ was proposed. Because the OTA is fully differential, we need a circuit to keep the common mode voltage at 50% of the supply voltage. This CMFB circuit senses the output signals and feeds them back to the OTA to keep the common-mode voltage stable. The selected CMFB circuit consists of a differential difference amplifier. At the conclusion of the analysis to design each transistor, and to verify the expected performance of the OTA in simulation, the layout of the OTA is made. In this work, the integration area is optimized, and both the common centroid technique and that of interdigitated transistors were used. Three levels of metal were our choice to reduce parasitic resistances, poly connections were minimized, and to reduce the number of parasitic capacitances metal-metal and metal-poly overlaps were avoided as much as possible [15]. The design also considers the non-uniform concentration of the N-well. To avoid unwanted increases in threshold voltage V_{TH} [21], the transistors were moved away from the edge of the well. Additionally, dummy transistors were included to minimize variations in OTA performance due to mismatch [22]. In the Fig. 6, the resulting layout is shown. It should be noted that the OTA shown in Fig. 5 does not include the CMFB circuit and does not include a boost stage to increase the output impedance. Both circuits are included in the final layout.

IV. PRELIMINARY RESULTS

Table 3 shows simulation results, schematic vs layout. In practice, each interconnection is a parasitic resistance r_p , and each overlap of conductive materials is a parasitic C_p capacitance. Each C_p contributes to decrease the bandwidth of the OTA, and each r_p causes slight voltage changes at the nodes and affects the operating point. The common mode voltage, on the other hand, exhibited a change that may be due to parasitic resistances [15].

Then, the OTA was configured as a g_mC integrator (see figure 7), with a capacitor $C=7.5\text{pF}$. The input signal is a square wave with amplitude $V_{pp}=40\text{mV}$ and frequency $f=100\text{MHz}$. The response corresponds to a triangular signal as expected and includes an offset voltage of -6mV . Harmonic distortion was also simulated, and for this, the OTA was configured to have unity gain. Three amplitudes were selected for a 100 MHz sine signal. For 40mV, 140mV and 150 mV the third harmonic was $75\mu\text{V}$, 7.78mV, and 10.12mV or equivalently $\text{HD3}=0.18\%$, 5.3% and 6.75%, respectively. From this result, it is concluded that, from simulation, the OTA presents an output swing of 300mV_{pp} with a distortion of 6.75%. Figure 8 shows, at the top, the test chip manufactured in 130nm CMOS technology.

Fig. 5 PMOS-input fully-differential folded-cascode OTA.

Fig. 6 Layout of the OTA.

TABLE III
COMPARISON OF SIMULATION RESULTS.

Parameter	Schematic	Post-layout	Error (%)
A_{DC} (dB)	60.4	59.9	1.6
f_T (GHz)	1.02	0.99	2.2
MF (°)	68.7	64	6.8
C_L (pF)	0.75	0.75	0
g_m (mS)	5.05	4.99	1.01
r_{out} (k Ω)	207.4	197.8	4.6
P (mW)	1.91	1.8192	4.6

The same figure shows the OTA's response (configured as integrator) to a square input signal. The answer, which is as expected, is just an example of the test plan designed for the OTA. At this time, future work includes incorporating some improvements to the OTA. One of them is to increase the open-loop gain by means of a programmable arrangement, so that the OTA is useful for those applications where a large transition frequency is not required. Additionally, it is important to note the following. Transconductance is the ability of the OTA to convert a voltage signal into a current signal. Ideally, the conversion is expected to be directly proportional to g_m , and implies that the OTA is a linear circuit. Linearity, on the other hand, is of interest to increase because the integrator will adequately perform its function, and the modulation scheme in general will operate satisfactorily.

V. CONCLUSIONS

Several topics concerning folded-cascode OTA design were analyzed. The boost stage is an excellent option to increase the output impedance between some tradeoffs, such as silicon area and power consumption. We also analyze several OTAs by including both NMOS- and PMOS-input transistors as well as single-ended proposals. Then, we redesign the folded-cascode OTA and our choice is a fully-differential one, a PMOS-input proposal actually. The layout design takes into account the non-uniform concentration of the N-well. To avoid unwanted increases in threshold voltage V_{TH} , transistors are moved away from the edge of the well. Dummy transistors are included to minimize variations in the OTA performance due to mismatch. From experimental results, the OTA can handle signals with peak-to-peak amplitude of 300mV, and consumes 1.5mA from 1.2V supply. The transition frequency is 0.99GHz, 59.9dB open loop gain and the OTA presents an output swing of 300mV_{pp} with a distortion of 6.75%. The OTA is fabricated in 130nm standard CMOS technology, N-well, $\pm 0.6V$.

Fig. 7 Simulation result of the OTA-based integrator.

Fig. 8 Top view of the test chip (above) and experimental response of the OTA-based integrator (below) to square input signal.

Acknowledgments

Two authors (VHAP and SDCC) wish to thank Consejo Nacional de Ciencia y Tecnología (CONACyT), Mexico, for the scholarship received. The authors thank MOSIS for the manufacturing facilities, and MC Rickey Castillo-Valenzuela for his contributions to this research and for the tests carried out. This work was possible thanks to CONACyT's support for the project No. 169660.

International Journal of Emerging Technology and Advanced Engineering

Website: www.ijetae.com (ISSN 2250-2459, ISO 9001:2008 Certified Journal, Volume 10, Issue 11, November 2020)

REFERENCES

- [1] Bolatkale M., Breems L. J., Rutten R. and Makinwa K. A. A. 2011. A 4GHz CT $\Delta\Sigma$ ADC with 70dB DR and -74dBFS THD in 125MHz BW, Journal of Solid-State Circuits, 46, (Dec. 2011), 2857-2868.
- [2] Baker, R. J. 2010 CMOS: Circuit design, layout, and simulation, IEEE Press.
- [3] El-Kareh, B. 2009 Silicon devices and process integration: Deep submicron and nano-scale technologies, Springer Science Business Media.
- [4] Vasilevski M., Aboushady H., Louerat M. M. 2009. Automatic Model Refinement of GmC Integrators for High-Level Simulation of Continuous-Time Sigma-Delta Modulators, In Proceedings of IEEE International Symposium on Circuits and Systems
- [5] Fang X., Srinivasan V., Wills J., Granacki J., LaCoss J., Choma J. 2009. CMOS 12 bits 50kS/s Micropower SAR and Dual-Slope Hybrid ADC, In Proceedings of the 52nd IEEE International Midwest Symposium on Circuits and Systems
- [6] Chen-Yan C., Jiang Y., Sai-Weng S., Seng-Pan U. and Martins R. P. 2011. A Passive Excess-Loop-Delay Compensation Technique for Gm-C Based Continuous-Time $\Sigma\Delta$ Modulators, in Proceeding of the IEEE 54th International Midwest Symposium on Circuits and Systems
- [7] Lee Ch., Jeon T., Jang M., Park S., Kim J., Lim J., Jong-Hyun A., Huh Y., Chae Y. 2020. IEEE Journal of Solid-State Circuits, 55 (Nov. 2020), 2889-2901.
- [8] Lopez-Martin, A., Baswa, S., Ramirez-Angulo, J., & Carvajal, R. 2005. Low-Voltage Super class AB CMOS OTA cells with very high slew rate and power efficiency. IEEE J. Solid-State Circuits, 40 (May 2005), 1068-1077.
- [9] Moallemi S. and Jannesari A. 2012. A New Architecture For Two-Stage OTA with No-Miller Capacitor Compensation, In Proceedings of the IEEE International Conference on Circuits and Systems
- [10] De Carvalho Ferreira L. H. and Pimenta T. C. 2004. AN ULTRA LOW-VOLTAGE ULTRA LOW POWER RAIL-TO-RAIL CMOS OTA MILLER, In Proceeding of the IEEE Asia-Pacific Conference on Circuits and Systems
- [11] Ferreira L. H. C., Pimenta T. C. and Moreno R. L. 2007. An Ultra-Low-Voltage Ultra-Low-Power CMOS Miller OTA With Rail-to-Rail Input/Output Swing, IEEE Transactions on Circuits and Systems—II: Express Briefs, 54, (Oct. 2007), 883-887.
- [12] Johns D. and Martin K. 1997 Analog integrated circuits design. John Wiley & Sons.
- [13] Gregorian R. and Temes G. C. 1990 Analog MOS integrated circuits for signal processing. John Wiley & Sons.
- [14] Sandoval-Ibarra F., Ortega-Cisneros S., “El amplificador Miller CMOS y sus consideraciones de diseño”, XVI SENIE, 2020, in press
- [15] Castillo-Valenzuela R., 2017 Diseño de un OTA para un modulador Sigma-Delta tiempo-continuo en tecnología CMOS 130nm, Master Thesis, Cinvestav-Guadalajara
- [16] Saatlo A. N., Ozoguz S. and Minaei S. 2015. Applications of a CMOS Current Squaring Circuit in Analog Signal Processing, In Proceedings of the 38th International Conference on Telecommunications and Signal Processing
- [17] Tsividis Y. and Antoniadis D.A. 1982. A Multiproject Chip Approach to the Teaching of Analog MOS LSI and VLSI, IEEE Transactions on Education, 25, (May 1982), pp. 48-53.
- [18] Cárdenas-Castellón S. D., 2020 Diseño de un filtro Pasa-Banda CMOS, programable en el rango audible, Master Thesis, Cinvestav-Guadalajara
- [19] Dammak D., Bensalem S., Zouari S. and Loulou M. 2008. Design of Folded Cascode OTA in Different Regions of Operation Through g_m/I_D Methodology. International Journal of Electrical and Electronics Engineering, (Dec. 2008) 178-183.
- [20] Arzate-Palma V. H. 2020 Diseño de bloques básicos de procesamiento para el control de ganancia, y ancho de banda de un filtro CMOS Pasa-Banda, Master Thesis, Cinvestav-Guadalajara
- [21] Tsividis, Y., and McAndrew, C. 2012 The MOS transistor. Oxford University Press.
- [22] Maloberti, F., 2001 Analog design for CMOS VLSI systems. Kluwer Academic.