Nyquist Model based Thermal Noise Analysis—From Passive Components to CMOS Circuits

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Abstract—The analysis of thermal noise in network components that have resistive properties is presented. Noise analysis, based on the Nyquist model, is calculated as the rms (voltage or current equivalent) noise generated by a transimpedance, which is the concept used by general-purpose circuit simulators like Spice. It shows how this concept is used and understood in RC circuits, and how to evaluate its effect in analog circuits, particularly in the design of CMOS integrated circuits. It is shown that the magnitude of the noise generated by a transistor is not of interest, but the net effect of all sources of thermal noise in circuits and systems, fundamentally, when the miniaturization of the transistor implies reducing the value of the supply voltages. The ultimate purpose of this contribution is to highlight the importance of noise analysis using fundamentals of circuit theory and identify the variables under the designer's control to minimize their effect on the performance of the circuits under development.

Keywords—Analog circuits, circuits theory, CMOS integrated circuits, network analysis, passive components, Spice, thermal noise, teaching.

I. INTRODUCTION

In 1928, H. Nyquist published a paper where electron fluctuations in a conductive path were explained by using thermodynamics theory [1]. Those electron fluctuations are currently known as thermal noise. Since then thermal noise has been measured to know how much this unwanted effect affects the response of an electronic system. A system under analysis, in general, is characterized by ports where one of them is used to apply an *input* and the other one is to measure an *output*, i.e. the system response. How the *output* depends on the system *function*, which correctly works once the *input* is applied (see Fig. 1a). In that sense, the interest of analyzing an electronic system is because thermal noise does not depend on the *input* (hereafter called the input signal). Thermal noise, measured as an equivalent electronic signal at the *output* port, is not zero. That is why thermal noise must be minimized in order to enhance the ratio defined by the magnitude of the input signal over the magnitude of thermal noise. The latter is a Figure-Of-Merit (FOM) called Signal-to-Noise Ratio, SNR. The importance of thermal noise is because it defines by itself an open problem in several application areas.

For instance, an electronic system for data acquisition consists of n -input ports ($n=1, 2, 3\dots$) and a *function* based on a unique Analog-to-Digital Converter (ADC), where multiplexing techniques are commonly used to save both power consumption and integration area [2]. In practice, that description just highlights the *input scenario* because the *function* currently consists of m -functions ($m=1, 2, 3\dots$) that means there are several sources of thermal noise limiting the performance of the electronic system. In addition, mobile communication devices impose the need of ultra-wide band designs that results actually in wide bandwidth system design with Signal-to-Power Ratio (SPR) below background noise. For those devices, the *function* is supported in the operation of a Local Oscillator (LO). In other words, communication systems impose the design of LOs with reduced noise and low power consumption [3]. Even more, silicon based transducers for translating physical variables into electrical ones not only requires suppress $1/f$ noise, but the remaining white noise due both the conditioning circuitry and the transducer output impedance [4]. White noise is a signal with a constant power spectral density with respect to frequency, implying that it is made up of many frequency components. Since thermal noise shares this characteristic, it is referred as white noise [5].

Fig. 1. Two-port network (a) and multi-port network (b). Each function is a noisy electronic circuit.

Today, many electronic devices include not only n -inputs and m -functions, but k -outputs making thermal noise analysis a mandatory task (see Fig. 1b). Therefore, how thermal noise must be faced in order to understand its unwanted effect on an electronic system is the purpose of this paper. However, for education purposes and taking into account that thermal noise reduction must be a skill of novice and expert designers, this paper deals with some practical methods for analyzing the thermal noise effect in electronic circuits.

The methods are applicable to electronic circuits containing passive components and/or active components with emphasis on CMOS technology. The purpose is twofold. Firstly, noise analysis is based on basics of circuit theory, and secondly the designer must know how noise analysis is carried out when simulation tools are used. In this paper, Tanner-Tools and Cadence are our choice. Basics on thermal noise for analyzing RC circuits are presented in Section II, where several comparison results based on Spice simulations are also given. The idea behind comparison results is to introduce few statements to clearly understand not only how Spice computes noise effect at circuit level, but also how simulation statements must be used in order to corroborate results based on hand-made circuits analysis. Section III shows how this knowledge allows to the designer be able to use noise analysis to assess noise effect at CMOS system level. Conclusions are presented in Section IV, where some design hints are described/validated by analyzing some active circuits.

II. BASICS ON THERMAL NOISE

H. Nyquist published the modelling of the electromotive force E , due to the thermal agitation in a conductor of resistance R , in 1928:

$$E = 4kTR, \quad (1)$$

where $k (=1.38 \times 10^{-23} J/K)$ is the Boltzmann constant, T the conductor temperature [1], and $[E]=V^2/Hz$. Today the electromotive force is commonly known as the Normalized Noise Power (NNP), $V_{n,rms}^2$, and its root square is the so-called voltage spectral density (or rms noise voltage):

$$V_{n,rms} = \sqrt{4kTR}, \quad (2)$$

Where $[V_{n,rms}]=V/\sqrt{Hz}$ [4]. The 1st order R_2C_1 Low-Pass filter shown in Fig. 2a is used in this paper to show how thermal noise affects the output of an electronic circuit. Thermal noise generation is represented by adding a thermal noise voltage source in series with a noise-less resistor. So, firstly, if room temperature conditions ($T=300K$) are assumed and $R_2=8.71k\Omega$, the rms noise voltage is $V_{n,R2,rms}=12nV/\sqrt{Hz}$ (see Fig. 2b). To calculate how noise affects the circuit response, a short circuit (as shown in Fig. 2c) replace the input. Equation (3) shows the voltage response, from the noise source to the output node, where the constant time $\tau_{12}=R_2C_1$ is related with the corner frequency of the circuit, $\omega_{12}=1/\tau_{12}$. Note that the noise effect on the circuit response is low-pass type, i.e. noise effect varies with frequency because of the R_2C_1 network.

$$V_{n,out} = V_{n,rms} \frac{\frac{1}{sC_1}}{R_2 + \frac{1}{sC_1}} = V_{n,rms} \frac{1}{1 + sR_2C_1} \quad (3)$$

Then, if capacitor $C_1=1.0pf$ is assumed the corner frequency is $f_{12}=18.52MHz$, where the equivalence $2\pi f=\omega$ was used. At lower frequencies, where the frequency response is flat, resistor contributes a total of $12nV/\sqrt{Hz}$ at the circuit's output. In order to minimize the noise generation low resistance components must be used. Note that if resistor R is scaled-down by a factor α , capacitor C has to be scaled-up by the same factor, so the pole value remains unchanged. This design procedure is the so-called impedance denormalization [3].

Fig. 2. RC circuit under study (a), equivalent lumped circuit to compute how noise generation affects the response of the circuit (b). Equivalent noisy circuit under analysis (c), and Norton circuit to compute the circuit's transimpedance (d).

A. Noise analysis with SPICE

It is based on the complex AC nodal voltages, which in turn are based on the DC operating point. What does this sentence means? A source noise is firstly assumed to be not statistically correlated to other noise sources, and the total output noise voltage is the rms sum of the individual noise contributions:

$$V_{n,out} = \sqrt{V_{n,out,R_1}^2 + V_{n,out,R_2}^2 + \dots + V_{n,out,R_k}^2}, \quad (4)$$

here $V_{n,out,R_j}^2 = |Z_j I_{n,j}|^2$, Z_j is the equivalent transimpedance between noise source and the output node, $I_{n,j} = V_{n,j}/R_j$ is the equivalent current due to thermal noise and $j=1,2,3,\dots,k$. Therefore, the voltage response (see Fig. 2d) is given by (5). From this result, the reader easily identifies the equivalent transimpedance of the circuit, which varies also with frequency. The magnitude function is then given by (6), where, as mentioned, the corner frequency is $f_{12}=18.52MHz$.

$$V_{n,out} = I_{n,R_2,rms} \frac{\frac{R_2}{sC_1}}{R_2 + \frac{I}{sC_1}} = I_{n,R_2,rms} \frac{R_2}{I + sR_2C_1} \quad (5)$$

$$|Z_{R_2}| = \frac{V_{n,out}}{I_{n,R_2,rms}} = \frac{R_2}{\sqrt{1 + \left(\frac{f}{f_{12}}\right)^2}} \quad (6)$$

In order to analyse the circuit response, the simulation result shown in Fig. 3 were obtained. The output file includes as much noise parameters as the designer defines in the circuit script.

Fig. 3. Frequency response of the RC circuit.

With the help of the statement `.print dn(R2)` all about noise data is printed and plotted, i.e. **R2** is the device under analysis. The transimpedance plot obtained from Tspice [4] is shown in Fig. 3, where both labels and cursors were added to highlight specific values. The plot describes how the transimpedance varies with frequency. Now, let us suppose we add another resistive component to the Low-Pass circuit as shown in Fig. 4a, where $R_2=R_3$. The total output noise voltage is given by

$$V_{n,out} = \sqrt{V_{n,out,R_2}^2 + V_{n,out,R_3}^2}, \quad (7)$$

Where the voltage response from each voltage noise source (see Fig. 4b and Fig. 4d) to the output node is

$$V_{n,out,R_2} = V_{n,rms,R_2} \frac{I}{\frac{R_2}{R_3}(I + sR_2C_1) + I}, \quad (8)$$

and

$$V_{n,out,R_3} = V_{n,rms,R_3} \frac{I}{\frac{R_3}{R_2}(I + sR_3C_1) + I}, \quad (9)$$

due to R_2 and R_3 , respectively. Taking into account that $\tau_{12}=\tau_{13}$ the total output noise is as eq. (9) shows, where, at low frequencies, all resistors contribute a total $V_{n,rms,R_2}/\sqrt{2}=8.48nV/\sqrt{Hz}$ at the circuit's response.

Fig. 4. RC circuit under study based on two resistive components, $R_2=R_3$.

Now, with the help of the statement `.print noise onoise`, the total output noise is printed and plotted. The later, obtained from Tspice, is shown in Fig. 5, where labels and cursors highlight useful values. One of them is the corner frequency, $f'_{12}=37.0MHz$, which can be verified by analysing (10). Note that the denominator function is $(2+s\tau_{12})$, or equivalently $2(I+0.5s\tau_{12})$. That is why $f'_{12}=2f_{12}$. This result is an unwanted one, i.e. the noise effect on the circuit's output is lower that the simple RC circuit, but largest bandwidth increases the noise effect on the circuit's performance.

$$V_{n,out} = \frac{\sqrt{V_{n,rms,R_2}^2 + V_{n,rms,R_3}^2}}{(I + s\tau_{12}) + I} = \frac{\sqrt{2} V_{n,rms,R_2}}{(I + s\tau_{12}) + I}, \quad (10)$$

A common practice to minimize noise is by attending narrowband applications. On the other hand, by using CADENCE the output file includes the equivalent complex transimpedance as shown in Table I. Values shown in Table I correspond to the complex function obtained from analysing the lumped circuit shown in Fig. 4c and Fig. 3e when $s \rightarrow i\omega$. The equivalent transimpedance is shown in (11).

Note that to obtain the transimpedance due the noise generated by R_2 and R_3 , both circuit (see Fig. 4c and Fig. 4e) are equivalent so that (11) models both networks. The magnitude response of $|Z_{R_3}(i\omega)|$ is shown in Fig. 5.

$$Z_{R_3}(i\omega) = \frac{\frac{R_3}{2}}{1 + i\frac{\omega}{2\omega_{l2}}} = \frac{R_3}{2} \cdot \frac{1 - i\frac{\omega}{2\omega_{l2}}}{1 + \left(\frac{\omega}{2\omega_{l2}}\right)^2} \quad (11)$$

Fig. 5. Tspice output noise due R_2 and R_3 . In the frequency domain, noise magnitude is as theory predicts.

TABLE I
COMPLEX TRANSIMPEDANCE, WHEN CONSIDERING R_3

f (Hz)	$Re(Z_{R_3})$	$Im(Z_{R_3})$
1.00E+00	4.36E+03	-1.1917E-04
1.00E+01	4.35E+03	-1.1917E-03
1.00E+02	4.35E+03	-1.1917E-02
1.00E+03	4.35E+03	-1.1917E-01
1.00E+04	4.35E+03	-1.1917E+00
1.00E+05	4.35E+03	-1.1917E+01
1.00E+06	4.35E+03	-1.1908E+02
2.00E+06	4.34E+03	-2.3762E+02
4.00E+06	4.30E+03	-4.7103E+02
6.00E+06	4.24E+03	-6.9624E+02
8.00E+06	4.16E+03	-9.0974E+02
1.00E+07	4.05E+03	-1.1087E+03
1.50E+07	3.73E+03	-1.5298E+03
2.00E+07	3.35E+03	-1.8340E+03
2.50E+07	2.97E+03	-2.0295E+03
3.00E+07	2.60E+03	-2.1358E+03
4.00E+07	1.98E+03	-2.1686E+03
6.00E+07	1.18E+03	-1.9348E+03
8.00E+07	7.52E+02	-1.6460E+03
1.00E+08	5.13E+02	-1.4040E+03

B. Noise in MOS transistors

The model for computing thermal noise in most of the literature and circuit simulators as Spice is given by (12), where $[I_{n,rms}] = A/\sqrt{Hz}$, g_m is the transistor's transconductance at the operating point [2], [5], and it is valid for operation in the saturation region. This noise is commonly modelled by adding a current source in parallel with the MOS transistor.

$$I_{n,rms} = \sqrt{4kT \left(\frac{2g_m}{3} \right)}, \quad (12)$$

An equivalent model to compute the rms voltage is given by

$$V_{n,rms} = \sqrt{4kT \left(\frac{2}{3g_m} \right)}, \quad (13)$$

This result models a noise voltage that is connected at the gate of a hypothetical noiseless MOS transistor, to produce an equivalent amount of noise current [2], [6], [7]. Both noise sources depend on the dimensions, bias conditions, and temperature of the device. In practice, although the calculation of noise in a MOS transistor is important, of greater interest is to evaluate its effect in MOS circuits. Therefore, the purpose of this contribution is to show the sizing of a basic CMOS cell, which by itself generates noise and affects the performance of the cell itself.

III. THERMAL NOISE IN CMOS CIRCUITS

In order to show how thermal noise affects the output of MOS circuits, let us introduce the voltage divider shown in the Fig. 6, where $V_{DD} = -V_{SS}$. Note that $|V_{GS}| = |V_{DS}|$ for all transistors in the active proposal, and the condition for saturation $|V_{DS}| > |V_{GS}| - |V_T|$ is satisfied. Therefore, the common drain current I_{BIAS} is computed by any of the following equivalent models [8]:

$$\frac{V_{DD} - V_{REF,1}}{R_1} = \frac{V_{REF,1} - V_{REF,2}}{R_2} = \frac{V_{REF,2} - V_{SS}}{R_3}, \quad (14)$$

where $V_{REF,1}$ and $V_{REF,2}$ are voltages usually specified, and R_j ($j=1, 2, 3$) is the equivalent resistance of each diode-connected transistor, i.e. the transconductance, $g_i = 1/R_i$. Because the transistors drive the same current, the eq. (14) is used to find the resistive ratios of the circuit:

$$\frac{R_2}{R_3} = \frac{V_{REF,1} - V_{REF,2}}{V_{REF,2} - V_{SS}}, \quad (15)$$

$$\frac{R_1}{R_3} = \frac{V_{DD} - V_{REF,1}}{V_{REF,2} - V_{SS}}$$

where these design models assume that each diode-connected transistor behaves as a lumped resistor, which means that the current is independent of the drain-to-source voltage, V_{DS} :

$$I_{BIAS} = |I_{D,j}| = \left| KP_j \left(\frac{W}{L} \right)_j (|V_{GS,j}| - |V_{T,j}|)^2 \right|, \quad (16)$$

where $|V_{T,j}|$ and $|KP_j|$ are the threshold voltage and the conductivity factor of the transistor, respectively [6], [7]; both parameters are provided by the manufacturer.

Fig. 6. Passive voltage divider and its active equivalent circuit, where $I_{DD}=I_{BIAS}$.

According to the simulation model used in this work, and taking into account that each bulk-to-source voltage, V_{BS} , is zero, some design conditions result, where $|V_{T,1}|=|V_{T,2}|$, $|V_{T,2}| \neq |V_{T,3}|$, $|KP_1|=|KP_2|$, $|KP_2| \neq |KP_3|$ and $|KP_3| > |KP_2|$. Since the MOS transistor is biased in its saturation region, the equivalent transconductance of each transistor is the derivative evaluated at the bias point:

$$g_{m,j} = \frac{d|I_{D,j}|}{d|V_{GS,j}|} = 2|KP_j| \left(\frac{W}{L} \right)_j (|V_{GS,j}| - |V_{T,j}|), \quad (17)$$

where the equivalent resistance of each transistor is $R_j = 1/g_{m,j}$. Then (15) can be written as shown in (18), where $L=L_1=L_2=L_3$, $|V_{GS,3}|=|V_{REF,1}-V_{DD}|$, $|V_{GS,2}|=|V_{REF,2}-V_{REF,1}|$, and $|V_{GS,1}|=|V_{REF,2}-V_{SS}|$.

$$\frac{|KP_3| \left(\frac{W}{L} \right)_3 (|V_{GS,3}| - |V_{T,3}|)}{|KP_2| \left(\frac{W}{L} \right)_2 (|V_{GS,2}| - |V_{T,2}|)} = \frac{V_{REF,1} - V_{REF,2}}{V_{REF,2} - V_{SS}}, \quad (18)$$

$$\frac{|KP_3| \left(\frac{W}{L} \right)_3 (|V_{GS,3}| - |V_{T,3}|)}{|KP_1| \left(\frac{W}{L} \right)_1 (|V_{GS,1}| - |V_{T,1}|)} = \frac{V_{DD} - V_{REF,1}}{V_{REF,2} - V_{SS}}$$

As an example, let us propose $L=1.5\mu m$, $V_{DD}=2.5V$, $V_{REF,1}=1/4(V_{DD}-V_{SS})=1.25V$ and $V_{REF,2}=1/2(V_{DD}-V_{SS})=0V$. Using (18) the following design model results

$$W_{p1} = 36.0844W_{n3}, \quad (19)$$

where $W_{p1}=W_{p2}$. Then, if $W_{n3}=21.0\mu m$ is assumed the channel width is $W_{p1}=757.77\mu m$ (the same is true for W_{p2}).

Unfortunately, that physical dimension cannot be manufactured because of the resolution of photolithography techniques. By taking into account the design rules used in this work, the size of any transistor must be fitted to a number given by $n_j\lambda$, with $\lambda=0.3\mu m$ and n_j an integer; note that $n_3=70$ for the NMOS transistor. Then, the manufacturable size of both PMOS transistor is one of the following values $n_{1,2}=\{2526, 2525\}$, where the first one allows us to obtain the round up value while the second one is the round down value. In practice, the size of both PMOS transistors is deduced from a Tspice-based Design Of Experiments (DOE), where the variables under control are W_{p1} and W_{p2} , and the performance under study are the DC results including reference voltages. Table II shows simulation results, where these values warranty that transistors work in saturation region [9]. Note that $V_{REF,1}$ and $V_{REF,2}$ present an offset of $67mV$ and $135mV$, respectively. In order to explain the reason of that variation, we must highlight that rounding introduces a round-off error in the expected result. Another source of error is that due to the Transistor Simulation Model (TSM). In this work, for simulation purposes we are using the LEVEL=49 TSM, while for hand-made design the so-called square law (also called LEVEL-1 model) was used, see (15). In order to minimize the design error, the square law was used to translate a resistive ratio into a transconductance ratio (see (17)), and then obtain a channel width ratio. This design procedure allows us to calculate the channel width of each transistor. However, we must take into account that the layout design introduces another source of error.

In practice, the effect of the errors due rounding is reduced by avoiding minimum size, but parasitic increases. In the following $W_{p1}=757.8\mu m$, $W_{p2}=757.8\mu m$ and $W_{n3}=21\mu m$ is the authors choice.

TABLE II
SPICE-BASED DC RESULTS AS A FUNCTION OF THE TRANSISTORS SIZING

W_{n3}	W_{p2}	W_{p1}	$V_{REF,1}$	$-V_{REF,2}$	I_{BIAS} (A)
21 μm	757.50 μm	757.50 μm	1.1824V	0.1351V	159mV
		757.80 μm	1.1825V	0.1350V	159mV
	757.80 μm	757.50 μm	1.1824V	0.1350V	159mV
		757.80 μm	1.1825V	0.1349V	159mV

Figure 7 shows the noise generated by each transistor [10], as rms current sources, being of interest to know its effect on the two nodes of interest. Therefore, the analysis of the PPN branch is aimed at obtaining models that allow quantifying the effect of reflected noise in $V_{n,x,out}$ and $V_{n,y,out}$. Applying KCL, and after a bit of algebra, it can be verified that the noise reflected in the nodes of interest is given by

$$v_{nx,out} = \frac{-Ag_{mp1}V_{n,p1} + (A-1)g_{mp2}V_{n,p2} - g_{mn3}V_{n,n3}}{(2A-1)(g_{mp1} + g_{ds,p1})} \quad (20)$$

$$v_{ny,out} = \frac{(B-1)g_{mp2}V_{n,p2} + Bg_{mn3}V_{n,n3} + g_{mp1}V_{n,p1}}{(g_{mp2} + g_{ds,p2})(1-B) - B(g_{mn3} + g_{ds,n3})} \quad (21)$$

where

$$A = \frac{g_{mp2} + g_{ds,p2} + g_{mn3} + g_{ds,n3}}{g_{mp2} + g_{ds,p2}} \quad (22)$$

$$B = \frac{g_{mp1} + g_{ds,p1} + g_{mp2} + g_{ds,p2}}{g_{mp2} + g_{ds,p2}} \quad (23)$$

here the equivalence $I_n = g_m V_n$ was used to obtain a representation of the noise equivalent in voltage. Note that (20)-(23) have not been simplified because the purpose is to show the contribution of each noise source and the small signal parameters. In practice, because the design method is based on equations LEVEL=1, the sizing has an implicit error at the operation point, but transistors still operate in saturation. It must be noted that sizing of transistors grows (see Table III) as the operation point moves away from the desired value; this variation does not modify the expected operation of all transistors.

The last nine lines correspond to the small signal parameters for each transistor obtained from SPICE simulations, and the first three lines are analytical results obtained from design equations.

Fig. 7 Noise from the voltage divider with equivalent current sources, small-signal equivalent.

In practice, designing a basic cell has many advantages. The sizing of each transistor follows a bias specification.

Using the basic cell to build circuits that perform specific functions does not result in decoupling between them. Small signal parameters are defined for each sizing and the same is true with thermal noise generation. The generation of thermal noise, described by (20) and (21) is shown graphically in Fig. 8, where, as expected, the higher the I_{BIAS} current, the lower the noise contribution.

TABLE III
SMALL-SIGNAL PARAMETERS AS FUNCTION OF SIZING, WHERE $L=1.5 \times 10^{-6}$

	1	2	3	4
W_{n3}	3,00 μ m	6,00 μ m	7,50 μ m	21,0 μ m
W_{p2}	104 μ m	209 μ m	259 μ m	757,8 μ m
W_{p1}	104 μ m	209 μ m	259 μ m	757,8 μ m
$V_{REF,1}$	1,22V	1,20V	1,19V	1,1825V
$V_{REF,2}$	-60,6mV	-106mV	-118mV	-134,9mV
I_{DD}	182 μ A	410 μ A	525 μ A	1590,0 μ S
g_{mn3}	180 μ S	370 μ S	475 μ S	1450 μ S
$g_{ds,n3}$	2,81 μ S	6,43 μ S	8,29 μ S	25,3mS
g_{mp2}	843 μ S	2,00mS	2,49mS	7,12mS
$g_{ds,p2}$	9,16 μ S	20,6 μ S	26,4 μ S	74,3 μ S
g_{mp1}	843 μ S	2,00mS	2,49mS	7,12mS
$g_{ds,p1}$	9,16 μ S	20,6 μ S	26,4 μ S	74,3 μ S

Fig. 8 Effect of noise generated by the voltage divider, on the reference nodes.

Figure (9) shows an example to illustrate the use of the basic cell and incorporate thermal noise analysis. In DC, the cells have the same operating point, and this property is not altered when connecting them. Strictly speaking, both cells are voltage dividers. In AC, the basic cell, on the right, is a grounded active resistor and can be understood as the output impedance. By including a capacitor, the network turns out to be a first-order high-pass filter. So it should be noted that the voltage divider does not include three voltage sources as figure shown, but two sources ($V_{n,x,out}$ and $V_{n,y,out}$). Their inclusion in the schematic is only to show that those two noise sources are connected (as indicated) at each gate of the transistors in the cell to the right.

Note that each gate includes the noise source (voltage equivalent) that each transistor generates. For all practical purposes, the total noise source at the gate of each transistor is calculated with (7), and the total noise effect is equivalent to the model shown in (21), where only the corresponding noise sources should be substituted. Note also that if the effect of the capacitor is not included, the calculated noise value is at low frequency value, and including the capacitor in the analysis gives a response equivalent to the transimpedance of the network in the frequency domain. The resulting graph is the one provided by any general-purpose simulator program.

Fig. 9 Noise sources in an active high-pass filter.

IV. CONCLUSIONS

In the design of analog ICs, noise analysis is very important, mainly when the polarization of new technologies is up to 1.0V. Noise analysis, on the other hand, makes it possible to understand and / or determine which variables are under the designer's control so that the know-how leads to a design with less noise effect. Knowing the fundamentals of noise analysis allows the designer to understand how to evaluate its effect on the performance of circuits and systems, fundamentally when every analog circuit uses voltage dividers and its effect is not usually taken into account because thermal noise corresponds to an AC analysis. In a few years, the first centenary of the model to quantify noise, proposed by H. Nyquist, will be fulfilled, and to date his contribution continues to be included in general-purpose simulation programs, and this is so because of its practical utility.

What is new? Silicon devices are known to be candidates for RF applications, and this explains why it is of interest to study thermal noise in Halo devices. Furthermore, when the MOS transistor operates in saturation the thermal noise is dominated by the transistor channel, while in weak inversion the noise is due to the Halo [11] regions. In addition to thermal noise, in GPS applications, where accuracy is not assured due to noise

effects, shot noise is now included because a large number of devices are diodes.

In addition, by considering both sources of noise the position improves [12]. In portable applications, on the other hand, where it is desired to increase the useful life of the batteries, the use of memristors is being considered to develop computer systems, as it is expected to be an option to replace the current DRAMs. Currently the effect of thermal noise in read and write operations is being studied because it should not be forgotten that the memristor is an ionic device [13]. What is evident is that the study of thermal noise does not lose relevance, and understanding it as a fundamental part of any design improves the expected performance.

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