A NOVEL APPROACH FOR POWER OPTIMIZATION IN SEQUENTIAL CIRCUITS USING LATCH BASED CLOCK GATING

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ABSTRACT

Low power design methodologies have gained more prominence in the present designs. Designers will have to come up with amicable designs in order to reduce the power. In synchronous circuits, clock is distributed to all the blocks and it consumes more power dynamically. Clock gating is a technique in which the gating signal has the potential to enable or disable the clock signal.

In this paper clock gating macro is inferred in pre-mapping stage of synthesis. Latch based clock gating is chosen as it reduces the glitches in the circuit. The synthesized netlist is functionally verified with RTL netlist and synthesized netlist, which is followed by PnR. Then power is calculated using test vectors generated after functional verification. Synthesis is carried out for enable signal driven by combinational logic, shift register, counter and sequence detector. Implementation is done to check different scenarios of enable signal and to vary the number of flip-flops used. The dynamic power consumption has reduced by 0.284mW in FSM, 11.754mW in 200-bit counter and 13.441mW 200-bit enable signal driven by combinational logic.

Key words: RTL-Register Transfer Level, FSM- Finite State Machine, PnR- Place and Route.

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1. INTRODUCTION

In the 1970's and 1980's primary concern of designing Very Large-Scale Integrated Circuits was area and speed. Later, complexity of the designs increased to meet the computational and entertainment demands by incorporating signal processing units and graphic cards.

Hence, there was a need to add additional circuitry in the designs to enable checking for proper operation of the chip after fabrication. This process called testability came into picture which added a new dimension to the design process.[1]

In modern day designs, the feature size is decreasing, and more circuits are being integrated per die area, power density is increasing and as a result leading to more power consumption. The need for increased speed of operation and increasing complexity in designs to provide better performance also leads to more switching power. Moreover, with the advent of portable devices in the late 20th Century which operate on battery power, there has been a limit on power that the IC's must consume while simultaneously meeting other required design criteria. The need for miniaturization of devices by reducing battery size has also put a limit on power consumption of IC's. [2]

Low power VLSI design has added a 4th dimension to the design process. Low Power VLSI design techniques are being incorporated in present designs to reduce the amount of power consumed by chips. A lot of investment is made for extensive research in developing EDA tools that address the problem of power optimization. In fact, it has become deciding factor in most modern-day designs. [3]

Designing of circuits with low power strategies have also gain importance. Various techniques have been invented to reduce the power consumption in the chip. For power optimization, an advanced technique called design using power intent description based i.e., UPF have been used industry wide. Bus Invert multiplexing, Gray coding, state machine encoding, Pipelining, parallelism and reducing the unwanted transitions are the popular techniques for power reduction.[4]

Low power design became so prominent in sequential elements which are usually designed with flip-flops or latches, also called as memory elements. Memory elements hold data called tokens. Memory elements are used to enforce sequence, to differentiate the current token from the previous or next token. Therefore, it is called as sequencing elements. Without sequencing elements, the next token might catch up with the previous token, altering both. Sequencing elements delay tokens that arrive too early, preventing them from catching up with previous tokens. Unfortunately, they add some delay which decreases the performance of the system.

Most of the sequential circuits are controlled by clock signal. The transition of register's state is controlled and synchronized by the clock signal. Since the clock switches continuously consumes almost 50% of the dynamic power [5]. Therefore, reducing clock power helps in reducing the total power of the chip.

2. CLOCK GATING

In many synchronous circuits clock gating technique used for reducing dynamic power dissipation. Clock gating saves power by adding logic block to the circuit in which gated clock disables part of the circuit which are inactive so that the flip-flops connected to it do not have to switch states[6].

Clock gating is a technique used to disable register banks during some clock cycles. The typical implementation of registers is using multiplexers as shown in Fig. 1. Clock gating cell replaces multiplexers [7] and aids in saving Dynamic power. Clock gating cell has low toggle rate on clock pin. Gated by the enable signal, the clock network has less switching activity and consumes less dynamic power. Clock gating circuit is easy to implement, and in source code no change is required since it can be implemented in synthesis stage.

Figure 1 Without Clock Gating

Clock Gating macro has internal circuit of latch-based clock gating and it is used to route internal fabric signal to global network. The enable signal can be used to turn off the global network to save power. Latch based clock gating as shown in Fig. 2 is glitch free, doesn't need setup and hold check, hence most commonly used [8].

Figure 2 Latch based Clock Gating

The latch-based clock gating adds a level-sensitive latch to the design to hold the enable signal from the active edge of the clock until the inactive edge of the clock. Since the latch captures the value of the enable signal and holds it until complete clock pulse. The enable signal should be stable around the falling edge of the clock, since negative latch is used.

Figure 3 Waveform for latch-based clock gating

Fig. 3 consist of waveform for output of latch-based clock gating macro. At the negative edge of clock if enable is high the latch stores value high. The output of latch is anded with the clock to get gated clock output. It can be observed that gated clock removes glitches in enable signal.

3. METHODOLOGY OF POWER ESTIMATION

Figure 4 Methodology

Fig. 4 shows various steps carried out in power analysis of sequential circuits.

- A synthesizable source code is written.
- The source code is synthesized which includes 3 steps compilation, pre-mapping and mapping.
 - Compilation stage checks the syntax of source code and optimizes the RTL. It gives technology independent netlist.
 - The inputs to pre-mapping stage are timing constraints, low power file and compilation output. In pre-mapping the inference of clock primitives is carried out.
 - Mapping stage generates technology netlist and forward annotates constraints to be passed to PnR.
- The output from synthesis stage and source code are verified for its functionality using testbench as input. The output of functional verification is test vectors.
- The synthesized output is then given to PnR tool.
- The output of PnR and test vector is given as input to Power analysis.

4. IMPLEMENTATION

The RTL code is written, and synthesis is performed. The enable signal of the flip-flop is extracted and different fanouts of clock are checked by varying the number of flops used by varying the data_width of din.

Synthesis is carried out for enable signal driven by combinational logic, shift register, counter and sequence detector.

4.1. Enable Signal Driven by Combinational Logic

Enable pin of flop is driven by combinational logic which is anded output of two enable signals.

Figure 5 RTL view of enable signal driven by combinational logic

Fig. 5. consists of RTL netlist after optimization and compiling source code. In RTL netlist clock gating macro is not inferred.

Figure 6 Pre-mapping view of enable signal driving flops with different control signals.

Fig. 6 shows the pre-mapping view, in which clock gating macro is inferred by extracting enable and clock.

4.2. Shift Register

Flip-flop with synchronous reset and enable signal is used to implement 2-bit shift register.

Figure 7 RTL view of shift register

Fig. 7 shows RTL netlist of 2-bit shift register without clock gating macro.

Figure 8 Pre-mapping view of shift register

Fig. 8 shows the pre-mapping view of two-bit shift register after inference of clock gating macro.

4.3. Counter

Counter of 4-bit is implemented, input value will be passed to output of flop when both enable and load are high. When enable is high the value will be incremented since it's a up counter. When load is high and enable is low the flip-flop will retain its previous value.

Figure 9 RTL view of counter

Fig. 9 shows RTL view of counter of 4 bit without clock gating macro.

Figure 10 Pre-mapping view of counter

Pre-mapping view of counter with clock gating macro after enable and clock extraction is shown in Fig. 10

4.4. FSM

The implementation of sequence detector for sequence 101101.

Figure 11 RTL view for FSM

The RTL view of sequence detector before inference of clock gating macro is shown in Fig. 11.

Figure 12 Pre-mapping view for FSM

The inference of clock gating macro in sequence detector after extraction of enable and clock is shown in Fig. 12.

Figure 13 FSM for sequence detection

Fig. 13 shows the state diagram for 101101 sequence detector.

5. RESULTS AND DISCUSSION

Functional verification and power calculation are carried out. Functional verification includes comparison of RTL netlist, synthesized and optimized netlist to check if the functionality remains same after optimization. Test vectors are generated after functional verification.

Power calculation is carried out using test vectors generated after functional verification which is used to calculate dynamic power of the design.

Above steps are performed by changing the data_width which is the variable used to change the number of flip-flops used, hence changing clock load in the design for enable signal driven by combinational logic, shift register, counter and FSM.

Functional verification and Power calculation in flipflops with enable signal driven by combinational logic:

Figure 14 Simulated output of flipflops with enable signal driven by combinational logic

In Fig. 14 whenever enable is high the value of input is passed to output. When reset is high the output will be reset.

Figure 15 Dynamic power dissipation in enable signal driving different types of flops

In Fig. 15 number of flops used is changed by varying variable data_width. For data_width of 200 13.441mW dynamic power reduction is observed.

Functional verification and Power calculation of shift register:

Figure 16 Functional verification of shift register

In Fig. 16 when enable signal is high the input value is passed to output after a clock cycle, since two flops are in series.

Figure 17 Dynamic power dissipation of shift register

In Fig. 17 it is observed that there is dynamic power reduction of 8.194mW power reduction for 200-bit flops used.

Functional verification and Power calculation of counter:

Figure 18 Functional verification of counter

When load and enable are high, input value is passed to output as shown in Fig. 18. The counter value is incremented when enable is high and retained its value when load is high.

Figure 19 Dynamic power dissipation of counter

From Fig 19 it is observed that 11.744mW power reduction is observed when 200-bit flops used.

Functional verification and Power calculation of FSM:

Figure 20 Functional verification of FSM

Fig. 20 shows simulation output of functional verification of FSM. Whenever enable is high, reset is low and input sequence is 101101 the output will be high and low if reset is high.

Figure 21 Dynamic power dissipation of FSM

Fig. 21 shows dynamic power reduction of 0.284mW for 3-bit sequence detector.

In this paper it is found that

In 200-bit enable signal driven by combinational logic dynamic power reduction of 13.441mW is observed.

In 200-bit shift register 8.194mW dynamic power reduction is observed.

In 200-bit counter 11.744mW dynamic power reduction is observed.

In 3-bit FSM 0.284mW dynamic power reduction is observed.

6. CONCLUSION

Clock gating is useful for registers which has to maintain same logic values over many clock cycles. Shutting off the clocks eliminates unnecessary switching activity. The main challenges of clock gating are finding the best places to use it and creating the logic to turn off and turn on the clock at the proper times. Clock Gating is relatively simple to implement because it only requires a change in the netlist but not in source code. No additional supply power or power element changes is required. Since Latch based Clock gating is glitch free, it is used for dynamic power reduction. The dynamic power consumption has reduced by 0.284mW in 3-bit FSM, 11.754mW in 200-bit counter and 13.441mW in 200-bit enable signal driven by combinational logic.

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