DESIGN AND ANALYSIS OF QUASI CASCADED MULTI-LEVEL INVERTER

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ABSTRACT

This paper presents new topology of Quasi multi-level inverter (MLI) with five level output voltage. Traditional cascaded MLI is a buck DC-AC conversion circuit, which puts a limit on the peak AC voltage. However, within the proposed converter a shoot through state is implemented to increase the output voltage. The number of passive components used in the circuit is less, thereby reducing size, cost and weight. The voltage unbalance problem is prevented by using a low voltage capacitor between the two full bridge outputs. The capacitor voltage of each module is organized with a PI controller to generate the switching pulses for switches of the proposed structure. Simulation results are added to examine the feasibility.

Keywords: Boost inverter, Cascaded Multilevel inverter, and quasi-Z-source inverter

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1. INTRODUCTION

Multilevel inverters (MLI) are so popular attentions from scholars because of their blessings of improved satisfactory output waveforms with decrease fashionable Total Harmonic Distortion (THD), smaller filter size and lessor electromagnetic interface (EMI) [1]. Some of the basic multilevel inverter topologies are flying capacitors, neutral point clamped (NPC), and Cascaded Multilevel Inverters (CMI). Among those topologies, the CMI has more popular due to modularity and its contribution of excessive power. It makes the CMI an appealing choice for applications including uninterruptible power supplies (UPS), grid-connected system, Statcom and motor drive [2-4].

The conventional cascaded multilevel inverter is a stepdown DC-AC energy conversion, in which the peak AC output voltage is restrained through the DC voltages. In [5] an extra DC-DC boost converter is added for every module within the CMI topology to attain the excessive AC output voltage while the DC input voltages are low. Adding DC-DC boost power converter

consequences in low efficiency and excessive price. Two capacitors, two enhance inductors, two diodes, ten switches, filter inductor used in the conventional CHB-BFLI.

DC-link voltage on each full bridge circuit can be controlled using boost converter. Short circuit in the DC source can be avoided by inducing a dead time between two switches in a leg [6]. Singlestage power conversion in a cascaded ZSI was proposed in [7]. The number of the ST states in the single-phase Single Bridge Inverter (SBI) is two in one switching period. Therefore, the switching frequency of the inductors are half of the operating frequency. In cascaded ZSI, the input DC current possess less ripple and hence continuous. The same DC-link voltage can be producing by controlling the ST duty cycle in each module of cascaded ZSI. The control of Three-phase cascaded ZSI's is demonstrated and proposed in [8].

Cascaded ZSI based PV power generation and energy storage system is proposed in [9]. Fault tolerant cascaded inverter using Z-sourced network are demonstrated in [10]. Design and simulation of cascaded transformer based multilevel inverter using single Z-source network is investigated in [11]. Dual-boost/buck converter used Active Cascaded Multilevel Inverter (ACMI) is proposed in [12]. Similar to cascaded ZSI, ACMI inverter also has the buck boost voltage and shoot-through immunity. Moreover, the cascaded ZSI and the ACMI inverter use a large number of passive elements with raising the cost, weight & size of the cascaded system.

The Quasi Z Source (qZS) network is replaced by a quasi-switched boost (qSB) network [13]. On comparison of qZS network, the qSB network uses one less inductor, one less capacitor, one more switch and one more diode in front of the main full bridge circuit. The qSB network based isolated high step up DC-DC converter is proposed. In this paper, a new quasi cascaded full bridge five level boost inverter (qCFB-FLBI) in single stage is proposed. In the proposed CMI, the qSB network is used in each module.

This work proposes a quasi-cascaded five-level boost output with a phase shifted pulse width modulated scheme to control the non-shoot through and shoot through states of the inverter modules. The peak value of AC output can be boosted with the help of shoot through state. The quasi switched boost structure is used in the full Bridge modules that reduces the number of passive components at the same time increasing the shoot-through immunity.

The voltage imbalance problem while cascading the output voltages in full Bridge modules needs to be addressed. The structure of the converter is to be designed in a such a way that it aids the cascading of more than two full bridge modules to increase the output AC voltage's level obtained from the converter. The circuit needs to be analyzed using simulation for various loading conditions and the results are compared with conventional CMI to ensure that objective of the proposed converter.

2. PROPOSED QUASI CASCADED MULTI LEVEL INVERTER

The configuration of proposed single-stage Quasi cascaded multi-level inverter (QCMI) is presented in Fig.1. The proposed inverter contains two DC sources, an inductor filter in the output side and two quasi boost inverter (qBI). Single qBI module contains two diodes, four power switches, boost inductor and capacitor. The proposed QCMI has five levels in output voltage. It operates symmetrical and asymmetrical modes.

2.1. Operating Principles

Double qBI modules operates with same parameters, so module A is used to analyze the operating principle. Fig. 2 shows modes of operation of the qBI module A in the inverter. The switches S_1 and S_2 are turned on in the Shoot-Through (ST) state 1, as shown in Fig. 2(a), D_{A1} is conducting, while D_{A2} is blocking.

The output voltage of the qBI module A is $-V_{CA}$ when the switch S_3 is on otherwise it is zero. The inductor L_A is charged by the source.

Figure 1 Proposed QCM with Filter Capacitor.

Figure 2 Modules operating states 1, (b) ST state 2, (c) NST state 1, (d) NST state 2, (e) NST state 3 and (f) NST state 4.

The switches S_2 and S_3 are turned on in the NST state 2, as shown in Fig. 2(d), The qBI module A output voltage is $-V_{CA}$. The switches S_1 and S_4 are turned on in the NST state 3, as shown in Fig. 2(e), The qBI module A output voltage is V_{CA} . During the non-Shoot through (NST) states as shown in Figs. 2(c)–2(f), D_{A1} and D_{A2} are conducting. The capacitor C_A is

charged from V_1 , while the inductor L_A transfers energy from the DC voltage source to the main circuit. The full bridge circuit is equivalent as a current source, i_{PNA} .

$$L_A \frac{di_{LA}}{dt} = V_1 - V_{CA} \quad (2)$$

In one switching period, T , each leg has twice short circuits alternatively. From (1) and (2), volt-sec balance equation is

$$\bar{V}_{LA} = \left[1 - 2\frac{T_0}{T}\right] (V_1 - V_{CA}) + 2\frac{T_0}{T} V_1 \quad (3)$$

where $T_0/T = D_1$, a ST duty ratio in each leg of module A, T_0 is total ST time intervals in one leg. The average inductor voltage should be zero in a steady state.

$$V_{CA} = \frac{1}{1-2T_0/T} V_1 = \frac{1}{1-2D_1} V_1 \quad (4)$$

Similarly, we also obtain the capacitor voltage on the module B as

$$V_{CB} = \frac{1}{1-2D_2} V_2 \quad (5)$$

2.2. Modulation control of the proposed inverter

For module A, the control voltages, $-V_s$ and V_s are compared to a high frequency carrier signal, V_{t1} , produce control pulses for the S_1 and S_2 switches. The DC voltages, V_{SH} and $-V_{SH}$, are compared with V_{t1} to produce the S_{0a} control pulse. Then S_{0a} is added to the control pulses of switches S_1 and S_2 to produce the ST states. Likewise, the V_{t1} is shifted by 90° to create another high-frequency carrier signal, V_{t2} . V_s and $-V_s$ are compared with V_{t2} to produce control pulses for the S_3 and S_4 switches. V_{SH} and $-V_{SH}$ are compared to the V_{t2} to produce S_{0b} control pulse. The S_{0b} is then added to the control pulses of switches S_3 and S_4 to produce the ST states. As a result, the output voltage V_{ab} of the inverter module A contain three levels. Similar for the second inverter module, two control voltages (V_s and $-V_s$) are shifted in 180° to produce output voltage V_{cb} of the module B.

The difference of V_{ab} and V_{cb} gives the output voltage V_{ac} Fig. 3. Shows Phase Shifted Modulation (PSM) for the proposed QCMI. The number of the ST is four in one switching period in the proposed QCMI as shown in Fig. 3, the switching frequency of inductors is the one fourth times the operating frequency. Therefore, high frequency current ripple is reduced.

To achieve a quality of output voltage as shown in Fig. 4, the capacitor voltage in each module will be the same. From (4) and (5), the capacitor voltages V_{CA} and V_{CB} , is controlled by ST duty cycle D_1 and D_2 respectively. When D_1 is different from D_2 to keep $V_{CA} = V_{CB}$ in such a case the input voltage in each module is unbalanced. The difference between D_1 and D_2 results in generating the DC offset at the output voltage. A capacitor C is added to the output of the inverter to remove the DC offset of the output voltage.

(a)

(b)

(c)

Figure 1 PWM pattern for the proposed QCMI. (a) S1 and S2 switching pattern, (b) S3 and S4 switching pattern, (c) S5 and S6 switching pattern, (d) S7 and S8 switching pattern

Fig. 1. Shows the inverter with unbalanced DC source condition, where the capacitor C is connected between b_1 and b_2 at filter output. Assuming $V_C = V_{CA} = V_{CB}$, the DC offset voltage is calculated as

$$V_C = \frac{D_1}{1-2D_1} V_1 - \frac{D_2}{1-2D_2} V_2 = (D_1 - D_2) V_C \quad (6)$$

The voltage stress on C is very low because of the very low value of difference between D_1 and D_2 . Therefore, the size of the overall cascade system is small due to the size and cost of the capacitor C.

3. COMPARISON WITH CONVENTIONAL CMI

Comparison of the passive and active components of the qCMI is shown in table 1. The proposed inverter uses two less switches and one more capacitor in comparisons with CBFL but the CBFLI has a shoot through problem. The switching frequency is one fourth times the operating frequency of the full bridge circuit, while it is two times in the cascaded ZSI. As a result, the high frequency current ripple on inductors of the proposed QCMI is a half that of the cascaded ZSI.

Since, the cascaded ZSI has the same nature in shoot-through immunity as the proposed QCMI, the voltage stress comparison between two inverters is addressed. Table I compares the equations of the cascaded ZSI to the proposed QCMI. As in Table I, the capacitor voltages of the cascaded ZSI are smaller than those of the proposed inverter. However, capacitor voltage stresses in each module is same. The voltage stress on switches and diodes of the proposed inverter is same as that of the cascaded ZSI.

Table 1 Comparison between the proposed qCMI and the Conventional Five – Level Inverters.

S.NO	PARAMETERS	QCMI	CascadedZSI	CBFLI
1.	Inductors	2	4	2
2.	Capacitors	3	4	2
3.	Diodes	12	10	12
4.	Power switches	8	8	10
5.	Shoot-through immunity	Yes	Yes	No
6.	Input current	Continuous	Continuous	Continuous
7.	Inductor frequency	4fs	2fs	Fs

4. SIMULATION RESULTS AND ANALYSIS

To test the performance of the proposed QCMI, MATLAB simulation model has been developed. Table II shows the simulation parameters used.

Table 2 Simulation parameters of proposed qCHB-FLI

PARAMETERS	RATINGS
Power	1kVA
Output Voltage& Frequency	230Vrms& 50 Hz
Inductors (L_A & L_B)	3mH
Capacitors (C_A & C_B)	4.7mF/400 V
C	4.4mF/25 V
Inductor (L_F)	4mH
Load Resistor (R)	40 Ω
Switching frequency (fs)	20KHz

All switches are assumed with 0.3 Ω as on state resistance in the simulation. First, $V_1 = V_2 = 50$ V so as to conform the properties of the balanced DC source condition. When both input voltages are the same then Fig. 4 shows the simulation results for the proposed QCMI. Fig. 4(a) shows, the five-level output voltage of the inverter and the load voltage is 230 V_{rms}. From Fig. 4(a), it is seen that both the capacitor C_A and C_B voltages are boosted to 126 V in the steady state and the peak to peak voltage on C_A and C_B capacitors is 7 V. The square waveform of each modules of the DC link voltage is shown in Fig. 4(b).

Under unbalanced DC source condition, input voltage of modules, $V_2 = 60$ V, while $V_1 = 50$ V is considered.

The simulation results asymmetric OCML is shown in Fig.5.

4.(a)

5 (a)

4 (b)

5 (b)

4 (c)

5 (c)

Figure 4 (a) Simulation results for $V_1=V_2=50V$ of five level output voltage, output current, inductor currents, capacitor voltages, (b) THD of Output voltage, (c) THD of uotput current.

Figure 5 (a) Simulation results for $V_1=50V$ & $V_2=60V$ of five level output voltage, output current, inductor currents, capacitor voltages, (b) THD of output voltage, (c) THD of output current.

Table 3 Output Voltage THD

PARAMETERS	QCM I	Cascaded ZSI	CBFLI
When $V_1=V_2=50$ V	1.90	3.10	3.21
When $V_1=50$ V & $V_2=60$ V	2.60	3.50	3.86

Table 4 Output Current THD

PARAMETERS	QCM I	Cascaded ZSI	CBFLI
When $V_1=V_2=50$ V	2.08	3.40	3.60
When $V_1=50$ V & $V_2=60$ V	2.35	3.70	3.90

(a)

(b)

Figure 5 (a) THD in Output voltage, (b) THD in output current.

The output voltage of the proposed inverter has five levels and the load voltage is $230 V_{rms}$ as shown in Fig. 5(a). From Fig. 5(a), both the capacitor C_A and C_B voltages are also boosted to 126 V in the steady state, and the peak-to-peak voltage on C_A and C_B capacitors are 7 V. The average value of the capacitor C filter voltage is very low, about 7 V.

The total size and weight of proposed inverter is not affected as the size of the capacitor filter as small. The square waveform as shown in Fig. 5(b) for the DC link voltage of each module. Because the ST duty cycle of module B is smaller than that of module A, there are high distortion in the positive half cycle of the five-level output as shown in Fig. 5(a). When the ST

duty cycle of module A is higher than that of module B the five-level output voltage has a lower distortion in the negative half cycle.

THD analysis of the output current and voltage between the cascaded ZSI, CFLBI and the proposed QCMi is shown in Table III and IV. It can be observed from Table III and IV that the THD of the output current and voltage of the proposed inverter is lower than that of the cascaded ZSI.

5. CONCLUSION

A single-phase QCMi five-level inverter with boost voltage ability is proposed here. The features of the proposed inverter are as follows: Output voltage in five levels, reduced number of passive components and shootthrough immunity. Enhanced rejection of disturbance with good performance can be achieved by using PI controller maintaining constant voltage at capacitor. Circuit analysis and its PWM control strategy for the proposed system was discussed. Simulation results are shown to validate the proposed QCMi. Number of full Bridge modules can be added to increase the levels of output voltage, thus increasing the reliability and modularity of the converter. The proposed inverter can be used in distributed generation with more DC sources and grid integrated PV systems.

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