(Research Article)

Novel and reliable design of 5-input Majority Gate in Quantum dot Cellular Automata Approach**Sankit Kassa^{1*}, Shikha Nema²**^{1*,2}Department of Electronics Engineering, Usha Mittal Institute of Technology, Mumbai, INDIA**Abstract**

It is the demand and necessity of time to achieve a reliable and low power consumption circuit designs for a very fast growing field of low power circuit designing at nano technology. The Quantum-dot Cellular Automata (QCA) can be an alternative of CMOS approach for this low power nano-scale regime due to its small size, extremely high speed of operation, reliable circuit designing and robustness in the structure. In this presentation, a novel 5-input majority gate has been presented using Rotated Majority Gate structure only. Rotated Majority Gate (RMG) is a fundamental logic gate in QCA approach similar to Original Majority Gate. Mathematical proof for RMG Gate is obtained and structural analysis for 5-input MG has been carried out systematically. Based on the proposed 5-input MG, a novel design of 1-bit Full Adder has been implemented which requires very less number of cell counts, area and clock cycles in its design. QCADesigner 2.0.3, a simulation tool, has been used for checking the working condition of the proposed approaches.

Keywords: QCA, 5-input Majority Gate, Inverter, Full Adder**1. Introduction**

Various techniques like QCA (Quantum dot Cellular Automata), SET (Single Electron Transistor), TPL (Tunneling Phase Logic) and CNT (Carbon Nano Tube) are available to design low power VLSI circuits at nano-scale regime but amongst them, QCA is best suitable because of its attractive features of high speed of operation, low power consumption, high density, small dimension of quantum dot cells and high reliability and robustness in the circuit. Lent et al. proposed a physical implementation of an automaton using quantum-dot cells in 1993 which quickly gained popularity among researchers worldwide and it was first fabricated in 1997 [1].

1.1 QCA basic Building Blocks: As shown in Figure 1(a), four quantum dots in a single QCA cells are there, arranged in a square pattern, with two extra electrons residing diagonally to each other. By tunneling these electrons, we create mutual electrostatic force between them and get either logic '0' or logic '1'. Figure 1(b) shows the wire structure in QCA approach.

For designing any QCA circuit, we require two basic logic gates: (1) QCA Inverter and (2) QCA Majority gate. QCA

Figure 1. QCA (a) Cell structure (b) Wire

Inverter is a basic logic gate which inverts the topology of an input from one logic to another as shown in Figure 2 (a), while QCA Majority gate (MG) are combination of 5 QCA cells that gives the output according to the arrangement of QCA cells. Original Majority Gate (OMG) and Rotated Majority Gate (RMG) are two types of MG as shown in Figure 2 (b).

(a)

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Figure 2. QCA (a) Inverter (b) Majority Gate

RMG gate can be a very good option sometimes compared to OMG gate and if we utilize both of them very effectively, we can get good circuit design with very less area and energy [12-13]. In this presentation, we have given mathematical proof for RMG gate as well as made a new 5-input MG which is a novel first design of its kind utilizing 12 number of QCA cells in its structure.

2. Mathematical Proof for Rotated Majority Gate

Here A, B, C are inputs and Y is Output. Output (Y) will always gain the opposite value than that of Imaginary Output (Y_1). So we will find the value of imaginary output (Y_1) here. For mathematical proof, all the equations and assumption have been taken from [2].

If A=logic '1', B=logic '1' and C=logic '0'. Then, Y_1 =?

Figure 3. Circuit diagram of RMG gate showing the central device cell's output as an imaginary output (Y_1) for (a) logic '0' and (b) logic '1'

Assumption 1: If Y_1 is logic '0' as in Figure 3

Figure 3 a (electron x)	Figure 3 a (electron y)
$U_1 = \frac{A}{r_1} = \frac{23.04 \times 10^{-29}}{20.09 \times 10^{-9}} = 1.146 \times 10^{-20} J$	$U_1 = \frac{A}{r_1} = \frac{23.04 \times 10^{-29}}{42.94 \times 10^{-9}} = 0.536 \times 10^{-20} J$
$U_2 = \frac{A}{r_2} = \frac{23.04 \times 10^{-29}}{20.09 \times 10^{-9}} = 1.146 \times 10^{-20} J$	$U_2 = \frac{A}{r_2} = \frac{23.04 \times 10^{-29}}{42.94 \times 10^{-9}} = 0.536 \times 10^{-20} J$
$U_3 = \frac{A}{r_3} = \frac{23.04 \times 10^{-29}}{42.94 \times 10^{-9}} = 0.536 \times 10^{-20} J$	$U_3 = \frac{A}{r_3} = \frac{23.04 \times 10^{-29}}{42.94 \times 10^{-9}} = 0.536 \times 10^{-20} J$
$U_4 = \frac{A}{r_4} = \frac{23.04 \times 10^{-29}}{20.09 \times 10^{-9}} = 1.146 \times 10^{-20} J$	$U_4 = \frac{A}{r_4} = \frac{23.04 \times 10^{-29}}{20.09 \times 10^{-9}} = 1.146 \times 10^{-20} J$

$U_5 = \frac{A}{r_5} = \frac{23.04 \times 10^{-29}}{28.28 \times 10^{-9}} = 0.81 \times 10^{-20} J$	$U_5 = \frac{A}{r_5} = \frac{23.04 \times 10^{-29}}{18.11 \times 10^{-9}} = 1.27 \times 10^{-20} J$
$U_6 = \frac{A}{r_6} = \frac{23.04 \times 10^{-29}}{18.11 \times 10^{-9}} = 1.27 \times 10^{-20} J$	$U_6 = \frac{A}{r_6} = \frac{23.04 \times 10^{-29}}{28.28 \times 10^{-9}} = 0.81 \times 10^{-20} J$
$U_{T11} = \sum_{i=1}^6 U_i = 5.384 \times 10^{-20} J$	$U_{T12} = \sum_{i=1}^6 U_i = 4.164 \times 10^{-20} J$

$$U_{T1} = \sum_{i=1}^2 U_i = 9.548 \times 10^{-20} J$$

Figure 3 b (electron x)	Figure 3 b (electron y)
$U_1 = \frac{A}{r_1} = \frac{23.04 \times 10^{-29}}{28.28 \times 10^{-9}} = 0.81 \times 10^{-20} J$	$U_1 = \frac{A}{r_1} = \frac{23.04 \times 10^{-29}}{18.11 \times 10^{-9}} = 1.27 \times 10^{-20} J$
$U_2 = \frac{A}{r_2} = \frac{23.04 \times 10^{-29}}{18.11 \times 10^{-9}} = 1.27 \times 10^{-20} J$	$U_2 = \frac{A}{r_2} = \frac{23.04 \times 10^{-29}}{28.28 \times 10^{-9}} = 0.81 \times 10^{-20} J$
$U_3 = \frac{A}{r_3} = \frac{23.04 \times 10^{-29}}{28.28 \times 10^{-9}} = 0.81 \times 10^{-20} J$	$U_3 = \frac{A}{r_3} = \frac{23.04 \times 10^{-29}}{53.74 \times 10^{-9}} = 0.42 \times 10^{-20} J$
$U_4 = \frac{A}{r_4} = \frac{23.04 \times 10^{-29}}{2.828 \times 10^{-9}} = 8.14 \times 10^{-20} J$	$U_4 = \frac{A}{r_4} = \frac{23.04 \times 10^{-29}}{28.28 \times 10^{-9}} = 0.81 \times 10^{-20} J$
$U_5 = \frac{A}{r_5} = \frac{23.04 \times 10^{-29}}{28.28 \times 10^{-9}} = 0.81 \times 10^{-20} J$	$U_5 = \frac{A}{r_5} = \frac{23.04 \times 10^{-29}}{20.09 \times 10^{-9}} = 1.146 \times 10^{-20} J$
$U_6 = \frac{A}{r_6} = \frac{23.04 \times 10^{-29}}{42.94 \times 10^{-9}} = 0.536 \times 10^{-20} J$	$U_6 = \frac{A}{r_6} = \frac{23.04 \times 10^{-29}}{20.09 \times 10^{-9}} = 1.146 \times 10^{-20} J$
$U_{T21} = \sum_{i=1}^6 U_i = 11.706 \times 10^{-20} J$	$U_{T22} = \sum_{i=1}^6 U_i = 4.932 \times 10^{-20} J$

$$U_{T2} = \sum_{i=1}^6 U_i = 16.638 \times 10^{-20} J$$

With comparison to the above results, we can conclude that the potential energy of cell-2 ($U_{T2} > U_{T1}$) in Figure 1a is lower. So, cell-2 will be logic '1'. Same as if cell-1 is logic '0', so we can take cell-2 as logic '0' if they are connected in series with each other.

3. Proposed 5-input Majority Gate

A novel 5-input MG is proposed utilizing the important area minimizing factor of RMG gate. Figure 4 shows the layout diagram of the proposed 5-input Majority Gate. The design includes total 12 number of QCA cells. A, B, C, D, E are inputs and Y is the output. We can get output according to the Boolean logics applied at the inputs as shown in Table 1.

Figure 4. 5-input Majority Gate

Table 1. Values of different input cells for Boolean logic in 5-input MG

Boolean logic	A	B	C	D	E	Expression	OUTPUT
3-INPUT AND	I/P	I/P	I/P	0	0	$Y = \Sigma(A, B, C, 0, 0)$	$A.B.C$
3-INPUT OR	I/P	I/P	I/P	1	1	$Y = \Sigma(A, B, C, 1, 1)$	$A+B+C$
1-BIT FA CARRY	I/P	I/P	I/P	1	0	$Y = \Sigma(A, B, C, 1, 0)$	$AB+BC+CA$

Figure 5. Graphical representation of 5-input MG with polarity of each cell for inputs (1, 0, 1)

(a)

(b)

Figure 6. 5-input MG based 1-bit FA (a) Layout (b) schematic diagram

Table 2. Comparison of different Full Adder designs with the proposed design

Reference designs	Area (μm^2)	Complexity (Total number of Cell Count)	Delay (Clock Cycles)	Wire Crossing
[4]	79	0.65	4	Multilayer
[5]	58	0.04	4	Multilayer
[6]	69	0.07	4	Coplanar

[7]	71	0.06	6	Coplanar
[8]	59	0.05	6	Coplanar
[9]	61	0.05	3	Multilayer
[10]	105	0.14	3	Multilayer
[11]	63	0.05	3	Coplanar
Proposed Design	50	0.05	3	Coplanar

Comparison of the proposed 5-input majority gate based FA design with previous well known designs is given in table 1. One can easily observe from the table that the proposed design is much better in all aspects w.r.t. previous ones.

5. Simulation Results

For computer simulation purpose, we have used QCADesigner 2.0.3 [3] tool. The default parameter values have been taken for simulation as shown in table 3. Figure 7 shows the output waveform obtained using QCADesigner for proposed 5-input MG based 1-bit Full Adder design.

Figure 7. Simulation result for 1-bit Full Adder

Table 3. Default parameter values in QCADesigner tool

Parameter Name	Values
Number of Samples	12800
Convergence Tolerance	0.001
Radius of Effect [nm]	65.000
Relative Permittivity	12.900
Clock High	9.800E-22
Clock Low	3.800E-23
Clock Shift	0.00E+00
Clock Amplitude Factor	2.000
Layer Separation	11.500
Maximum Iterations per Sample	100.000

6. Conclusion

This paper gives the mathematical proof for Rotated Majority Gate as well as shows its importance by utilizing it for designing a new 5-input Majority Gate design, which is effective enough to minimize the overall circuit area. Mechanistic analysis of the proposed approach is also carried out. For showing effectiveness of the proposed 5-input MG, 1-bit full adder circuit has been designed. The results of the proposed FA designs have been compared with previous designs which show much overall improvement in the proposed design. The proposed design shows 50% of total saving in terms of area, 67% saving in terms of complexity and 50% saving in terms of Clock cycles compared to the recent designs of Full Adder. The simulation has been attained using QCADesigner 2.0.3 tool.

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