STABILIZATION OF CORIOLIS VIBRATORY GYROSCOPES BY FREQUENCY LOCKING TO ULTRA STABLE CLOCKS

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ABSTRACT

This work demonstrates experimentally, for the first time, stabilization of a MEMS Coriolis Vibratory Gyroscope (CVG) drive loop by frequency-locking to an ultra-stable clock acting as a frequency reference. A theoretical model is presented to explain the experimental results and predict ultimately achievable rate bias instability performance based on a variety of high stability reference oscillators. A 600 μm diameter, 40 μm thick silicon disk resonator gyroscope (DRG) operated in its $n = 3$ wineglass mode is employed as the proof of concept test device and the stabilized drive loop is implemented using a Zurich Instruments HF2LI digital lock-in amplifier.

INTRODUCTION

MEMS Coriolis Vibratory Gyroscopes (CVGs) have favorable cost, size, weight, and power compared with conventional gyroscope technologies, but suffer from relatively poor stability [1]. To date, microfabrication and environmental sensitivity hurdles have limited the adoption of MEMS gyroscopes in high-precision applications. A significant effort has been expended by the MEMS research community on novel fabrication and interrogation methods for MEMS CVG resonators, seeking mainly to increase the stability of these devices in the gyroscope application through improvements in symmetry, mitigation of energy losses to maximize mechanical quality factor (Q), and elimination of conductive over-coatings which damage the pristine nature of the as-fabricated structures [2-7]. While a great amount of progress has been made, and many novel technologies proposed and developed at the device level, these approaches all rely on the CVG resonator itself as the source of stability in the gyroscope readout system, in addition to its function as the rotation sensitive component.

We propose an alternative approach to improving stability of MEMS CVGs, in which the source of system stability comes from a separate, ultra-stable frequency reference, wherein the CVG resonator only serves as the rotation sensitive component. HRL has recently demonstrated that significant improvement is possible in the stability of a silicon disk resonator gyroscope (DRG) by controlling the temperature of the DRG to a few milli-Kelvin, which ultimately can be performed on a micro-ovenization platform with integrated heaters and resistance temperature detectors (RTDs) [8]. The present work builds on the frequency-locked ovenization scheme in [8] by moving the frequency locking concept directly into the gyroscope control loops and introducing an ultra-stable frequency reference.

CONCEPT AND THEORY

HRL's new control scheme treats the MEMS CVG resonator as a gearbox on a highly-stable clock, which could be a commercial chip-scale atomic clock (CSAC), a conventional ovenized quartz crystal oscillator (OCXO), or an emerging high-performance MEMS oscillator. Figure 1a shows the typical or measured clock stability in terms of Allan Deviation (ADEV) of fractional frequency of a few potential reference clocks. Based on the seminal Lynch model [9], HRL has developed a theoretical model which relates the gyro bias instability ADEV ($B(\tau) = \sigma_{\Omega}(\tau)$) to the clock ADEV ($\sigma_y(\tau)$) which is assumed to represent the contribution of each individual mode to residual frequency mismatch (Δf) between

the mode-matched and stabilized CVG control loops, where k is the CVG angular gain and Q is the quality factor of the CVG modes:

$$B(\tau) = \frac{90\sqrt{2}f\sigma_y(\tau)}{kQ} [^\circ/\text{s}]; \sqrt{2}f\sigma_y(\tau) \approx \Delta f. \quad (1)$$

Figure 1: (a) Measured and typical Allan Deviation (ADEV) of fractional frequency of potential reference clocks shows that a pairing of an OCXO and a CSAC will provide the best stability over a wide range of integration times. (b) Reference clock stability converted to equivalent ultimate gyro stability showing that an 8 mm silicon DRG will exceed its state-of-the-art intrinsic performance [8] when locked to either an OCXO or a CSAC.

The above model, when applied to measured 8 mm diameter, 250 μm thick silicon DRG drive loop frequency stability (purple trace in Figure 1b) with the addition of thermomechanical noise using the well-known gyro angle-random-walk (ARW) formula [10], closely matches (within an order of magnitude) measured rate ADEV of a silicon DRG precisely controlled down to 3 mK (green trace in Figure 1b) [8]. The extra experimental noise beyond the model is expected to arise due to additional bias instability resulting

from demodulator errors. This result affirms the model is capable of predicting the ultimate CVG noise when all parameters are controlled to high stability. Using the predictive capability of HRL's new model, stabilizing the DRG to a CSAC (red trace in Figure 1b) or an OCXO (blue trace in Figure 1b) would give orders of magnitude improvement in ARW and bias instability beyond state-of-the-art MEMS gyroscopes.

Figures 2 and 3 present the original frequency and rate stability data for the 8 mm DRG from [8] which was used in the analysis presented in Figure 1b to derive the purple and green ADEV curves.

Figure 2: 8 mm DRG frequency versus RTD temperature variations over a 14 hour run showing a total variation in the frequency and DRG temperature of 2.6 mHz and 5.8 mK, respectively [8].

Figure 3: 8 mm DRG rate output versus RTD temperature variations over a 14 hour run [8].

EXPERIMENTAL DEMONSTRATION

CVG Device

The demonstration vehicle for proving the concept of frequency locking the control loops of a CVG to an ultra-stable clock was chosen to be a 600 μm diameter, 40 μm thick variant of the silicon DRG which was available in large quantities thanks to the Stanford epi-seal MPW run funded by DARPA. This resonator was designed at HRL based on the existing 8-fold symmetric DRG,

with appropriate modifications to fit into the Stanford process. Also, the electrodes were designed to be paired periphery electrodes in contrast to the internal electrodes of the standard DRG [10]. An SEM of this structure is shown in Figure 4.

Figure 4: SEM of HRL's 600 μm diameter, 40 μm thick silicon Disk Resonator Gyroscope (DRG) fabricated courtesy of DARPA and the Kenny group at Stanford. SEM courtesy of Yushi Yang at Stanford.

The overall die size including electrodes, pad and routing metal, and vias was 2 mm by 2 mm as shown in in Figure 5. Also presented in Figure 5 is the pin assignment and wirebonding configuration. Since the device was fabricated on a (100) silicon wafer, it is apparent that the $n = 3$ mode is the appropriate mode of choice for gyroscope operation due to the expected low frequency split. The traditional $n = 2$ modes of the DRG are expected to have a large frequency split on a (100) wafer, limiting their usefulness for gyroscope application. The epi-sealed die was attached to a 24 pin Cerdip package for easy interfacing of the device.

Figure 5: Wirebonding configuration and pin assignment of 2 mm by 2 mm epi-sealed silicon DRG die mounted in 24 pin Cerdip package.

The measured resonances are shown in Figure 6 along with finite element predictions of the modal frequencies and shapes. The measured frequencies and frequency splits agree well with their finite element predicted values. The $n = 2$ modes are situated in the range 240 to 260 kHz, and exhibit the expected large frequency split of 12 kHz. The $n = 3$ modes measure around 311 kHz and exhibit a frequency split of only 270 Hz. Tuning experiments have shown that up to 500 Hz of tuning range is available on these devices with only 5 V of DC tuning, which is sufficient to mode match the DRG.

Figure 6: Measured and simulated $n = 2$ and $n = 3$ resonances of the 600 μm diameter silicon DRG. The $n = 2$ modes measure 242.34 kHz and 254.84 kHz, respectively for a 12.5 kHz frequency split. The $n = 3$ modes measure 311.48 kHz and 311.75 kHz, for a frequency split of only 270 Hz.

Figure 7: Zurich Instruments HF2LI Digital Lock-In Amplifier used to demonstrate frequency locking of a gyroscope control loop to an ultra-stable frequency source. The 600 μm diameter silicon DRG is interfaced to the HF2LI through a PCB breakout board which contains the 24 pin Cerdip socket and direct pinout to SMA connectors.

Test Setup and Experimental Results

To demonstrate experimentally that a MEMS CVG can be locked to a stable frequency source and inherit its stability, HRL has

locked the drive loop of the 600 μm silicon DRG to an OCXO and improved the loop frequency stability $> 10 \times$ using a benchtop system centered on a Zurich Instruments HF2LI digital lock-in amplifier that includes a 10 MHz high-stability OCXO reference (Figure 7). The HF2LI was fitted with the Ultra-High-Stability (UHS) option, which provides short term stability < 50 parts per trillion, long term aging of < 0.4 ppm/year, and a phase noise of -140 dBc/Hz @ 1 kHz offset from carrier.

The block diagram of this digital implementation of frequency-locking is shown in Figure 8a. The DRG is operated in its $n = 3$ wineglass mode which is sensed using a transimpedance amplifier (TIA) fed into the PLL block to adjust the local oscillator (f_{drive}) to track the natural resonance of the DRG. The measured ADEV shows the intrinsic frequency stability of the unstabilized DRG is 2 ppb at approximately 60 s (Figure 8b top line). A second oscillator is used to provide a reference frequency ($f_{\text{set-point}}$) in the tuning range. The output signal of the DRG is demodulated at $f_{\text{set-point}}$, providing a phase difference which is routed to the input of a PID controller with a phase set-point equal to the natural resonance of the DRG. The PID applies a control voltage to the frequency tuning port (T) of the DRG, tuning its resonance to $f_{\text{set-point}}$. In this case, the tuning port consisted of applying an equal DC voltage on both the clockwise and counterclockwise quadrature tuning electrodes due to the $n = 3$ wirebonding and electrode configuration. Future devices are expected to have independent tuning ports for each independent wineglass mode. The ADEV of this frequency-locked DRG is plotted in Figure 8b (bottom line) and does not show a minimum for all times measured (up to 1,000 s). At 60 s, the stability is better than 0.1 ppb, 20 $\times$ better than without locking. Beyond 60 s, the control scheme improves the stability to 100 $\times$ over the uncontrolled DRG. With this first experimental demonstration of frequency-locking of a CVG to an ultra-stable clock, we have shown that orders of magnitude of stability of a silicon MEMS gyroscope can be gained.

DISCUSSION

Equation (1) is valid when the CVG is a symmetric structure operated in a mode-matched condition. The frequency split in Equation (1) results from the inability to perfectly control the frequency in each control loop (drive mode and sense mode) of the gyroscope. The limit of frequency split control is determined by the fractional frequency stability of each control loop. Since the frequency noise in each control loop is assumed to be uncorrelated, the factor of $\sqrt{2}$ accounts for drift in the frequency of each mode relative to the other in the total frequency split.

In the original Lynch model [9], there is a factor of $\sin(2\theta_r)$ which should be considered in Equation (1), where θ_r represents the angle between the transducer axes and the principal modal damping axes. However, in a highly symmetric structure, such as the DRG, the damping is distributed around the circumferential direction of the structure and it is not clear that there is a preferred set of principal damping axes. Therefore, given the above and the inability to predict a value of θ_r for a given DRG device in practice, we took the worst case situation by letting $\sin(2\theta_r) = 1$ in our model. It remains to be seen if some DRGs have smaller sensitivity to this source of bias drift than others, at which point a conclusion can be made as to whether a set of preferred damping axes exist in the DRG structure.

The novel control loop in Figure 8a should be implemented around both the CVG drive mode and sense mode. This experiment is in progress to show the ultimate goal of improving the output rate stability of the DRG. Also, further tuning of the loop parameters is needed for optimal performance. However, this concept of using a high stability frequency source to stabilize the control loop of a

sensor applies to other types of resonant MEMS sensors beyond CVGs. For example, resonant magnetometers, accelerometers, or gravimetric sensors could all improve their ultimate sensitivity by stabilizing the sensitive device to a higher intrinsic stability frequency reference.

Figure 8: First demonstration of frequency-locking CVG control scheme showing enhanced frequency stability ($> 100 \times$ @ 1000 s) of HRL's silicon DRG when locked to an OCXO frequency reference. (a) Block diagram of control scheme used to stabilize HRL's 600 μm Stanford-fabricated epi-seal encapsulated silicon DRG. The light gray box with dashed outline indicates the traditional MEMS CVG control loop, while the outlined beige box indicates the new control loop added to stabilize the control loop frequency. Operational parameters are: $V_{\text{bias}} = 25 \text{ V}$, $V_D = 20 \text{ mV}_{\text{ao}}$ and $f_{n=3} = 301.8 \text{ kHz}$ (b) Measured frequency stability shows orders of magnitude improvement with stabilized control loop operation (PID-on).

CONCLUSION

The demonstrated frequency-locking concept significantly reduces microfabrication and environmental sensitivity hurdles that have limited the adoption of MEMS gyroscopes in high-precision applications. We anticipate that this technology will enable MEMS sensors to progress significantly beyond their current levels of performance.

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