METAL-SU-8-GRAPHENE INTEGRATED CIRCUIT TECHNOLOGY FOR RIGID AND FLEXIBLE SUBSTRATES

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ABSTRACT

We have demonstrated in our previous work that SU-8 is effective and stable in ambient n-doping technique for graphene. In this paper we proposed a reliable technology for constructing graphene integrated circuits that can be used as an alternative to CMOS where graphene and SU-8 were used as replacements to silicon and oxide. In this work we selectively doped a graphene sheet and both n-type and p-type graphene FETs were fabricated on the same graphene sheet on a rigid and flexible substrates. E-beam lithography was used to pattern SU-8 resist and then selectively doped the SU-8 resist within the graphene sheet. The fabricated graphene transistors observed a high stability in air and at a wide range of temperatures.

INTRODUCTION

Graphene has attractive research interest since its discovery in 2004 [1]; Geim and Novoselov receipt of the Nobel Prize in 2010. The ultrahigh electron mobility and cutoff frequency of graphene made it a candidate for future integrated circuits design. However, the lack of a reliable and practical technology for fabricating graphene circuits delayed the chance of transfer graphene circuits to the market.

It is well known that pristine graphene in always has a p-type property in ambient due to the oxygen that interact with the graphene edges [2]. However, Fabricating integrated circuits requires making both n-type and p-type graphene transistors monolithically on a single substrate. We have demonstrated in our previous work [3] that SU-8 is an effective and stable in ambient n-doping technique for graphene. We found out that the photo-acid generator (PAG), one of the SU-8 chemical components, is the n-doping source for graphene. The doping concentration can be controlled by controlling the amount of SU-8 chemical components (PAG, epoxy resin and cyclopentanone).

FABRICATION OF GRAPHENE CIRCUIT

One great benefit of using e-beam lithography to expose SU-8 [4] is the ability to selectively pattern and n-dope a graphene sheet at the nanoscale feature size. First, graphene was transfer to a SiO₂/Si substrate. Three Ti/Au electrodes were constructed on the graphene sheet to form two transistors, via e-beam lithography, metal deposition, and the metal lift-off patterning. The SU-8 3005 was spin-coated on a SiO₂/Si substrate with a spin speed of 6000 rpm. Then, the substrate was soft-baked at 65 °C for 3 min and then at 95 °C for 3 min. JEOL 840 e-beam lithography instrument was used for selectively pattern the SU-8 resist within graphene sheet. The instrument operated at acceleration voltage of 35 kV, beam current of 25 pA and dose of 3 μC/cm². Then samples were developed by SU-8 developer for ~1 min, followed by immersion in isopropanol, and a rinse with DI water. Finally, samples were hard baked at 100 °C for 3 min. As schematically shown in Figure 1(a,b), The SU-8 coated graphene was an n-type region and the uncoated graphene was a p-type region. The two transistors shared a same back gate as an input voltage terminal (V_{in}). The source and drain contacts of the two transistors were connected together for use as an output voltage terminal (V_o), Figure 1 (c). We should

mentioned that for preciously and selectively doping, a sacrificial layer, for example, PMMA resist is need to be deposited on the other parts of graphene sheet prior to patterning SU-8 to protect them from doping, which usually occur due to the effects of the impinging electrons during e-beam exposure (Figure 1 (d)).

Figure.1 An integrated graphene inverter: (a) the schematic of the circuit fabrication; (b) the SEM image of the fabricated inverter; (c) the circuit layout and (d) Fabrication process.

CHARACTERIZATION OF GRAPHENE CIRCUIT

To verify the formation of the n-type and p-type transistors on the same graphene sheet, the transfer resistances R_p and R_n between the source and drain contacts of the individual FETs were measured as a function of the applied voltage V_{in} , as illustrated in Figure 2.

Figure 2: The transfer resistance (R_p and R_n).

The measured Dirac points of both the p-type and n-type graphene sheets were at -27 V and 17 V, respectively. By connecting p-type FETs to V_{DD} and n-type FET to the ground, a Dirac point splitting along the V_{in} axis and then the complementary configuration were achieved within the region of Dirac points. The voltage transfer characteristic of the fabricated inverter is given in Figure 3. The two FETs operated in the range between the Dirac points. Away

from the Dirac points, the saturation of the output voltage V_0 resulted in the approximately constant ratio of R_n/R_p , when $V_{in} < -27$ V for the n -type FET and $V_{in} > 17$ V for the p -type FET. The voltage gain of the inverter was much less than 1, as determined by $A = dV_0/dV_{in}$. The small voltage gain of the fabricated inverter could be mainly due to the very small change of the transistor resistances around the Dirac points. The swing voltage of the inverter was 3 mV at $V_{DD} = 10$ mV. The threshold voltage (V_{TH}), which is the input voltage at the maximum voltage gain of the inverter, was approximately 5.6 mV ($V_{in}=V_{TH}$) and slightly greater than $V_{DD}/2$.

Figure 3: Voltage transfer characteristic, demonstrating a logic inverter function.

The ambient stability of n -type FET was studied by measuring the V_s - σ for 7 days of air exposure (Figure 4(a)) results showed no major change in the mobility of the charge carriers. The maximum carrier mobility was ~ 800 cm²/Vs. The device was also stable at relatively wide range of temperature (Figure 4 (b)).

Figure 4. n -type FET chemical stability: (a) In ambient for several days (b) At temperature variation.

Our developed metal-SU8-Graphene technology can also be applied in the development of flexible graphene transistors. The fabrication of transistor began with the deposition of a 10 μ m Parylene layer on a silicon substrate, which was used as a mechanical carrier during the subsequent fabrication process. The

graphene was transferred onto the Parylene surface and confirmed by Raman spectroscopy (Figure 5(c)). Schematic of the device illustrated in Figure 5(a) and device after fabrication is illustrated in Figure 5(b). Figure 5(d) shows the flexibility test of Parylene based graphene circuits.

Figure 5. Flexible n -type graphene FET: (a) The overview of graphene-polymer layer structure; (b) A fabricated device; (c) Raman spectrum of graphene transferred on a Parylene substrate. (d) Demonstration of the device flexibility.

CONCLUSION

Doping a dedicated area within graphene sheet in a nanoscale feature size is a great achievement. It represents a practical method for Metal-SU-8-Graphene (MSG) integrated circuit technology. This technology can be applied for digital and analog circuits, as well. Furthermore, it can be used in the development of flexible graphene electronic circuits, which provides an enormous opportunity for future applications in, for example, biomedical systems.

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