ULTRA-MINIATURIZED POWER CONVERTER MODULES USING MICROMACHINED COPPER SCAFFOLDS

C.D. Meyer^{1,2*}, S.S. Bedair¹, B.C. Morgan¹ and D.P. Arnold²

¹U.S. Army Research Laboratory, Adelphi, Maryland, USA

²University of Florida, Gainesville, Florida, USA

ABSTRACT

This paper presents ultra-miniature ($<2\text{ mm}^3$) power converter modules with high power density (77 W/cm^3) enabled by micromachined 3D copper scaffolds containing high-inductance-density (130 nH/mm^2) air-core power inductors. The scaffolds are formed by electroplating multiple, $30\text{-}\mu\text{m}$ -thick layers of copper within patterned photoresist molds, yielding freestanding copper traces with $>10:1$ aspect ratios. After backfilling with a chemically-resistant polymer, the scaffolds are then fully detached from the silicon fabrication wafer by wet-etching an underlying oxide layer. Surface-mount switch/controller chips and capacitors are attached by solder reflow to the copper scaffolds, forming self-contained converter modules.

INTRODUCTION

While modern power converters for portable electronics are typically realized with a switch/controller IC that is connected at the PCB level to a handful of off-chip passives, self-contained “single-chip” power converter modules are highly desired for size, performance, cost, and system integration. Reduced-size-scale dc-dc converters could replace series regulators in mobile communications devices, providing greater efficiency in down-converting battery voltage levels to the continually decreasing supply voltages required by LSI circuits [1]. Diminutive size and weight will also be prerequisite to the mobility of future envisioned autonomous robotic microsystems [2], which will further require a sort of mobile “pico-grid” for efficient energy transfer to a system of sensors, actuators, and processors having vastly divergent power needs [3].

The power inductor remains one of the greatest impediments to the miniaturization of power converters, and it increasingly dominates the overall size as converter volume decreases. Inductors by their nature require large areas or high-magnetic-permeability materials to increase induction. Emerging high-frequency converter circuits switching at 10^3 – 10^5 ’s of MHz have reduced inductance requirements down to 10^3 – 10^5 ’s of nH. However, magnetic materials exhibit greatly increased core losses at these frequencies due to eddy currents and domain dynamics [4], [5]. On the other hand, air-core microinductors, common in RF applications, typically have inductances that are too low for most power converters and yield low quality factors at sub-GHz frequencies.

At Hilton Head 2010 [6] we presented a process for realizing 3D air-core microinductors and transformers formed in $10\text{-}\mu\text{m}$ -thick copper layers. Leveraging strong magnetic coupling between vertically stacked, tightly wound planar spirals, the devices yielded high inductance densities $>100\text{ nH/mm}^2$ [7]. However, the process required sequential removal of the molding and seed metal at each layer, so that photoresist posts would remain between windings to prevent electrical shorting. Although the inductors provided high quality factors >20 on Pyrex substrates, they would need to be fabricated monolithically on an IC converter substrate in order to form a compact power converter. However, this approach would increase high-frequency losses due to coupling with the conductive substrate and would require extra processing to protect the freestanding structures during packaging.

In this article, we now report an extension of our 3D copper process with $3\times$ thicker layers to realize inductors that not only have lower dc resistance (DCR) but also are sufficiently robust to be detached from the fabrication wafer. With aspect ratios up to $10:1$ per layer, the process results in tighter coil turns than have been achieved in other 3D metal efforts [8], [9], [10]. Furthermore, the multilayer copper process is generalized into a flexible microfabrication platform that enables the formation of air-core microinductors within other copper scaffolding structures. When detached from the silicon fabrication wafer, the copper scaffolding functions as an interposer for interconnecting power IC and passives all within a highly compact, integrated module, as depicted in Fig. 1. The scaffolds are constructed of three independently molded layers of $30\text{-}\mu\text{m}$ -thick electroplated copper. For the purpose of demonstration, scaffolds containing 130 nH microinductors were microfabricated and tested with commercially available boost converter chips and surface-mount capacitors that were attached by solder reflow.

Figure 1: Photographs of converter module. (a) Multilevel copper scaffolding detached from Si. (b) Surface-mount capacitors and BGA converter chip soldered to copper pads. Tip of ballpoint pen shown (left) for size reference.

BACKGROUND AND DESIGN

Chip-scale power modules have previously been demonstrated by integrating the inductor into an interposer that sits between the power IC and the circuit board that is to be powered. Hayashi, et al. [1] fabricated solenoidal-winding inductors within a $525\text{-}\mu\text{m}$ -thick ferrite wafer to which IC chips were flip-chip ultrasonic bonded using gold stud bumps. Wang, et al. [11] fabricated spiral-winding inductors using a silicon wafer as a mold, which was subsequently etched away and back-filled with a ferrite-polymer composite; an IC chip and capacitors were mounted onto the 0.6-mm -thick inductor by solder reflow.

In contrast, the use of detached copper scaffolds in this work results in an inductor interposer platform that, at a total thickness of $90\text{ }\mu\text{m}$, is several times thinner than these previous results. The use of stacked, planar spiral windings within an interposer is also unique and results in exceptionally high volumetric inductance density. As depicted in Fig. 2, the inductor design consists of six turns in each of the two $30\text{-}\mu\text{m}$ -thick winding layers, which are arranged in a square-shaped spiral layout with a 1 mm outer diameter, $32\text{ }\mu\text{m}$ trace width, and $16\text{ }\mu\text{m}$ lateral spacing between

Figure 2: SEM of air-core microinductor realized in three layers of 30 μm thick electroplated copper.

adjacent turns. Because all three copper layers were deposited with equal thicknesses, the vertical gap between the upper and lower winding layers was similarly 30 μm .

FABRICATION

The copper scaffolds are fabricated by the process illustrated in Fig. 3. The scaffolds are constructed on standard, 500- μm -thick, 100-mm-diameter silicon wafers. First, a 2- μm -thick insulating layer of silicon dioxide is deposited via PECVD, which forms the sacrificial release layer for later detachment. Next, a 20 nm layer of Ti is sputter deposited over the oxide to improve the adhesion with copper. The copper scaffolds are then sequentially constructed layer-by-layer by electroplating copper onto thin sputter-deposited copper seeds through photoresist molds. The details are explained next.

Figure 3: Illustration of process sequence to realize integrated converter module by detaching multilevel copper from silicon wafer and attaching surface-mount parts by solder reflow.

At the start of each layer, the surface is cleaned by RF sputter etching to remove any oxide from the surface of the preceding electroplated copper. Then a 200 nm seed of copper is sputter deposited over the entire wafer surface. Higher power dc sputtering (1.2 kW, 12-inch-diameter target) yields improved adhesion of the copper seed to underlying photoresist as compared to lower power. Positive-tone AZ9245 photoresist is spun to a thickness of 30 μm and cured. Contact lithography is used to expose the regions where copper is to be plated, and the photoresist is developed by immersion in AZ400K developer. Ashing in O_2 plasma is then

used to clean the copper seed of any residual photoresist scum in the developed regions.

The thick copper structures of each layer are electroplated in an acid copper sulfate electrolyte bath composed of 15 g/L Cu and 210 g/L sulfuric acid [12]. The electroplating is timed such that the copper fills just to the top of the photoresist mold, and no further planarization steps are taken. The sequence of sputter deposition, photolithography, and electroplating is repeated for each layer. Three layers are used to form the scaffolds, as shown in Fig. 3a.

Finally after all layers have been deposited, the photoresist molds and copper seeds are all removed simultaneously by ultrasonic agitation Baker PRS-3000 *N*-methyl-2-pyrrolidone (NMP) photoresist stripper. Subsequent etching in a solution of ceric ammonium nitrate removes the bottommost copper seed. After the wet processing steps, the wafer is rinsed in water and dried on a hotplate (Fig. 3b). The process has been tested with up to four 30- μm -thick layers of copper and yields critical dimensions $\sim 5 \mu\text{m}$ for aspect ratios up to 20:1, as demonstrated in Fig. 4.

Figure 4: (a) Fins implemented in four layers of 30 μm thick copper illustrate fine resolution capability, (b) as used, for example, to form slits in an inductor winding.

The 3D freestanding copper scaffolds are then backfilled with Brewer ProTEK A2-22 protective polymer, which is specifically formulated for resistance to hydrofluoric acid [13] (Fig. 3c). After curing on a hotplate, the backfilled copper scaffolds are released from the wafer by sacrificial oxide etching in hydrofluoric acid (Fig. 3d). For testing purposes, the individual converter modules are affixed to an aluminum nitride substrate (Fig. 3e), though in practice the scaffolds would likely be connected by solder reflow to a PCB containing the broader circuit of the desired application. A BGA-style converter chip and surface-mount capacitors are mounted onto landing pads on the scaffolds by solder reflow (Fig. 3f).

RESULTS

Inductor Impedance Characterization

Prior to attaching the converter chip and capacitors, the impedance of the inductor was measured in order to verify functionality after encapsulation and wafer detachment. Impedance was measured using an Agilent E8361A network analyzer with excitation frequency swept from 10 MHz – 1 GHz and RF probes landed at one-port ground-signal-ground pads formed in the copper scaffolding at the input of the inductor. As plotted in Fig. 5, the inductor yielded 130 nH inductance with a self-resonant frequency of 370 MHz. A peak quality factor (ratio of imaginary to real part of impedance) of 15 was obtained at 160 MHz. The inductor dc resistance was measured at 0.695 Ω using a Keithley 2400 SourceMeter with four-point probing and 20 mA source current.

The performance parameters of the inductor are summarized

Figure 5: Plots of frequency-dependent inductance and quality factor of micromachined inductor after encapsulation and detachment from Si wafer.

in Table 1 for comparison with several example inductors from the literature that have been tested within chip-scale power converter circuits. Compared to the air-core microinductor reported in [14], the inductor presented here features $>10\times$ the inductance while occupying the same lateral area at 1 mm^2 . Similar levels of inductance and peak quality factor are found in the ferrite-core surface-mount 0402-sized inductor tested in [15], but at roughly $5\times$ the volume. The magnetic-film-core microinductors were designed for low DCR and are larger than even the 0402 surface-mount part.

Table 1: 3D copper microinductor of this work compared to those demonstrated in mm^3 -scale converters in other works. Parameters are inductance (L), dc resistance (DCR), peak quality factor ($Q_{\max}$) and inductor volume.

Example	Core	L	DCR	$Q_{\max}$	Volume
This work	Air	130 nH	0.7 Ω	15	0.09 mm^3
Micro. on Si [14]	Air	11 nH	0.4 Ω	30	0.31 mm^3
Surface-mount[15]	Ferrite	140 nH	0.3 Ω	12	0.49 mm^3
Micro. on Si [15]	NiFe	150 nH	0.2 Ω	4	1.26 mm^3
Micro. in Si [11]	NiZn	350 nH	0.1 Ω	10	5.40 mm^3
Micro. in NiZn [1]	NiZn	1650 nH	0.02 Ω	20	6.43 mm^3

Converter Testing

The copper scaffolding platform was tested in conjunction with a Texas Instruments TPS61240 boost converter chip, which is designed to output a fixed voltage of approximately 5 V. The TPS61240 was selected for having one of the highest switching frequencies amongst commercially available boost converters at up to 4.5 MHz and, as such, called for one of the lowest values of inductance at 1 μH . Because the microinductor was significantly smaller-valued at 130 nH, the converter was only able to effectively regulate the output voltage at light load currents in the pulse frequency modulation (PFM) mode of operation. Two surface-mounted 4.7 μF capacitors with $1.0\text{ mm} \times 0.5\text{ mm}$ footprints were soldered onto the converter module for source and load filtering.

Two Keithley 2400 SourceMeters were used in the test setup and were connected by needle probes to the converter module: one in source mode at the input regulated the input voltage V_{in} and measured the input current I_{in} ; the other in electronic load mode at the output regulated the output current I_{out} and measured the output voltage V_{out} . Fig. 6 indicates these quantities on a simplified boost circuit diagram. Input and output powers were calculated from these measurements as the product of voltage and current, and efficiencies were calculated as the ratio of output to input power. The output current I_{out} was swept from 1 mA to 30+ mA for several values of V_{in} , with V_{out} fixed at 5 V by the converter circuit.

Figure 6: Simplified circuit diagram of boost converter circuit. Diagram indicates measurement points of input voltage (V_{in}) and current (I_{in}), output voltage (V_{out}) and current (I_{out}), and inductor voltage (V_L).

Figure 7: Inductor voltage $v_L(t)$ measured as a function of time for one series of high frequency pulses.

The inductor voltage $v_L(t)$ was monitored using a LeCroy oscilloscope with high impedance probes. As shown in the waveform in Fig. 7, the inductor was intermittently switched with a high frequency pulse sequence—the amplitude, duty cycle (D), and frequency (f_s) of which were dependent on the input voltage. These pulse sequences were repeated at lower frequencies as necessary to maintain an output voltage with $<100\text{ mV}_{\text{p-p}}$ ripple (i.e. as a function of output current).

As plotted in Fig. 8, the converter efficiency was relatively insensitive to output current but fell off dramatically with decreasing input voltage (increasing conversion ratio). For input voltages of 3.0 V, 3.5 V, and 4.0 V, the switching frequencies (f_s) within each pulse sequence were measured to be 3.9 MHz, 4.1 MHz, and 4.2 MHz with duty cycles D of 0.5, 0.4, and 0.3, respectively. Greater duty cycles were associated with lower efficiencies, since the longer pulse width ($v_L > 0\text{ V}$) more nearly approached the L/R time constant of the inductor. A peak

Figure 8: Plot of the converter module efficiency measured as a function of output current with 5 V output and several different input voltages.

efficiency of 62% was measured with $V_{in} = 4$ V and $I_{out} = 5$ mA, while a maximum power output of 153 mW was recorded at 60% efficiency with $V_{in} = 4.0$ V and $I_{out} = 30$ mA. At output currents greater than those reported in Fig. 8, the converter exhibited control loop instability as it switched to the pulse-width modulation (PWM) mode of operation.

CONCLUSION AND FUTURE WORK

The process of 3D micromachining detachable copper scaffolds represents a powerful new capability for realizing ultra-miniature power systems, enabling high performance passives to be built into self-contained modules with minimal volume. With its low profile and wafer detachment, the microfabricated inductor presented in this work provided exceedingly high volumetric inductance density ($1.4 \mu\text{H}/\text{mm}^3$). As a result, high power density ($77 \text{ W}/\text{cm}^3$) was obtained from testing the 130 nH inductor in combination with a commercially available ~ 4 MHz boost converter chip, despite the converter being designed for a much larger inductor (1 μH).

The 3D copper scaffolding is particularly complementary for use with emerging power converters of higher switching frequency (tens to hundreds of MHz), which require even smaller passive components. The process may additionally be used to form high dielectric strength capacitors through interleaved plates of high aspect ratio copper. Because the scaffolds are fully exposed and freestanding, it may be possible to selectively backfill inductor and capacitor structures with magnetic and dielectric composites, respectively, prior to encapsulating the full scaffold package.

Deformable sockets formed in the copper scaffolding (Fig. 9) could ease the integration of the smallest-sized surface-mount components (with $400 \mu\text{m} \times 200 \mu\text{m}$ footprint), which are problematic to attach by solder reflow due to tomb-stoning and misalignment [16], [17]. The converter IC and capacitors could then be integrated with the scaffolding before embedding to enable wafer-level packaging of fully integrated converter modules.

Figure 9: Deformable copper sockets (a) before and (b) after fitting with a 01005-sized resistor and capacitor.

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CONTACT

*C.D. Meyer, tel: +1-301-394-4286;
christopher.d.meyer1.civ@mail.mil