DIRECT-WRITE NANOLITHOGRAPHY ON FLEXIBLE SUBSTRATE

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ABSTRACT

This paper presents a mask-less lithography process using direct-write nanofibers via near-field electrospinning on flexible substrate as masking materials in processes such as lift-off, wet-etching and dry-etching. The polymer fibers have diameter of sub-micrometer to micrometer with good adhesion to substrate and chemical sustainability. Key demonstrations successfully realized in this work include sub-micrometer metal gaps, micro heaters and definition of graphene structures on flexible substrates. As such, this direct-write lithography technique could find applications in low-cost microelectronics, including flexible electronics.

KEYWORDS

Mask-less lithography, electrospinning, flexible electronics

INTRODUCTION

Lithography process is one of the most important and widely used processes in the fabrication of IC (Integrated Circuitry) and MEMS (Microelectromechanical Systems). Large area patterns are generated using photoresist and mask via the conventional optical aligner at moderate cost. Some limitations in the typical lithography processes include low design flexibility and difficulty in processing flexible substrates such as roll-to-roll fabrications. Furthermore, for sub-micrometer features, several advanced lithography solutions have been introduced such as nano imprinting [1], and direct-write femto-second laser mask [2] to realize small features which are not available in conventional lithography processes. Moreover, e-beam lithography has been used in areas such as electronic circuitry [3] and photonic crystal [4], [5]; AFM (Atomic Force Microscopy) has been used to generate sub-100nm scale features for nanoelectronics [6] and NEMS (Nanoelectromechanical Systems) devices [7]. All of these aforementioned processes are excellent tools in creating ultra-small features in nanolithography processes but they are limited to either very expensive equipment or small area operations.

In this paper, we introduce the direct-write nanofibers on flexible substrates as a “shadow mask” for mask-less lithography in processes such as lift-off, wet-etching and dry-etching with several potential advantages. First, the process does not require photoresist as the hard mask as polymeric fibers are deposited to the substrate by controlling the movement of an x-y stage for designated patterns via the near-field electrospinning technique [8]. Second, the process is simple and low-cost without any expensive equipment. The basic setup includes a high voltage power supply and x-y stage to generate continuous fibers with well-controlled deposition precision. Third, the process can deposit fibers on flexible and dielectric substrates for possible applications in new emerging areas such as flexible electronics. Fourth, the diameter of fibers is adjustable with a range from sub-micrometer to 10 μ m. These features make the technology an excellent candidate for mask-less lithography processes. Several proof-of-concept prototype demonstrations have been conducted and characterized in this work and the experimental setup of the details of near-field electrospinning has also been described.

NEAR-FIELD ELECTROSPINNING SETUP

Spinning on flexible/dielectric substrate

Previously, the well-controlled electrospinning process has been conducted on hard and conductive substrate [8] as a strong electrical field between the syringe and substrate is required to generate and control the deposition location of fibers. Here, a modified setup is utilized to enable direct-write of fibers on flexible and dielectric substrates. Figure 1 shows the schematic diagram of the near-field electrospinning process used for flexible or dielectric substrates. In the prototype experiments, a doped silicon wafer or metal coated hard substrate is placed underneath the flexible or dielectric substrate. The conductive substrate is grounded by connecting it to the negative side while the metal syringe tip is connected to the positive side of the power supply, respectively. In contrast to the far-field electrospinning process, a small gap of less than 1mm is used in near-field electrospinning process and about 1kV of voltage is strong enough to generate continuous fibers. The target flexible substrate such as Kapton film is placed on top of the conductive substrate. As illustrated in the electrical field simulation results in the right image of figure 1, the electrical field between syringe and conductive material can be still be established with the existence of the dielectric substrate. Therefore, electrospun fibers can be pulled from the tip of the syringe onto the dielectric substrate.

Figure 1. Schematic diagram of the direct-write nanolithography process on a non-conductive flexible substrate. The near-field electrospinning process utilizes high electrical field formed between the metal syringe tip and conductive substrate lying underneath the target dielectric flexible substrate. COMSOL® simulation shows electric field can be established within the flexible dielectric substrate on top of grounded conductive substrate.

DIRECT-WIRTE MASK-LESS LITHOGRAPHY

Process demonstrations: Lift-off, Wet-etching, Dry-etching

Based on the proposed direct-write nanolithography process as shown in figure 1, three lithography-based microfabrication processes including lift-off, wet-etching and dry-etching, are chosen as the demonstration examples in this work. In all experiments, the flexible dielectric film, Kapton, were chosen as the substrate and PEO (Polyethylene Oxide) was selected as the electrospun fiber material. Figure 2 illustrates process flows for lift-off, wet-etching and dry-etching, respectively, using the direct-write mask-less lithography technique.

Figure 2. Three basic mask-less lithography and etching processes via the direct-write nanolithography technique: (a) lift-off, (b) dry-etching, and (c) wet-etching to demonstrate (a) sub-micrometer gap, (b) micro heater, and (c) graphene etching processes.

In the lift-off process as shown in figure 2(a), a gap of narrower than $1\mu\text{m}$ is the target demonstration. First, a $25\mu\text{m}$ -thick Kapton film is placed in the near-field electrospinning setup. Thin PEO fibers are directly deposited on top of Kapton film to form the gap. A 50nm -thick gold layer is deposited using e-beam evaporation and the lift-off process is performed by dipping the sample into DI (Deionized) water for 5 minutes. As the PEO fiber is dissolved in DI water, the sub-micro meter metal gap as defined by the diameter of the electrospun fiber could be easily constructed. Figure 3 shows the optical image of a fabricated sub-micrometer gap at the top and a SEM image at the bottom.

Figure 3. A sub-micrometer gap was formed by using the electrospun PEO nanofiber as the lift-off shadow mask: (a) Optical and (b) SEM images.

For the wet-etching process as shown in figure 2(b), two requirements should be fulfilled for the electrospun fibers to be effectively used as mask. First, the fibers must have good adhesion to the substrate to prevent possible leakage of etchant underneath the fiber during the etching process. The adhesion strength between the fiber and the substrate is generally determined by the choice of polymers and solvent used in the electrospinning process. Solvents

such as acetone evaporate fast and result in weak adhesion force. Polymers which use DI water as solvent typically have better adhesion strength with the Kapton substrate. Experimentally, PEO polymer with 20% v/v mixing ratio with DI water have shown good adhesion strength on Kapton and copper substrate in the prototype tests. The second requirement for the electrospun fiber as the etching mask in the wet etching process is their chemical resistance to the etchant as the physical dimension of masking fibers should be maintained throughout the whole wet-etching process. It turns out that the PEO polymer used in the prototype experiments is robust during entire copper wet-etching process. In the process as shown in figure 2(b), a 30nm -thick copper is via the sputtering process on top of the Kapton substrate. The designed device pattern, a micro heater, is then written on to the copper thin film via the near-field electrospinning process. After the wet-etching process, figure 4(a) shows the optical image of a fabricated substrate being deformed under the force between two fingers. Figure 4(b) is the image of the fabricated micro heater under an optical microscope. The width of the heater could be adjustable during the timed etching process. However, as the copper film has many grain boundaries which result in uncontrolled etching in the boundary areas, the overall wet-etching process is challenging with poor pattern accuracy compared with the lift-off and dry-etching process to be discussed in the next session.

Figure 4. Optical image of micro-heater fabricated on flexible Kapton film. (a) A fabricated substrate being deformed between two fingers. (b) The image of the fabricated micro heater under an optical microscope. The width of the heater can be adjusted by the time-etching process.

Figure 2 (c) shows the dry-etching process using direct-write electrospun fibers. Similar to the wet-etching process, good adhesion of fiber to substrate is desirable. Moreover, dry-etching is generally used to generate patterns with smaller line width such that even small amount of gas/plasma leak under the fiber can severely impact the process. Multiple tests have been conducted and the conclusions from the prototype experiments indicate that PEO fibers have good adhesion to Kapton substrate and their gas barrier property against oxygen plasma is very good. Therefore, graphene patterning by means of oxygen plasma has been chosen as the demonstration example for the dry-etching process. A silicon dioxide layer is deposited on top of the Kapton film to promote adhesion of graphene. A CVD grown, single layer graphene is transferred on the substrate via the scoop and dry method [9]. The PEO fiber is directly-written on the substrate followed by oxygen plasma etching for 5 seconds at 50Watt to define a $2\mu\text{m}$ -wide line-pattern of graphene. The fiber is then removed by dipping into DI water with sonication for 5 minutes. Figures 4(a) and (b) show: Raman spectroscopy result on the patterned graphene area and the optical photo of the graphene, respectively. Raman spectroscopy has also been examined at the adjacent areas and the responses have shown only background noises (result not shown) as the verification for the successful wet-etching/patterning process.

Figure 5. (a) Raman spectroscopy taken on the patterned graphene structure by O_2 plasma etching at 50Watt for 5 seconds. (b) The graphene channel was visible under the optical microscope.

Figure 6 shows the capability of using electrospun fibers to make good lithography patterns with an array of structures. Figure 6(a) is four $2\mu\text{m}$ -wide electrospun fibers with an equal separation distance of $50\mu\text{m}$ and figure 6(b) shows the etching result of patterned graphene structure. Clearly, the graphene film has been successfully patterned and PEO fibers have been removed as the successful demonstration of using near-field electrospinning to generate arbitrary patterns as a dry etching masking layer.

Figure 6. (a) An array of electrospun fibers with equal separation distance of $50\mu\text{m}$ and (b) etching result showing graphene array. The oxygen plasma etching process is followed by fiber removal process in DI water. Arbitrary pattern can be constructed by controlling the movement of an x-y stage.

PROTOTYPE DEVICE TEST

Mask-less lithography processes using electrospun fibers have been demonstrated in the previous session. In this session, experimental results on fabricated working devices are described.

Micro heater via wet-etching

The whole micro heater fabricated by wet-etching method and the device is shown in figure 7(a). It is made of 30nm -thick copper with width of $20\mu\text{m}$ and total length of 20mm . When an electrical current is applied, the heater can heat up accordingly and an infrared camera is used to monitor the temperature and power during the experiments. Figure 7(b) is a sequence of IR photos showing the micro heater under different input power. It is observed that under an input power of 37mW , the substrate temperature reaches 92°C . Figure 7(c) shows the recorded power consumption versus input current and highest temperature versus power consumption.

Figure 7. (a) The micro heater with $20\mu\text{m}$ in width and 20mm in total length is fabricated by the direct-write electrospun fibers with the wet-etching process. (b) Temperature profile of the micro heater with respect to various input currents under an infrared camera. (c) Recorded results of power consumption versus input current and peak heater temperature versus power consumption.

Graphene FET via dry-etching

Graphene structures fabricated by the direct-write lithography process using dry etching have been constructed as channel field effect transistors (FET). In this case, the FET is tested on a p-type silicon wafer with 285nm of thermally grown silicon dioxide working as gate oxide instead of a flexible substrate. First, a CVD grown single layer graphene film is transferred onto the substrate and PEO polymer fibers based near field electrospinning are used to construct channel patterns. The width of the fiber is measured to be around $1\text{--}2\mu\text{m}$. Afterwards, oxygen plasma at 50mW for 5 seconds is performed to etch graphene. The source and drain regions of the FET are patterned using the conventional lithography process in which OCG825 G-line photo resist is used. A lift-off process with 5nm -thick palladium and 100nm -thick gold layer by e-beam

evaporation is followed by PR removal to complete the device fabrication. Figure 8(a) shows the top view optical image of the graphene channel FET. The patterned graphene channel is clearly visible in the image. The electrical test includes I-V sweep between source and drain. As shown in the top of figure 8(b). It is observed that graphene channel with $2\mu\text{m}$ in width and $10\mu\text{m}$ in length has good ohmic contact behavior since graphene is metallic and palladium is used to promote adhesion between gold and graphene.

Figure 8. (a) Optical images of graphene channel FET via the direct-write electrospun fibers using a dry-etching process. The FET is fabricated on silicon wafer with 285nm of thermally grown silicon dioxide as gate oxide. (b, top) The graphene is metallic such that I-V sweep between source and drain shows good ohmic behavior. (b, bottom) Gate voltage is swept showing the typical large area graphene channel FET characteristics.

On the other hand, if the gate voltage is swept from -35V to $+35\text{V}$ while keeping the SD voltage at 0.1V , the FET behaves like a p-type transistor where the Dirac point is observed around $+21\text{V}$. The Dirac point is where the carrier density is almost zero such that the current flow in graphene channel is minimal. These results show

good FET characteristics and imply the patterned graphene of high quality without being damaged by the oxygen plasma process.

CONCLUSION

Direct-write electrospun polymer fibers on flexible substrate have been successfully utilized as the masking materials in the mask-less lithography processes. The near-field electrospinning on flexible and dielectric substrate was achieved by having conductive substrate underneath to achieve pattern line width from sub-micro to micrometers on flexible substrate. It is found that PEO fibers have good adhesion strength on top of Kapton and copper substrates as well as good wet and dry-etching resistance to wet copper etchant and dry oxygen plasma, respectively. As a result, sub-micrometer gaps on a 30nm-thick gold layer, micro heaters made of copper and graphene patterns have all been successfully demonstrated via the electrospun fibers with lift-off, copper wet-etching and oxygen dry-etching processes, respectively. Testing results also confirms basic operations of micro heaters as well as graphene channel based FET. As such, the direct-write electrospun fiber lithography technique could have versatile application on flexible electronics and wearable electronics with possible simple, low-cost and large area processing capabilities.

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