ELECTRICAL CHARACTERIZATION OF PECVD SILICON CARBIDE FOR APPLICATION IN MEMS VAPOR HF SACRIFICIAL RELEASE

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ABSTRACT

This paper reports results from the characterization of dielectric properties and the electrical conduction mechanism in PECVD amorphous silicon carbide (a-SiC) films. We demonstrate that a-SiC is a good dielectric and passivation film for MEMS devices: (i) leakage current density is well acceptable under typical operating voltages (i.e., fields up to 3 MV/cm); and (ii) the films have super chemical inertness and corrosion resistance, can act as excellent etch stop/passivation layer for vapor HF sacrificial release in various type of transducer fabrication, compared to silicon nitride which has poorer selectivity and requires post-cleaning to remove generated particles. This has large significance to the MEMS community.

INTRODUCTION

Silicon dioxide is the most commonly used sacrificial material in MEMS micromachining. Various wet etch release methods had been developed but all require extra steps to prevent release stiction which complicated the whole process, like supercritical or sublimation drying, or the use of self-assembled monolayer to modify surface energy. Recently, HF vapor phase release has had broad attention [1]. One key material directly related to the success of integrating vapor release into the whole MEMS process is the suitable dielectric material as etch stop layer and passivation layer. Silicon nitride and some other thin films had been studied and reported in [2].

The ideal dielectric in this target application needs to be resistant both chemically and electrically. Popular dielectric thin films, like SiO₂ and Si₃N₄, are well understood and extensively used. It is known that primary charge transport mechanisms in these films are Fowler-Nordheim tunneling and Poole-Frenkel emission effects [3-4]. However, these films have limitations for MEMS, where harsh environment-resistant is needed because of exposure to release chemicals during fabrication and corrosive media during field use. SiC has high chemical inertness and corrosion resistance, and is stable at higher temperatures. Hence, it has gained increasing attention in the MEMS community. a-SiC by low-temperature deposition methods like PECVD and Ion Beam Sputtering has been demonstrated in applications such as Cu-Damascene interconnect process, SiOC and SiCN/SiC composite as Cu diffusion barrier and low-k dielectric layer [5], encapsulation layer for MEMS structures [6], or even as MEMS structure layer through doping (n- or p-aSiC) [7]. Although the dielectric breakdowns of SiOC and SiCN/SiC have been investigated [5], little is known about the temperature and field bias stability of and charge transport mechanism in a-SiC.

In this paper, a-SiC is selected as a potential candidate and brought into detailed investigation. Initial HF vapor etch test is demonstrated and the focus is the electrical characterization. The goal is to evaluate the capability of a-SiC in meeting the requirements from integrated process and proper device function.

EXPERIMENTAL

Vapor HF etch test sample

First, the a-SiC films were deposited onto both bare Si and

thermally-grown oxide coated Si wafers at 350°C by PECVD using tri-methyl-silane ((CH₃)₃SiH) as precursor [8]. Sample film thicknesses were designed to range from 50 to 120 nm, to determine minimum thickness required for achieving pin-hole free high integrity film. The oxide under the a-SiC can help to reveal the presence of pin holes and bare Si monitor wafer was used for more accurate film thickness and stress measurement. The vapor HF etch system used is commercially available PRIMAXX-CET25. Some simple polysilicon test structures were patterned on top of the a-SiC layer for vapor HF exposure to test the etch stop layer concept.

Electrical test sample preparation

Metal-insulator-semiconductor (MIS) capacitor test structures with various sizes on the same wafer were designed for I-V and C-V testing. Thin film intrinsic properties were evaluated using small features sized 10x10μm² and 50x50μm², while larger ones up to 1000x1000μm² were used to capture defects and estimate defect density from the wafer yield point of view. The fabrication started with 6-inch N(100) silicon wafers coated with 1.3μm thermally-grown silicon dioxide, followed by 250nm thick LPCVD phosphorous -doped poly-Si (Rs of 25Ω/□), which was patterned to form the bottom electrode. Then, the a-SiC capacitive dielectric of 120nm was deposited with ≤5% cross wafer non-uniformity. Temperature annealing was performed on select wafers. The residual stress of these films changed from as-deposited low compressive (~ -150MPa) to low tensile (~ 24MPa) after 450°C anneal and about 315MPa after 1150°C anneal. Contact windows were patterned using SF₆/CHF₃ based plasma etch through the a-SiC thin layer to connect the metal probe pad to the bottom poly-Si electrode. AlCu(1%Cu) of 1μm by sputtering was coated on top of dielectric and patterned to form top electrode as well as the final probe pads. LPCVD standard stoichiometric Si₃N₄ (stdNitride) and Si-rich silicon nitride (LSN) films were included in this investigation for comparison.

CASCADE probe station with temperature controlled chuck was used to run wafer level probe, Agilent B1500A semiconductor device analyzer was used to perform C-V and I-V.

RESULTS AND DISCUSSIONS

Vapor HF etching

It is found that the a-SiC film with thickness less than 80nm does have some pin holes, while 120nm thick film is pin-hole free. Thickness measurement after continues 24 hr vapor HF exposure confirms no detectable film loss, indicating extremely low etch rate. The simple test structure wafer with patterned poly-silicon on top of the a-SiC and silicon dioxide beneath it was etched in vapor HF for 30mins. The resulting SEM image (Figure 1) shows a-SiC functioning well in protecting underneath films. As a comparison, Figure 2 presents a silicon nitride blank film after exposed to vapor HF for the similar amount of time. Besides significant thickness loss, lots of etch by-products (residuals) remain on the surface and post treatment clean step is required.

Figure 1: Tilted view of a cross-sectional scanning electron micrograph: a-SiC film of about 120nm is used in this simple test structure wafer, under vapor HF exposure for 30mins, the SiO₂ film underneath the a-SiC is well protected.

Figure 2: Scanning electron micrograph of a blanket coated silicon nitride film after vapor HF etch and lots of etch residuals remain on the film surface which requires post-treatment to clean.

Capacitance drift

For both temperature and voltage bias drift tests, five different films including PECVD as deposited a-SiC, 450°C and 1150°C annealed a-SiCs, and LPCVD standard silicon nitride (stdNitride) and silicon-rich low stress nitride (LSN) were probed. The tests evaluate the dielectric film stability with the common bias conditions. Figure 3 is a bar chart illustrating capacitance drifts from small signal C-V measurement with DC voltage bias sweeping from -25V to +25V. Both as-deposited and 450°C annealed a-SiC have a much lower drift (~30ppm/V) compared to the others; LSN exhibits the largest drift of ~230ppm/V. The 1150°C annealed SiC shows higher drift than as-deposited and 450°C annealed a-SiC, but close to stdNitride (~100ppm/V); film shrinkage and dielectric permittivity change induced by very high temperature annealing are thought responsible. Figure 4 shows temperature bias (0°C to 150°C) dielectric stability results, again, it

is observed that as-deposited and 450°C annealed a-SiC samples had lowest drift of about 16 ppm/°C, while other 3 films exhibit 3-4 times higher drifting.

Figure 3: Capacitance drift determined from C-V measurement under a voltage bias sweeping from -25V to +25V. a-SiC annealed at 450°C is noted as SiC-450C. a-SiC annealed at 1150°C is notes as SiC-1150C.

Figure 4: Capacitance drift determined from C-V measurement under a temperature bias from 0°C to 150°C.

Leakage current density

I-V measurement was conducted with voltage stepping from 0 to 79V (instrument limit). The leakage current from films with different thicknesses under voltage bias was converted to the current at bias electric field for comparison. Figure 5 presents field dependence of leakage current density; stdNitride exhibits the best breakdown performance (>6MV/cm), followed by the 450°C annealed a-SiC, which has the 2nd highest breakdown field among all (>3MV/cm); LSN has the highest leakage (breakdown <1MV/cm), while as-deposited and 1150°C annealed a-SiC are in the middle (~2MV/cm). From both dielectric capacitance drift and leakage performance, it is shown that 450°C anneal process help a-SiC (deposited at 350°C by PECVD) to enhance dielectric property by annihilating defects, but the very high 1150°C anneal is thought to distort the film to some extent and some new defects might be generated so that the dielectric stability and leakage performance became poorer.

Figure 5: Field dependence of leakage current density.

Conduction mechanism study

The Poole-Frenkel charge transport model [4] can be used to describe a bulk limiting field enhanced thermal ionization of the trapped electrons (illustrated in Figure 6). In the model, J is the current density, E is the electric field, Φ_B is the barrier height, ϵ is dynamic permittivity which equals to $\epsilon_0\epsilon_D$, ϵ_D is dynamic dielectric constant, C_1 is a constant to be fitted.

Figure 6: Illustration of Poole-Frenkel charge transport model: bulk limiting field enhanced thermal ionization of trapped electrons.

Figures 7 & 8 show the samples' temperature and field dependence on leakage current density. To check the suitability of the Poole-Frenkel emission model to the sample films under investigation, the raw data from I-V measurements at various temperatures were reformatted to be plotted as $\ln J$ vs. $1/T$ and $\ln(J/E)$ vs. $\sqrt{E}$, respectively. This way, the rearranged linear equations (1) and (2):

$$\ln J = \ln C_1 E + \left[-\frac{q}{k} \left(\Phi_B - \sqrt{\frac{qE}{\pi\epsilon}} \right) \right] * \frac{1}{T} \quad (1)$$

&

$$\ln \left(\frac{J}{E} \right) = \left[\ln C_1 + \left(-\frac{q\Phi_B}{kT} \right) \right] + \left(\frac{q}{kT} \sqrt{\frac{q}{\pi\epsilon}} \right) * \sqrt{E} \quad (2)$$

from Poole-Frenkel model can be used for parameter fitting. The linear regions of the plots identify conditions in which charge transport in a-SiC is also governed by Poole-Frenkel emission. At higher fields, an expected competing mechanism (i.e., phonon assist tunneling) is not strong because no linear region was present by plotting leakage current density as a function of the square of the electric field as suggested in [9]. Through least-square fitting, trap barrier height (Φ_B), dynamic dielectric permittivity (ϵ_D), and trap density and mobility related factor (C_1) are determined and summarized in Table 1. Data from stdNitride and LSN show good agreement with those reported in [10]. The barrier height data from three a-SiC samples correlates to our previous explanation on as-deposited and annealed film relative dielectric stability and bias drifting.

Figure 7: Constant field (~ 6.4 MV/cm for stdNitride and SiC-450C, and 4.5 MV/cm for LSN, SiC, and SiC-1150C) leakage at various temperatures. Linear least squares fits to the data in the 75–150°C range. The electric field for each film was chosen to correspond to conditions in which Poole–Frenkel effect is active.

Figure 8: Poole–Frenkel characteristic at 75°C (348 K). Film thicknesses are 70–120 nm. The high field tail on the LSN sample is due to current constraint. The straight lines represent least squares fits to the linear regions of the data.

Table 1: Extracted constants for various films from P-F model fitting. Data in “()” is from [10].

	StdNitride	LSN	SiC	SiC-450	SiC-1150
C_1	1.26e-06 (1.44e-05)	6.70e-04 (2.75e-04)	9.60e-04	1.14e-04	6.70e-05
Φ_B	1.05 (1.08)	0.71 (0.69)	1.01	1.15	0.85
ϵ_D	5.60 (5.51)	7.92	3.79	3.79	4.17

A scorecard is summarized (Table 2) for all the five films under investigation in this work to reflect figure of merit in both dielectric and vapor HF etch stop functions.

Table 2: Scorecard of electrical/chemical characteristics of the films under investigation.

films	Leakage /Breakdown	Capacitance drift at bias	Vapor etch stop	HF
stdNitride	+++ Best	-	---	
LSN	--	--	++ Good	
SiC	+	++	+++	
SiC-450	++ Good	+++ Best	+++ Best	
SiC-1150	-	--	++	

CONCLUSION

Amorphous silicon carbide by PECVD is evaluated as a potential etch stop material for application in MEMS vapor phase sacrificial release. The initial etch test does show inertness of a-SiC film to the aggressive etchant. In order to verify if it can be integrated into real device for proper function, dielectric characterization including leakage current and capacitance drift under thermal and electrical field bias are conducted. Furthermore, the study on electron conduction mechanism improves the understanding of this new dielectric material intrinsically. It is found the a-SiC film after 450°C annealing performed best with very low bias drift and good breakdown performance and is suggested to be used in MEMS or MEMS/CMOS co-fabrication process.

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