NUMERICAL MODELING AND EXPERIMENTAL VERIFICATIONS OF SINGLE-STEP, DEPOSITION-FREE, HERMETIC SEALING USING SILICON MIGRATION

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ABSTRACT

We present, for the first time, a silicon-migration-based process for sealing release thru-holes in single crystal silicon (SCS), its detailed numerical modeling and evaluation of the hermetic seal. Utilizing silicon migration at 1100-°C in a 10-Torr hydrogen ambient, we successfully formed 2.6- μm - and 1.85- μm -thick, continuous, hermetically sealing membranes from 3- μm -thick SCS layers with two different perforation patterns. To understand and model the process, we developed a 3-D simulator and investigated over 300 release-hole designs. Our simulator predicted the final membrane geometries within 10% of experimental measurements. The quality of the hermetic seals was also robust: 90% of the sealed cavities maintained their initial pressure of 10-Torr over 210 days.

INTRODUCTION

Single-step, wafer-scale vacuum packaging can greatly simplify packaging processes for MEMS/NEMS, improve device reliability, and reduce production costs. Previously reported deposition-based approaches leave reactive gases and unintended material deposition within the encapsulated cavities [1], limiting their application. Silicon migration presents an alternative possibility for sealing release holes that avoids these problems.

Silicon migration is a phenomenon that minimizes the surface energy of SCS through physical migration of surface atoms and occurs in various reducing/inert environments at high temperatures (>850°C) [2-4]. This phenomenon can lead to significant 3-D shape transformations, including the splitting or joining of surfaces. Additionally, the phenomenon has been shown to work with high uniformity [2]. So far, sealing of trenches, but not thru-holes, has been considered possible and demonstrated [2,4]. Inspired by our detailed simulation work, we successfully transformed release thru-holes in SCS into stable, continuous membranes. Potential application to hermetic packaging is depicted in Figure 1.

Figure 1: Conceptual sketch of hermetic packaging application.

SIMULATION, DESIGN AND FABRICATION

Using our 3-D silicon-migration simulator [4], we studied the outcomes for 341 release-hole designs. We observed three salient features of the final structures: (1) thickness reduction in the sealed region relative to the un-patterned region; (2) step height at the region boundaries; and (3) trapped voids within the sealed membrane for certain designs (Figure 2).

Figure 2: Transient simulation of release-hole-array (0.62 μm diameter, 1 μm pitch, 3 μm thick layer) evolution.

Varying the hole's diameter-to-pitch ratio from 0.2 to 0.8 and the thickness-to-pitch ratio from 1 to 3 in simulation showed: (1) the number of trapped voids increased with the thickness-to-diameter ratio (Figure 3a dashed line); (2) very large trapped voids coalesced with their neighbors to form continuous cavities within the membrane (Figure 3a top right); and (3) as the diameter-to-pitch ratio increased, the functional dependence of final step height on thickness-to-pitch ratio became stronger (Figure 3b).

Figure 3: Summary of simulation results for 341 designs.

For experiments, we selected two starting patterns: an array of circular (0.62- μm diameter, 1- μm pitch) and an array of square (0.99- μm width, 1.5- μm pitch) holes in a 3- μm -thick. Figure 4 describes our process flow.

Figure 4: Fabrication process: (a) Oxidize SOI wafer and pattern array of release holes, (b) Etch pattern through 3 μm device layer, (c) Release structure in HF, (d) Induce silicon migration at 1100°C for 40mins in 10-Torr H_2 to seal release holes. Various temperature-time products will work because the final outcome of shape transformation depends on total thermal budget.

RESULTS AND DISCUSSION

SEM images before and after migration confirmed the formation of continuous membranes from the perforated structures (Figure 5). A tilt-angle-compensated side view taken at 80° closely resembled the cross-sectional profile predicted by our simulator (Figure 6).

Figure 5: SEM images: Top views of circular release holes (a) before silicon migration, (b) after migration. The latter SEM clearly shows the formation of a continuous top surface.

Figure 6: SEM at 80°-tilt view confirms the thickness difference between initial device layer (2.98 μm) and sealed region (2.60 μm). It also shows a faint projection of the trapped voids.

The release holes were sealed in a 10-Torr environment, resulting in ~750-Torr difference across the sealed membrane in atmosphere ambient. We used a white-light interferometer to characterize the pressure differential induced membrane

deflection (Figure 7) and calculated the membrane thickness [5]. Membrane thicknesses and step heights (AFM measurement) were within 10% of the simulation values (Table 1).

Figure 7: Deflection measurement (white light interferometer).

Design	Circular	Square
# of devices	5	5
Step height (sim)	0.23±0.02 μm	0.63±0.05 μm
Step height (exp)	0.26±0.02 μm	0.65±0.06 μm
Thickness (sim)	2.50±0.10 μm	1.70±0.16 μm
Thickness (exp)	2.6 μm	1.85 μm

Table 1: Comparison of simulation (sim) and experimental (exp) results. Results were within 10%.

To study the hermetic seal quality, we stored the membranes at an atmospheric pressure and monitored for deflection change: over 210 days, 9 out of 10 structures maintained their initial cavity pressure.

CONCLUSIONS

Using silicon migration, we have sealed release holes to form stable, hermetically sealed cavities. Using our 3-D simulator, we have accurately modeled experimental results and also investigated a broad range of design parameters to establish design/process guidelines. In the future, our technique can be combined with wafer bonding to create commercial-quality, hermetic seals for micro-/nano-structures at the wafer-scale.

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