VERTICALLY ALIGNED SILICON NANOWIRE ACTUATORS AND SWITCHES

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ABSTRACT

We report the development of novel, vertically aligned silicon nanowire electrostatic switches targeting 1V operation and 1 nanosecond switching times for future computing applications. Analytical and finite element models show that it is possible to obtain 1V operation and nanosecond switching. The source, gate, and drain electrodes of the nanoswitch are fabricated using standard MEMS processes. Silicon nanowires are subsequently grown by chemical vapor deposition. Electrostatic actuation of a Si nanowire in a two-terminal configuration was demonstrated *in situ* in a scanning electron microscope, and preliminary electrical tests showed repeated actuation of nanowires with an on-state resistance of $\sim 342 \text{ M}\Omega$.

INTRODUCTION

As the push towards faster, more powerful electronics continues, scaling of metal oxide semiconductor field-effect transistors (MOSFETs) along Moore's Law leads to significant design challenges, including on state losses and leakage currents associated with an ever-thinning gate dielectric [1]. These lead to severe thermal management problems that must be overcome by novel approaches at the device and system level. Here we propose a small footprint, low power consumption, and mass producible nanoelectromechanical switch design that offers an innovative solution to the above-mentioned problems. Switches based on nanoelectromechanical systems (NEMS) in particular have unique properties such as a physical air gap between source and drain that have the potential to alleviate many of the power losses in solid-state switches. Furthermore, they may enable all mechanical computing or the ability to create computers without the need for any cooling by allowing the active devices to operate at high temperature.

Inorganic nanowires are of particular interest in high frequency mechanical switching applications owing to the fact that their relatively high elastic modulus and small dimensions provides a high resonant frequency (Table 1). Indeed, the potential for nanowire/tube NEMS devices for GHz operation has been studied theoretically. Kinaret *et al.* [2] showed that horizontally-aligned carbon nanotube triode devices have the potential to switch in the nanosecond time regime. Jonsson *et al.* [3] also showed that such device could operate as GHz switches, though they also calculated that there is a non-linear resonant behavior at such frequencies.

Table 1. Calculated resonant frequency for a silicon and silicon carbide cantilever rod with various dimensions.

Resonator material	Dimensions (L (nm), r (nm))			
	1000, 60	300, 30	100, 10	30, 3
Silicon (E=108 GPa, $\rho=2.3 \text{ g/cm}^3$)	110 MHz	636 MHz	1.9 GHz	6.36 GHz
Silicon Carbide (E=400 GPa, $\rho=3.2 \text{ g/cm}^3$)	190 MHz	1 GHz	3.1 GHz	10 GHz

There have been few published experimental works on nanowire/tube switches. Ke and Espinosa [4,5] demonstrated a bi-stable NEMS device based on multi-walled carbon nanotubes by *in situ* SEM analysis, whereas Cruden and Cassell [6] demonstrated a vertically oriented carbon nanofiber-based device. We note that in

those works the nanostructures were actuated using external probes or structures, not by integrated microelectrodes. Blick and co-workers [7] fabricated silicon nano-pillar structures using top-down nanofabrication and demonstrated that field emission can be useful mechanism in identifying their resonant behavior. On the other hand, horizontally aligned carbon nanotube NEMS switches were demonstrated by Cha *et al.* [8], and in-plane silicon nanowire switches were shown by Li *et al.* [9].

Here we propose the use of integrated, vertically aligned silicon nanowire devices for switching applications. **Figure 1** shows a schematic of our device structure. The electrodes are fabricated using standard MEMS/microfabrication methods, whereas the nanowires are synthesized using bottoms-up catalytic growth processes. In this work we show that such devices structures have potential to act as high-speed switches, and demonstrate DC actuation of integrated two-terminal Si NW devices.

Figure 1: Schematic of the proposed electrostatically-actuated nanoelectromechanical switch consisting of gate, drain, and source electrodes and a nanowire actuator in (a) the open state and (b) closed state.

EXPERIMENTAL PROCEDURE

Device Fabrication

The nanoswitch fabrication process is shown in **Figure 2**. We are interested in both two and three-terminal devices. Two-terminal devices have only gate and drain terminals and were used to study the electrostatic actuator performance. The 2-terminal device fabrication process begins with a degenerately-doped Si <111> substrate. A 0.5-1 μm silicon dioxide film is first grown on the substrate. Then a thin (100-300 nm) metal layer, typically titanium or chromium, is deposited on top of the oxide. This metal film both acts as a mask for reactive ion etching (RIE) of the oxide film, and as the top contact/gate electrode for the device. The metal film is wet etched to form the electrode structure. RIE is then used to etch the SiO_2 film down to the Si substrate. A 5-10nm thin Au catalyst film is shadow evaporated on the substrate for growth of the Si NWs. Then the substrate is placed in a 5" horizontal chemical vapor deposition (CVD) reactor (Tylan) capable of growth on 4" wafers. Silicon nanowires are grown using the vapor-liquid-solid growth mechanism [10]. Typical growth times are 1-5 minutes. P-type doping in the nanowires has been confirmed in separate experiments [11,12].

Testing & Characterization

Electrical testing was performed using a semiconductor parameter analyzer (HP 4154B) in both DC and pulsed modes. The

devices were characterized in a field emission scanning electron microscope (LEO 1530VP) equipped with an electrical feedthrough. *In situ* actuation of Si NWs in the SEM was performed by connecting probes through the electrical feedthroughs and connecting the devices to a DC power supply.

Figure 2: Schematic of nanoswitch fabrication process. (a) Conventional photolithography and liftoff methods are used to build a film stack comprising (top down) Au/Ti/SiO₂/Au/SiO₂ layers (for 3 terminal switch) or Ti/SiO₂ layers (for 2 terminal switch); (b) Shadow evaporation produces a thin (5~10 nm) Au film as a catalyst for nanowire growth. (c) Vertically oriented nanowires are grown by CVD method.

RESULTS AND DISCUSSION

Device Performance Modeling

An analytical model was first used to establish the basic geometrical parameters required to fabricate NEMS switches that can operate in the GHz regime with low operating voltages. A silicon nanowire with circular cross section was assumed to have bulk elastic constants ($E = 108$ GPa) and density (2330 kg/m³). The first resonant mode (f_r) was evaluated using the following equation:

$$f_r = \frac{3.52}{2\pi} \sqrt{\frac{EI}{\rho_{\text{length}} l^4}} \quad (1)$$

where I is the area moment of inertia ($0.25 \cdot r^4$) and ρ_{length} is the density per unit length ($\rho \cdot \pi \cdot r^2$). **Figure 3** shows a contour plot of the expected first resonant mode, from which it is evident that nanowires with diameters on the order of 20-80 nm in diameter and 200-1000 nm in length are required for such high-speed switching applications. The gap required to actuate a silicon nanowire was first evaluated analytically by assuming a uniform load applied to 4/5 of the nanowires (representing the gate, with the upper 1/5 representing the top contact). **Figure 3b** shows the pull in voltages for various wire and gap dimensions. It is found that for a nanowire with a resonance frequency of 250 MHz, a gap between the nanowire and the gate electrode on the order of 5-20 nm is required to achieve 1 V actuation.

Figure 3: (a) Contour plot showing the impact of nanowire radius and length on the first order resonance frequency and (b) contour plot showing the nanowire-gate gap and length for a Si NW with a $f_r = 250$ MHz.

A more detailed analysis of the expected device performance was undertaken using finite element analysis. Five critical factors were investigated: 1) impact of quality factor (Q) on the device performance; 2) Casimir force [13] at the length scales of interest; 3) effect of high surface-to-volume ratio in nanowires on their elastic properties and device performance; 4) effect of additional device parameters such as gate length and the presence of the catalyst particle on the mechanical response; and 5) optimal device geometry required to achieve nanosecond switching times.

Figure 4 shows the effect of Q on open time for the case of no damping, as well as overdamping ($Q = 0.4$) and under-damping ($Q = 8.3$), assuming a nanowire length of 500 nm, a diameter of 50 nm, and a gap of 20 nm. It is noted that no distinction is made here between damping due to the external environment and materials damping due to planar or line defects, grain boundaries, etc. In the case of overdamping, oscillation of the nanowire about the rest position is suppressed, though at the cost of increased open time. When the wire is underdamped the oscillations about the rest position are significant, though this is mitigated by the fact that the actual electrical open time is significantly shorter than the time it takes for the nanowire to initially reach the rest position, and hence the nanowire can be re-actuated to the closed position before settling at the rest position. A Q of 1-3 will thus be preferable for these Si NW devices.

Figure 4: Effect of quality factor on open time for a 500 nm long, 50 nm diameter Si nanowire placed 20 nm from the gate electrode

We also studied the impact of the Casimir force on Si NW NEMS switch devices, which may lead to an additional attractive force between the nanowires and the gate electrode. In the case of two parallel plates, this force (F_c) scales as A/d^4 , and for a sphere in the vicinity of a parallel plate $F_c \propto R/d^3$, where A is the area, R is the radius, and d is the distance between conductors [14]. We calculate a Casimir force of ~ 0.2 nN for our typical device dimensions, which if assumed to act as a point load will lead to a displacement of ~ 2 nm. This displacement will be less for a distributed load, and hence the Casimir force can be neglected for gaps greater than 5 nm.

Surface elasticity has recently been studied theoretically as a possible mechanism by which the elastic constants of a nanostructure can be modified compared to their bulk counterparts [15]. However, a recent study has shown that for silicon the nanostructure must have a critical dimension below 5 nm in order for the surface to significantly impact the mechanical properties of the nanostructure [16]. Since our nanowires have diameters in the range of 40-80 nm, surface elasticity will not be a factor in the devices studied here. Indeed, recent studies of semiconducting and metallic nanowires show that their elastic constants and strength are similar to bulk materials [17,18].

Having ruled out significant contributions of the above non-classical effects to the device performance, the impact of gate length on pull-in voltage ($V_{\text{pull-in}}$) and close time was evaluated. Assuming the device parameters discussed above, it was found that decreasing the gate length from 1000 nm to 700 nm led to an $\sim 24\%$ increase in pull-in voltage and a 20% increase in close time. Therefore, these device parameters will not drastically affect the device dynamics. The impact of the catalyst particle present at the tip of the nanowire, which also acts as the contact material, was also found to have a limited effect on the resonant frequency of a typical Si NW. Indeed by a detailed design of experiments, it was found that close times as low as 1.7 nsec with $V_{\text{pull-in}} = 0.5$ V can be obtained for 1000 nm long, 40 nm diameter nanowires placed 5 nm away from the gate electrode (**Figure 5**). The open time is on the order of 7-10 nsec (depending on Q), but as noted above the nanowire can be actuated prior to reaching the rest position.

Figure 5: Simulated displacement-voltage curve showing $V_{\text{pull-in}} = 0.5$ for a design capable of 1.7 nsec closing time.

Si NW NEMS Device Fabrication

As noted above, we have fabricated two-terminal Si nanowire devices on 4" wafers. In the vicinity of the electrode there are typically many nanowires, though few are close enough to be actuated at low voltages. At present the placement of the nanowires is not deterministic, and various methods are being explored so that nanowires can be placed at well-defined locations 5-20 nm away from the microfabricated electrodes. This fact does not, however, hinder our ability to test the nanowire actuators (see

below). Nevertheless, fabrication of the two-terminal Si NW NEMS actuators on large-area wafers clearly shows the potential of this technology to be mass-manufacturable. A three-terminal process has also been developed and is currently under fabrication. Testing data reported below is focused on two-terminal devices.

Testing

A typical wafer contains ~ 1000 devices; hence autoprobing was used to determine which devices are functional at reasonable voltages. In devices tested to date the pull-in voltage was in the range of 25-35 V, hence we typically observed stiction of the device as evidenced by repeated DC current-voltage (I-V) measurements on a given device. Calculations show that the local temperature at the contact at such relatively high voltage will be several hundred degrees, hence it is not surprising that stiction occurs. Of course, in three-terminal devices the actuation voltage is independent of the source-drain voltage, which will be on the order of 10's of mV. Hence, stiction due to local heating should not be a problem for three-terminal devices.

After autoprobing, functional devices were subject to low frequency pulsed testing and indeed showed actuation above the measured DC $V_{\text{pull-in}}$ and no actuation below $V_{\text{pull-in}}$, though a leakage current was observed (**Figure 6**). The typical on resistance was several 100 M Ω . High speed switching experiments will be performed on future three-terminal devices to assess the switching time and reliability issues that may arise in such nanoscale switches.

Figure 6: Pulsed gate voltage test data showing repeated actuations of a 2-terminal device with pull-in voltage of ~ 27 V. The on-state resistance of the device is ~ 342 M Ω . The off-state resistance is ~ 2080 M Ω , indicating the presence of a residual leakage path, which is currently under investigation. No switching was observed when the device was actuated at 25 V.

We also studied actuation of Si NWs using *in situ* scanning electron microscopy (SEM). **Figure 7** shows that upon application of 10 V, actuation/bending of the NW was clearly observed. Release of the applied voltage did not restore the nanowire to its rest position, indicating stiction between the top electrode and the nanowire occurred.

Figure 7. SEM images of a ~ 38 nm diameter Si nanowire ~ 33 nm away from a gate electrode (a) a 30 degree angle view; (b) top view at 0 V actuation voltage, (c) (top view) after application of a 10V actuation voltage, the nanowire was actuated to contact the gate electrode. After removal of the applied voltage the nanowire remained bonded to the top electrode. The expected pull-in voltage for this device was calculated to be 4.7 V.

CONCLUSIONS

We proposed and demonstrated vertically-aligned silicon nanowire switches. Detailed modeling studies showed that non-classical effects such as the Casimir force and surface elasticity will not impact the performance of these devices, and that it is possible to obtain device designs that can yield low-voltage, high-speed switches. Two-terminal Si NW actuators were fabricated with integrated electrodes on 4" wafers, thus showing the potential of this technology for mass manufacturing. Electrical testing showed repeated actuation of these devices, and actuation of an individual Si NW was observed via *in situ* scanning electron microscopy. Future work is focused on fabricating three-terminal switches and testing their high-speed response and lifetime.

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