SELF-ASSEMBLED 275NM-GAP ELECTRODES FOR CMOS-MEMS RESONATORS AND ITS PRECISION DC CHARGE-BASED CAPACITANCE MEASUREMENT

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ABSTRACT

A self-assembled electrode (SAE) technique and a precise DC charge-based capacitance measurement (CBCM) method are introduced for integrated on-chip characterization of lateral gap MEMS capacitance. A SAE with a 275 nm gap is applied in CMOS-MEMS free-free flexural mode resonators (FMRs) to enlarge input and output capacitive coupling. A 23 dB gain enhancement illustrates the importance of the method. The CBCM method can measure MEMS electrode capacitances down to a few femto-Farads with the existence of large parasitic capacitance to ground. A modified finite-element model verifies the relation between the measured capacitance to the electrode geometry. A temperature stability test demonstrates the SAE can operate in the range of 23-85°C without mechanical clamps.

INTRODUCTION

Over the last four decades, although integrated circuits double in computing power approximately every 18 months without increasing cost per IC, off-chip components are still needed to provide narrow-band filtering and stable reference frequencies. CMOS-MEMS technology is a platform to integrate narrow-band filters and mixer-filters (mixfilters) with active circuitry to realize single chip transceivers. However, several challenges, such as lowering termination resistance (R_T), need to be addressed before their implementation in wireless systems.

In order to form a flat pass-band, microresonators need to be terminated to a R_T proportional to the 4th power of the electrode gap. Air-gap capacitive microresonators need relatively high termination resistance; R_T is 370 M Ω for devices with electrode gaps of 800 nm and Q of 10,000. Lowering R_T to a manageable level for on-chip circuits, for example 10 k Ω , is necessary for integration and requires a smaller electrode gap. In select processes, narrow gaps may be formed with sacrificial layers [1] and with solid-dielectric drives [2]. In CMOS-MEMS, narrow gaps may be achieved by self-assembly of electrodes [3].

Precise characterization of the sensing capacitance in the presence of large parasitic capacitance (C_p) is important in understanding process and design limits. SEM image-based measurement and/or focused-ion-beam sectioning is the most common characterization technique where the capacitive gap and overlapped electrode area are measured and capacitance is extracted from a parallel-plate model. This technique is time-consuming for multiple-device measurement, impossible for automatic testing, and not accurate for sub-micron gaps due to significant geometry and material non-idealities. Within the integrated circuit community, a DC CBCM method has been widely used to measure inter-wire capacitance [4-7], and a bias-dependent technique was later developed to further reduce mismatch errors [8]. This technique is adopted here for the first-time to measure MEMS lateral gap capacitances and to study the temperature stability of SAE.

SELF-ASSEMBLED ELECTRODE DESIGN

Narrow gap electrodes (NGEs) are crucial for increasing capacitive coupling especially for RF-CMOS-MEMS resonator/filter applications. Previously, approximately 500 nm gaps have been achieved with electrothermal gap-closing actuators

operating at 3.5mW power consumption [3]. Shown in Figure 1, a self-assembled actuator (SAAs) achieves electrode movement with no power consumption. The actuator comprises a beam flexure with individual beams made of the dielectric and metal layers in the CMOS. The beam cross section has laterally offset stacks of metal layers to create an embedded residual stress gradient transverse across the beam. After releasing the structures, the stress creates an internal bending moment that moves the device laterally. The final gap is defined by the difference between the initial electrode gap and the stopper gap. The inner-metal layers are offset to one side of the beam for half the beam length and offset to the other side of the remaining half of the beam length. This arrangement generates a guided-end condition that allows multiple beams to be placed in parallel to create a stiffer actuator. Theoretically, the displacement of SAAs is proportional to the square of actuator length and the inverse of the actuator beam width. The optimal beam design for maximizing displacement is discussed in [9].

Figure 1: (a) The schematic of a self-assembled actuator, and (b) the cross-section of the self-assembled actuator at A-A'.

THE DESIGN AND FABRICATION OF CMOS-MEMS FLEXURAL MODE RESONATORS

The FMR topology comprises two free-free beams coupled by supporting tethers, vibrates horizontally on the silicon substrate. It achieves high quality factor due to low anchor loss and low motional impedance with large electrode area, and was introduced for its high-order mode in oscillator applications [10].

The beams are actuated and the displacement sensed electrostatically through lateral air-gap electrodes. The actuating force at the center of each cantilever excites the FMR to move laterally in the x-direction, which generates output motional currents across a DC biased output capacitor. The output motional current is converted into a voltage by passing through the input capacitance of the pre-amplifier. With the assumption of identical input and output electrode geometry, the transfer function of the differential FMR is

$$H(\omega) \approx \frac{-4j\epsilon_0 A^2 V_p^2 G_v}{Kg^4 \left(1 - \frac{\omega^2}{\omega_R^2} + j\frac{\omega}{Q\omega_R}\right)} \quad (1)$$

where ϵ_0 is the permittivity of free space, A is the electrode overlap area, V_p is a DC polarization voltage, G_v is the ratio of the voltage amplification of the amplifier to the input capacitance of the amplifier, K is the equivalent stiffness of the coupled resonators, g is the electrode gap, ω is the frequency of the input signal, and ω_R is the resonant frequency.

Figure 2: CMOS-MEMS flexural mode resonators. (a) Design with SAA electrodes. (b) A close-up view of a stopper and narrow-gap electrode (NGE). (c) Further close-up of NGE where mechanical gap is 172nm, and (d) A FMR fixed gap design.

Figure 3: (a) The 1st and (b) 2nd mode of the CMOS-MEMS flexural mode resonator. A homogeneous Young's modulus of 70 GPa and density of 2200 kg/m³ is assumed.

Figure 4: Cross-sections of CMOS-MEMS micro-machining process: (a) after foundry CMOS processing, (b) after SiO₂ etch, (c) after isotropic etch to release the resonator.

Figure 5: (a) The CBCM circuit diagram. (b) Timing diagrams of the three non-overlapping clocks (CK_p, CK_n, and CK_x). (c) An implemented CUT with a SAA narrow gap.

Figure 2 (a) shows the SEM of a FMR with SAA electrodes, (b) and (c) illustrate close-up views of stoppers and NGEs, respectively and (d) is the SEM of a fixed-gap (FG) FMR for comparison. The finite-element analysis results of the first two resonant modes are illustrated in Figure 3, where the pole splitting due to the stiffness of supporting tethers is observed. This effect is employed to construct the bandpass response.

As illustrated in Figure 4(a), the post CMOS micromachining process [3] starts with a foundry-fabricated four-metal 0.35 μm CMOS chip. A CHF₃:O₂ RIE removes all of the dielectric stacks which are not covered by top metal layers as shown in Figure 4(b). After the dielectric etch, a timed isotropic/anisotropic silicon etch releases the resonator and its SAA electrode simultaneously, resulting in Figure 4(c).

DC CHARGE-BASED CAPACITANCE MEASUREMENT

The bias-dependent CBCM method, shown in Figure 5, requires two transistor switches, a DC precision current meter, and three clocks [8]. The capacitor under test (CUT) is charged and discharged through control of two transistor switches, M1 and M2. The CUT capacitance is extracted by subtracting two charging-current readings of the DC current meter with different amplitudes of the clock CK_x. In the first measurement cycle, CK_x is ground and the average current reading is I_1 . In the second measurement cycle, CK_x is ΔV_{CK_x} and the average current reading is I_2 . The extracted capacitance is

$$C_x = \Delta I_{avg} / (f \cdot \Delta V_{CK\_x}) \quad (2)$$

where the $\Delta I_{avg} = I_2 - I_1$ is the difference of measured DC currents, and f is the clock frequency. This differential technique eliminates errors from charge injection into C_p , even if C_p is orders of magnitude larger than CUT. The limitation on the C_p to CUT ratio is defined by the resolution of DC current meter, and is about 300X for the Agilent/HP 4140B used in the measurements.

Figure 6: Measured frequency response of the (a) 1st and (b) 2nd mode of CMOS-MEMS FMRs with SAA and fixed electrodes at four different polarization voltages. The input power is 0dBm. Pressure is less than 50mTorr. Feedthrough is subtracted from the data.

EXPERIMENTAL RESULTS

Figure 6 provides the measured results of FMRs with self-assembled and fixed gaps. The two devices have identical resonator designs with the parameters listed in Table 1. An on-board unity-gain circuit buffered the output signal, which is then measured by a network analyzer. Comparing the plots in Figure 6 (a) and (b), a 23 dB enhancement in S_{21} occurred between the average 274 nm SAA gap, in Figure 2(c), and the fixed gap of 1.1 μm . This improvement is lower than the analytic prediction of 48 dB and the discrepancy is believed to be the result of low G_v due to the larger parasitic capacitance loading for the SAA electrodes and the non-ideal sidewall (i.e. not vertical profile) of the NGEs. The self-assembled sidewall capacitance is also limited by a 50-100 nm thick sidewall polymer deposited during the CMOS-MEMS processing.

To characterize the narrow-gap electrode capacitance, SAA CUTs with CBCM switches were implemented as illustrated in Figure 7(a-d). The finite-element method (FEM) was employed to compare the simulated capacitance from the physical geometry with the extracted CBCM capacitance. Two sidewall geometries were compared: the simplified model geometry with parallel-sidewall electrodes in Figure 8(a) and a modified model with process related non-ideality, including top-metal slops, sidewall polymers, inner-metal pull-ins, and bottom-widening gaps, shown in Figure 8(b). The modified model geometry is extracted from a series of side-view SEMs of electrode sidewalls, with one example

Table 1: SAA FMR parameters and characteristics

Items	Parameters
Resonator (Beam) width	4 μm
Resonator (Beam) length	53 μm
Electrode length	20 μm
Electrode height	4.8 μm
Tether length	13 μm
Tether width	0.5 μm
SAA length, single side	100 μm
Polarization voltage, V_p	27-54 V
Pressure	< 50 mTorr
Resonant frequency, 1st & 2nd mode	7.65 & 7.68 MHz
S_{12} (w/on-chip amp.), 1st & 2nd mode	-23.6 & -20.3 dB
Q, 1st & 2nd mode	1577 & 1652

Figure 7: (a) The layout of the switches and SAA CUT. (b) The SEM of CUT. (c) The close-up view of a stopper for a 450 nm gap defined by the stub length of d_s . (d) The SEM of a narrow gap of about 230 nm.

Figure 8: (a) The 2-D FEM (COMSOL) capacitance model of parallel narrow gap electrodes. (b) The modified capacitance model with geometry extracted from (c). (c) The SEM of close-up view of electrodes.

Figure 9: The comparison of CBCM extracted capacitance value and FEM simulated capacitance with simplified and modified models.

Figure 10: (a) CUT value and (b) parasitic capacitance C_p for three different test chips labeled as R18, R19 and R20, extracted directly from CBCM measurements. The calculated $\pm 10\%$ region is based on the average capacitance at room temperature.

given in Figure 8(c).

Seven CUTs were tested with gaps ranging from 218nm to 564nm. The CBCM extracted capacitances and the corresponding FEM results with the two different models are compared in Figure 9. The CBCM extracted capacitance matches the simulations from measured sidewall geometry. The conventional parallel-plate model overestimates the capacitance by around 80% for the narrowest gaps.

A temperature stability test on SAA devices was conducted on three CUTs. The results in Figure 10 demonstrates that the SAA devices can operate up to 85 °C, which fulfills the temperature requirements of commercial and automotive standards. In addition, by adding mechanical clamps to constrain the pull-back electrode movement for high temperature operation, the upper operational limit could be extended further.

CONCLUSIONS

This paper presents a self-assembled capacitive electrode to enlarge input/output capacitive coupling and its application in CMOS-MEMS flexural mode resonators (FMRs). The 275 nm self-assembled gap provides 23 dB gain without consuming actuation power. It should be possible to achieve even smaller gaps with future stopper designs and minimization of sidewall polymer formation. The DC charge-based capacitance measurement method was demonstrated through detailed FEM modeling to provide an accurate measure of the femto-Farad sidewall capacitance even with the existence of 9.6 times larger parasitic capacitance to ground. The temperature stability test demonstrates the SAA electrodes can operate within the range of 23-85°C. The high temperature limit could be extended with the help of mechanical clamps. The self-assembled electrodes and CBCM method are integrated on-chip directly, require little or no addition equipments, and therefore reduce process and testing complexity, respectively.

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