LOW-TEMPERATURE (<300°C) LOW-STRESS SILICON CARBIDE SURFACE MICROMACHINING FABRICATION TECHNOLOGY

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ABSTRACT

A low temperature (<300°C), low-stress micro electromechanical systems fabrication process based on a silicon carbide structural layer is presented. A Hexoloy-SG target enables low-temperature DC sputtering of amorphous silicon carbide. The process is designed for low-cost implementation and CMOS post-integration stemming from chemical and thermal compatibility. Process flow, deposition, etching, and stress control are discussed, and the electrical transfer characteristic of a fabricated resonator device is reported to demonstrate a process application.

INTRODUCTION

Historically, silicon has been the structural layer of choice for microelectromechanical systems (MEMS) fabrication as it is commonly used by the semiconductor industry. However, the mechanical properties of silicon are not optimal for many applications, and other materials such as silicon carbide (SiC) are being developed to improve performance, enhance reliability, and enable new functionalities in MEMS. In contrast with silicon, SiC exhibits higher acoustic velocity, higher fracture strength, hardness, and desirable tribological properties [1]. In addition, SiC can operate at higher temperature, and withstand corrosive and erosive environments, which makes this material suitable for use in harsh [2] and biological [3] environments. These factors, along with the maturation of deposition and patterning techniques, make SiC a natural choice for next generation MEMS processing.

Adding MEMS capabilities to integrated circuits processes (such as CMOS) is very desirable in many sensing and control applications. However, low-temperature processing of SiC is non-trivial, and most SiC MEMS processes do not intrinsically lend themselves to CMOS integration (<400°C). This work demonstrates for the first time a metallized, low-temperature, low-stress amorphous silicon carbide (*a*-SiC) surface micromachining process for the fabrication of micro electromechanical systems. It is designed to be CMOS-compatible, both chemically and thermally [4].

This paper outlines the process flow, and discusses the deposition and etching of SiC. Several devices are shown, and the measured characteristics of a microelectromechanical (MEM) resonator are reported to demonstrate the capabilities of this CMOS-compatible fabrication process.

DEPOSITION TECHNOLOGY

The technology is based on the use of Hexoloy-SG, which is an electrically conductive sintered SiC alloyed with 6 wt% carbon. This material permits DC sputtering of thin films at relatively high rates and low temperatures, with simple implementation and low cost. Residual stresses of the films can be tuned by changing the argon pressure during deposition.

SiC deposition has generally not lent itself to be CMOS compatible, because of the high temperatures involved (>800°C) in traditional polycrystalline SiC (poly-SiC) chemical vapor deposition (CVD) [5-7]. Plasma enhanced CVD (PECVD) has been used to deposit *a*-SiC at reduced temperatures [8], but annealing at around 600°C was required to reduce film stress [9]. Amorphous SiC has similar properties to poly-SiC, with variations in properties

such as the Young's modulus [10]. Low-temperature PECVD of *a*-SiC tends to form hydrogenated films (*a*-SiC:H) with lower Young's modulus than sputtered *a*-SiC [10]. Table 1 compares different SiC types, with poly-silicon as a reference. In accordance with the Hexoloy-SG properties [11], nanoindentation analysis of the DC sputtered SiC thin films yielded a higher Young's modulus than that of poly-silicon and other *a*-SiC films [12].

Table 1: Properties of different materials.

Material	Dep. type	Temp. (°C)	Young's mod. (GPa)	Acoustic Velocity (km/s)
poly-Si	LPCVD	1050	169 [13]	8.52
3C-SiC	LPCVD	900	401 [14]	11.18
<i>a</i> -SiC	RF Sput.	-	231 [10]	8.48
<i>a</i> -SiC:H	PECVD	600 (anneal)	153 [10]	6.90
This work (<i>a</i> -SiC)	DC Sput.	<170	258 [12]	9.50

THE PROCESS FLOW

The process provides a total of three metallic layers for routing signals and electrostatic actuation. Polyimide is used as the sacrificial layer in this surface-micromachining process. A layer of chromium is used as an etch stop for the SiC plasma etch, and also protects the underlying polyimide from fluorination [15]. Finally, a thick aluminum layer is available to lower the resistivity of interconnects, and to create bonding pads.

Figure 1 illustrates the process flow to create clamped-clamped beam resonators. A DC sputtered 60 nm aluminum layer is wet etched to pattern the bottom electrode (Fig. 1a). Subsequently, a variable thickness (>200 nm) polyimide sacrificial layer is spun-on, cured, and patterned to form the anchors (Fig. 1b). Another 60 nm aluminum layer renders the bottom surface of the SiC conductive (Fig. 1c).

Fig. 1: Process flow for a clamped-clamped beam resonator.

Fig. 2: (a) A released MEM inductor with two isolated conductive layers, and (b) a MEM switch with signal/actuation isolation.

An 80 nm chromium etch-stop layer is then DC sputtered (Fig. 1d) followed by the 2 μm SiC structural layer. The etch-stop protects the underlying polyimide from fluorination for subsequent release [15]. The SiC is then patterned through NF_3 reactive ion etching (RIE) (Fig. 1e). Finally, a wet etch removes the etch-stop (Fig. 1f), then oxygen plasma releases the structures (Fig. 1g). Not shown in Fig. 1 is an aluminum layer that can be added to the process flow on top of the structural layer. This interconnect layer can be patterned after the SiC etch, or be self-aligned to the SiC layer, by patterning it after the chromium mask.

The low-temperature SiC process allows for the deposition of a metal underneath the SiC, and hence provides the ability to route signals both on top and bottom of the structural layer. This yields interesting design advantages. For example, electrical isolation of signals across the structural layer is possible, such as in the released inductor shown in Fig. 2a, or as depicted in Fig. 2b, where this is exploited in a MEM switch to isolate the actuation and signal voltages.

DETAILS OF DEPOSITION AND ETCHING

Characterization of SiC thin films

Thin films deposited by physical or chemical vapor deposition are invariably subjected to intrinsic residual stresses. The choice of DC magnetron sputtering to deposit *a*-SiC permits good control of film stress. Figure 3a shows the effect of the argon pressure during deposition on the biaxial residual stress in the film. The stresses reported on this graph were measured using the wafer-curvature technique. The measured stress of the deposited film goes from compressive to tensile at a working pressure of approximately 6 mTorr. This is consistent with previously reported studies of DC sputtered Hexoloy-SG thin films [16]. Repeated depositions of films at this condition confirmed stress values of ± 50 MPa. Fracture due to tensile stresses of these magnitudes is not a concern for SiC; however, compressive stresses of tens of megapascals can lead to buckling in slender microfabricated beams. Therefore, the deposition pressure is selected to ensure a low level of tensile stress in the film. Figure 3b shows a scanning electron micrograph of doubly-clamped SiC structures confirming the absence of stress-induced buckling or fracture.

Although the deposition was performed at room temperature with no external heating, the substrate experienced an increase in temperature due to ion bombardment during film growth.

By using adhesive temperature labels on the wafer, the maximum temperature of the substrate was monitored continuously during the deposition of a 2 μm thick SiC. The maximum temperature experienced by the substrate was below 170°C, which is significantly lower than in chemical vapor deposition processes. Furthermore, the film can be grown in stages without vacuum break to lower substrate heating. A growth rate of 75 nm/minute was achieved at a deposition power of 2 kW. This is significantly higher than the 18-30 nm/min reported for *a*-SiC RF sputtering [17, 18].

Energy-dispersive X-ray (EDX) spectroscopy was used to obtain an approximate value for the SiC films' atomic composition. The incident electron beam had an effective volume of interaction which is typically on the order of the thickness of the films used in this work. Therefore, the SiC films were deposited on aluminum substrates to prevent any convolution of silicon signals from the films and substrates. Calibrated measurements yielded an average atomic composition of 47.7% silicon, 51.6% carbon, and 0.7% oxygen. The carbon to silicon ratio of 1.08 is consistent with expectations based on deposition from a Hexoloy-SG target.

The resistivity of the SiC was investigated by probing isolated micro-striplines using DC needles. A lower bound of 40 M Ω was established for the electrical resistance using a multimeter. The corresponding bound on the bulk resistivity of the film is $\sim 550 \Omega\cdot\text{cm}$. For comparison, the value reported in [16] for the electrical resistivity of deposited Hexoloy thin films was $\sim 2000 \Omega\cdot\text{cm}$.

Fig. 3 (a) Biaxial residual stress of an SiC film versus working pressure at 2 kW of power (error bars indicate standard deviation). (b) Scanning electron micrograph of released stress-free clamped-clamped SiC beams.

Fig. 4 Atomic force microscopy of the SiC film surface indicating an RMS roughness of ~ 20 nm.

X-ray diffraction (XRD) analysis ascertained the amorphous nature of the film. The surface morphology of the SiC films was examined using electron microscopy and atomic-force microscopy (AFM). The image from an AFM scan of a $1.5 \mu\text{m} \times 1.5 \mu\text{m}$ area is shown in Fig. 4. The measured RMS roughness ranges from 10 to 30 nm from a series of AFM scans. A remarkable feature of the surface is the presence of irregular mounds, which has also been previously reported for Hexoloy thin films [16].

Reactive-Ion Etching of SiC

SiC patterning is more difficult than other commonly used materials because of the strong inter-atomic bond of the silicon and carbon atoms. Therefore, etching using aqueous solutions must be performed at temperatures greater than 600°C [19], which is not compatible with low-temperature processes. As a result, dry techniques such as RIE and lift-off are better suited. Lift-off of SiC can yield good results [20], but entails multiple steps, requires sacrificial materials, and can be difficult to optimize for the desired resolutions. RIE is a more commonly used technique, and can yield better etch profiles and resolution.

A magnetically enhanced (ME) RIE with NF_3 was used in this work. NF_3 yields fluorine ions efficiently and, as a consequence, has one of the highest etch rates of all fluorinated gases. SiC RIE can lead to excessive etch residue formation from mechanisms such as micro-masking [21]. Fig. 5 shows an un-optimized etch recipe that yields a grassy etch field. The long columnar structures are attributed to re-deposited non-volatile material landing in the etch field, creating localized masks. This residue can significantly reduce the contact quality of the underlying metal layers. Optimizations in masking material and etch parameters were necessary to mitigate these effects. An etched SiC sample masked with chromium is shown in Fig. 6. The etch rate obtained was $2079 \text{ \AA}/\text{min}$, and no residue is present in either the etch field or on the sidewalls.

Fig. 5: SiC test structure etched using non-optimal process parameters, yielding etch field residue.

Fig. 6: Scanning electron micrographs of (a) an SiC corner, and of (b) a sidewall, both etched with optimal process parameters.

FABRICATION RESULTS

Several test devices were fabricated (Fig. 7) using the process flow outlined in Fig. 1. These include beam resonators, inductors, and variable capacitors. All devices clearly exhibited low stresses and low stress gradients in the structural layers. Fig. 7a and 7b show electron micrographs of a clamped-clamped beam resonator and its transducer gap, respectively. The gap is clear of residue, and confirms successful release of the devices. Fig. 7c and 7d show a released variable capacitor with release holes, and a released inductor. Stress control is apparent in the capacitor which shows no signs of plate deformation due to intrinsic stress.

Fig. 7: Scanning electron micrographs of (a) a released clamped-clamped beam MEM resonator, (b) its transducer gap, (c) a variable capacitor, and (d) a released inductor.

Similarly, the released inductor exhibits low stress gradients. This is important, as warping of large structural membranes, such as the parallel plates in a variable capacitor, can result in a significant loss in tuning performance or even device malfunction due to interlayer stray contacts.

The measured transfer function of a clamped-clamped beam resonator device with a natural frequency of 8.3 MHz is shown in Fig. 8. The mechanical quality factor (Q) measured in vacuum is 815, which compares favorably with values reported for similar SiC beam-type resonators (e.g. $Q=490$ in [20]).

Fig. 8: Transfer function of an 8.3 MHz clamped-clamped beam resonator.

CONCLUSIONS

This work presented a low-temperature and low-stress process for *a*-SiC that was demonstrated with functional fabricated MEM resonators. This process features double-sided metallization that allows for high quality conduction of two separate signal paths. The SiC structural layer allows for higher acoustic velocity, operation in harsh environment, and increased reliability. DC sputtering is used for metals and SiC, making the process low-cost and easy to integrate with standard integrated circuits processes. Additionally, the sacrificial spun-on polyimide allows for low-cost creation of the small gaps required for devices such as MEM resonators. This process enables processing of SiC through innovative masking techniques that reduce aluminum micro-masking issues. These results establish a strong foundation for the integration of high-performance MEMS with CMOS devices.

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