A NEW EXTRINSIC GETTERING TECHNIQUE IN THICK BONDED SILICON-ON-INSULATOR WAFERS ENABLING SENSOR – IC INTEGRATION

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ABSTRACT

A new technique for gettering of transition-metal impurities in thick bonded SOI (BSOI) wafers is demonstrated. A thin poly-Si interlayer was placed between the active silicon layer and the buried oxide by direct wafer bonding. Testing of wafers in CMOS processes showed a clear improvement of the gate oxide integrity, even approaching that of conventional bulk silicon wafers. Poly-Si interlayer layer showed no measurable effects on BSOI characteristics such as bond strength, interfacial voids, or sacrificial oxide etching, and the residual stress was very low. The results suggest that a thin poly-Si layer has minimal effect on fabrication of the MEMS elements.

INTRODUCTION

Integration of MEMS with integrated circuits is one of the major attractions of silicon micromachining. From the technical solution viewpoint, integrating MEMS and signal processing circuitry on a single chip has some distinct advantages. Significantly smaller signals can be processed on-chip as compared to the MEMS element and the electronics on separate chips, allowing smaller silicon sensor size and low power consumption. Also, package size constraints or high interconnection densities can justify integration. However, due to incompatibilities of MEMS and IC processes the development cycles have been long and complex device and process integration has made it less common in MEMS.

Processing options that combine thick BSOI wafers and deep reactive ion etching can considerably simplify process integration. In particular, it is possible to design the process to include the MEMS process steps in the beginning and in the end, not interrupting the CMOS processing at all. The buried oxide of the SOI wafer makes it possible to release the MEMS devices by deep reactive ion etching after the IC processing is completed, and standard IC foundry processes can be used. In CMOS integrated systems – or equally in power or mixed signal devices made on thick SOI wafers – the techniques for gettering fabrication-induced metal impurities need to be addressed.

Poor gettering of metal impurities is a fundamental problem on thick BSOI wafers. Transition metal contaminants in CMOS devices is known to lead to oxide breakdown device failures and decrease in gate oxide integrity [1]. The methods that are in widespread use for gettering transition-metal contaminants include e.g. SiO₂ precipitates in the bulk of Czochralski (CZ) silicon wafers, mechanical damage, deposited polycrystalline silicon film on the backside of the wafer, or substrates with high boron concentration [2, 3, 4]. In SOI wafers the buried oxide forms a diffusion barrier for most transition metals. It prevents the use of any of the standard gettering methods in which the sinks for diffusing impurities are located in the back surface of the wafer or in the bulk of the handle Si wafer. Oxygen precipitation within the active device layer would lead to SiO₂ precipitates and associated defects also on the surface of the device layer. Heavy boron implantation at the start of the CMOS process at defined areas has been used for gettering with BSOI wafers [5, 6]. Lateral gettering

techniques have several drawbacks as the implanted areas must be designed as part of the circuit layout, and the gettering efficiency depends on the distance to the active device area.

In this paper, use of polycrystalline silicon interlayer for effective gettering of metal impurities in thick BSOI wafers is demonstrated and discussed. In the BSOI structure, a thin LPCVD polycrystalline silicon (poly-Si) film is placed as a gettering layer between the active silicon layer and the buried oxide by direct bonding. The distance between the active device area and the gettering layer is short and constant, yet the poly-Si layer is in the noncritical region for CMOS processing.

EXPERIMENTAL

BSOI structures with and without a poly-Si interlayer were fabricated by direct bonding, mechanical grinding and polishing. The device wafers were p-type, <100> -oriented 150 mm Czochralski silicon wafers with resistivity of 1 – 15 Ω cm. Undoped poly-Si film was formed on the device wafer by LPCVD, and the poly-Si surface was polished by CMP. The thickness of the poly-Si film varied from 0.2 to 1.0 μ m. The device wafer was then bonded to the handle wafer with a thermally grown oxide (oxide thickness 0.2-2 μ m), and the bonded wafer pairs were annealed for 2 h at 1100°C. The bonded wafer was thinned down by grinding and polishing. The final thickness of the BSOI layer was from 2 μ m to 20 μ m, with thickness uniformity better than $\pm$ 0.5 μ m. Some of the wafers were run through a high temperature process cycle (total time at $\geq$ 1000°C 24 h, with maximum temperature of 1150°C for 4 h) to simulate wafer processing.

Two methods were applied to measure the efficiency of metal impurity gettering. Some wafers were intentionally contaminated with Fe by dipping in SC-1 solution and subsequent heat treatment was used to drive contaminants into the bulk. Fe concentration in the active region of the SOI wafer was analyzed with DLTS measurements based on surface contact method. The detection limit of DLTS depends on the active layer thickness and resistivity, and it was approximately $1 \cdot 10^{11}$ at/cm³ in the studied wafers.

SOI wafers with a poly-Si interfacial layer and a final active layer thickness of 10 μ m were processed through a 0.6 μ m CMOS flow. To ensure the effect on gate oxide quality, if any, of the buried poly-Si layer could be quantified, bulk Si wafers with intrinsic gettering and SOI wafers without an intrinsic gettering mechanism were processed at the same time in the same lots. Extensive wafer level testing was carried out to quantify relative gate oxide quality on the experimental splits by measuring gate oxide capacitor dielectric breakdown. To determine capacitor breakdown the voltage across the dielectric was ramped into accumulation until catastrophic breakdown was triggered.

The fabricated thick BSOI structures were examined with several techniques. Cross sectional analysis was done with Scanning Electron Microscopy (SEM) and defect etching. Wafers were analyzed for interfacial voids using Scanning Acoustical Microscope (SAM). The smallest detectable defect size in a bonded interface was from 25 to 30 μ m in diameter. Bond strength was examined with crack opening method [7] and with HF etching

test [8]. In the former technique, the bond strength is calculated from observed crack length by a blade inserted between bonded wafers. The latter technique is based on the measurement of the lateral buried oxide etch rate in hydrofluoric acid (HF) solution. In these tests 50% HF at room temperature and with 10 minute etching time was used. The surface roughness of poly-Si interlayer after removing the handle silicon wafer and the buried oxide was measured with Atomic Force Microscopy (AFM).

Stress in the poly-Si layer was measured with FSM-128 film stress measuring tool (laser scanner) and also by optically measuring the curvature of HF released beams. Samples for the latter method were prepared by dicing SOI wafers to get several pieces which were etched in 49% HF solution in order to release the beams from the handle wafer. Stress was calculated from the curvature results using Stoney's equation after Klein [9].

RESULTS AND DISCUSSION

Cross-sectional poly structure

Cross-sectional SEM image of the SOI structure with interfacial poly-Si layer is presented in Fig. 1. The poly-Si layer is just beneath the active device layer, and the bonded interface is between the poly-Si layer and the buried oxide layer (oxide thickness 1.0 μm). The polycrystalline region consists of randomly oriented grains with diameters varying from few tens of nanometers to few hundreds of nanometers. In the active silicon region there are no dislocations originating from the poly-Si layer.

The effect of high temperature heat treatment ($> 1000^\circ\text{C}$ for 24 h, maximum temperature of 1150°C for 4 h) on the polycrystalline structure can be seen in Fig. 2 where cross sectional SEM image of BSOI structure with 0.6 μm thick poly-Si interlayer is presented. Defect etching was made for enhancing the visibility of grain boundaries. The number of individual poly grains has decreased and their respective size has increased. As grain boundaries act as gettering centers for impurities, gettering efficiency will decrease as grains grow during heat treatment. However, the poly structure has remained relatively unaffected by the heat treatment when compared to literature results [10]. It is proposed that the presence of both single-crystal silicon and buried oxide next to the poly layer is responsible for this enhanced stability.

Figure 1: Cross sectional SEM image of bond interface in BSOI wafer structure with buried 0.6 μm poly-Si interlayer between the active silicon layer and the buried oxide.

Figure 2: Cross sectional SEM image of BSOI structure with 0.6 μm thick poly-Si interlayer after high temperature heat treatment ($> 1000^\circ\text{C}$ for 24 h, maximum temperature of 1150°C for 4 h) and defect etching for enhancing the visibility of grain boundaries.

Gettering efficiency

Active layer iron concentrations of different SOI samples measured with DLTS and calculated gettering efficiencies are presented in Table 1. Intentional contamination of BSOI wafers with no poly-Si interlayer induces Fe concentration in the bulk of the active layer from $2 \cdot 10^{13}$ to $4 \cdot 10^{13}$ at/cm^3 . With poly-Si interlayer (layer thickness 0.6 μm) the Fe bulk concentration was below the detection limit of the DLTS measurement ($1 \cdot 10^{11}$ at/cm^3). Compared to reference BSOI wafers, the Fe concentration decreases by at least two orders of magnitude. It is attributed to the polycrystalline Si interlayer forming a sink to diffusing Fe atoms. Gettering efficiency was calculated to be over 99%, and the exact value was limited by the DLTS detection limit.

Part of the wafers went through a high temperature heat treatment before intentional contamination and in these wafers the Fe concentration in the active device layer was $1.2 \cdot 10^{12}$ at/cm^3 with poly-Si interlayer. As indicated above, recrystallization at high temperatures increases the polycrystalline grain size reducing the area of grain boundaries resulting in fewer gettering sites. However, even after high temperature annealing cycle the gettering efficiency was as high as 96.5%.

Table 1: Fe concentrations in intentionally contaminated BSOI wafers with and without 0.6 μm poly-Si interlayer as measured with DLTS. Part of the wafers went through a high temperature heat treatment cycle before the intentional Fe contamination ($> 1000^\circ\text{C}$ for 24 h, maximum temperature of 1150°C for 4 h).

Wafer type	Heat treatment	Fe (at/cm^3)	Gettering efficiency (%)
SOI with poly	NO	$< \text{DL}$	> 99.4
SOI w/o poly	NO	$1.9 \cdot 10^{13}$	NA
SOI with poly	YES	$1.2 \cdot 10^{12}$	96.5
SOI w/o poly	YES	$3.4 \cdot 10^{13}$	NA

CMOS processing

The gettering effectiveness of the buried polysilicon layer was determined by comparing the spread of catastrophic gate oxide breakdown on the wafers with the poly-Si interlayer with that of traditional SOI wafers with no additional gettering and normal bulk wafers, after processing through a 0.6 μm CMOS flow. The CMOS flow is a well established, long running bulk wafer process which employs oxygen precipitate induced stacking faults in the bulk of the wafer to getter low levels of background metallics present in a typical state of the art processing environment. On traditional SOI wafers with no additional gettering gate oxide quality is degraded compared to bulk wafers. A midfield distribution in the breakdown is observed, indicative of reduced gettering of background metallics [Fig. 3]. When wafers with the

buried polysilicon layer are processed, this midfield distribution is substantially reduced leading to gate oxide quality approaching that of the bulk CMOS process [Fig. 4]. Additionally SEM images of cross sectioned wafers post processing show the continued presence of grain boundaries. This indicates that even after a thermal budget including cycles up to 1100°C the polysilicon retains some grain structure and so the gettering mechanism will remain active even through a significant thermal budget.

Figure 3: Cumulative probability plot of V_{bd} comparing standard BSOI to conventional bulk wafers.

Figure 4: Cumulative probability plot of V_{bd} comparing BSOI with buried polysilicon to standard BSOI.

Stress in the poly-Si interlayer

The stress in the as-grown LPCVD polysilicon film and in the poly-Si interlayer was measured using FSM-128 film stress measuring tool. The polycrystalline film is initially in high compression, and the film stress was in the range 280-350 MPa independent of the poly thickness (0.2-1.0 μm). Film stress in the poly-Si interlayer after SOI wafer processing was measured by removing the handle silicon wafer and the buried oxide. Small compressive stress of 1.5 MPa was found in a 0.6 μm poly-Si layer.

The film stress was also calculated from the radius of curvature induced by the poly-Si layer on release etched 20 μm thick beams. Film stress was 1.4 MPa with 0.6 μm poly and 1.1 MPa with 1.0 μm poly. The stress was tensile in both cases.

In conclusion it can be stated that the residual stress in poly-Si interlayer is relatively low (≤ 10 MPa) as bond annealing relaxes the initial high stress.

Bond interface characterization

Bond strengths measured with crack opening method were in the range of 2.1-2.5 J/m^2 for BSOI wafers with and without poly-Si interlayer. The values are in good agreement with typical surface energy of hydrophilic silicon/oxide bonds annealed at $\geq 1100^\circ\text{C}$.

Etching of the buried oxide can be used to characterize the bonded interface. Also, sacrificial oxide etching is a standard step in MEMS processing to release mechanical structures, and it is critical to have a well-defined oxide etching rate. Both the etching rate and the profile of the etched oxide are characteristic of the bond quality. For full strength of the bond the etched oxide edge is nearly straight. If HF etching proceeds faster along the bonded interface, a notch is formed and the oxide starts to etch also in vertical direction resulting in high effective etching rate. For hydrophilic silicon/oxide bonds the recorded values of the etching rate in 50% HF for 10 min at room temperature for a large number of different types of SOI products range from 1.4 to 1.6 $\mu\text{m}/\text{min}$.

In these tests the etching rate of buried oxide was measured with cross-sectional SEM. One cross-sectional image is shown in Fig. 5. The etched oxide profile is almost vertical indicating that the etch rate along the polySi-SiO₂ bond interface is very close to the etch rate along the thermal oxide interface. HF etch rate results of different SOI samples can be found in Table 2. These are calculated as average values from three points in each sample wafer. The poly-Si interlayer or polySi-SiO₂ bond interface have no influence on etching of the buried oxide.

Figure 5: Cross-sectional SEM image for measuring the HF etching rate of buried oxide. BSOI wafer with 10 μm active layer, 1.0 μm buried oxide, and 0.6 μm poly-Si interlayer.

Table 2: Etching rate of the buried oxide (50% HF for 10 min) in different BSOI samples. Poly-Si interlayer thickness 0.6 μm .

Wafer type	Heat treatment	Etch rate ($\mu\text{m}/\text{min}$)
SOI with poly	NO	1.45
SOI with poly	YES	1.47
SOI w/o poly	NO	1.46

Bond interface quality was inspected with SAM using measurement mode detecting voids larger than or equal to 20 - 30 μm in diameter. Image of a high-resolution SAM measurement of BSOI wafer with 0.6 μm poly-Si interlayer is presented in Fig. 6 showing defect-free interface down to 30 μm void diameter.

The number of voids was also evaluated by fabricating 100

BSOI wafers with a poly-Si interlayer, and scanning the whole wafer area with SAM. The smallest detectable defect size in a bonded interface was approximately $70\text{ }\mu\text{m}$ due to the scan resolution. The wafers had on average less than one void per wafer, and no voids larger than 1.0 mm . High temperature heat treatment had no effect on the void distribution. The results indicate good quality of the bonding between polycrystalline silicon and thermal oxide.

Figure 6: Bond interface quality of 200 mm BSOI wafer with $0.6\text{ }\mu\text{m}$ poly-Si interlayer measured with SAM ($50\text{ mm} \times 50\text{ mm}$ area).

The micro-roughness of the polySi-SiO₂ bond interface in BSOI wafer with $0.6\text{ }\mu\text{m}$ poly as measured with AFM was $R_q = 0.296\text{ nm}$ (AFM with $5\text{ }\mu\text{m} \times 5\text{ }\mu\text{m}$ scan area) [Fig. 7]. This is higher than in standard SOI wafers in which the Si-SiO₂ bond interface roughness was around 0.1 nm . Thermal wet oxidation ($0.2\text{ }\mu\text{m}$) of the poly-Si interlayer surface and oxide removal increased the surface roughness to $R_q = 5.0\text{ nm}$. With short oxidation and oxide removal after sacrificial oxide etching to release of the mechanical structures the polysilicon surface roughness might be high enough to reduce sticking of released active layer structures.

Figure 7: AFM image of active layer bond interface in gettered SOI wafer with $0.6\text{ }\mu\text{m}$ poly-Si interlayer ($R_q\text{ }0.296\text{ nm}$).

CONCLUSIONS

Thick BSOI wafers with and without a thin polycrystalline silicon film between the active device layer and the buried oxide were fabricated, and their properties were evaluated. With a poly-Si interlayer, the quality of the gate oxide after a full CMOS process flow was approaching that in standard silicon wafers. The significant improvement in the gate oxide integrity as compared with standard SOI structure is associated with effective gettering of fabrication-induced metal impurities by the poly-Si layer. One obvious application is for IC-integrated MEMS processing options that build on thick BSOI wafers. Implementation of gettering by a poly-Si interlayer provides effective gettering sinks that are built in the BSOI substrate. Evaluation of the wafer properties suggests that the thin poly-Si layer has minimal effect on fabrication of the MEMS elements. The quality of the bonded interface is similar to that in standard bonded wafers, there is no influence to the sacrificial etching of the buried oxide, and the residual stress in the poly-Si film is very low.

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