AN INTERDISCIPLINARY LABORATORY COURSE IN MICROSYSTEM DEVELOPMENT

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ABSTRACT

An interdisciplinary course in microsystem development is described in which students define, design, fabricate, and test a two-chip microsystem. A six-mask dissolved-wafer MEMS chip and a five-mask E/D NMOS LOCOS circuit chip are used to implement a wide variety of devices, including visible imagers, pressure sensors, accelerometers, g-switches, tactile imagers, cursor controllers, pressure-and-thermally-based flowmeters, micro-mirror arrays, thermal mass sensors, and Pirani gauges. The course teaches interdisciplinary teamwork and emphasizes the interactions among design, fabrication, and test, producing working microsystems in a single 14-week term.

INTRODUCTION

Integrated sensors, MEMS, and microsystems have developed over the past forty years driven by innovative process technology, microstructures, and applications. While microelectronics has managed to coalesce around CMOS technology, no single standard process exists for MEMS because of the divergent structures and device types needed. At the same time, reading out high-performance sensors resolving sub-femtofarad capacitance variations (or equivalent resistive changes) demands the integration of electronics with the transducer, either monolithically or as a multi-chip hybrid.

Educational programs in MEMS and microsystems must teach a variety of topics, including materials, transduction mechanisms, microstructures, process technologies (e.g., micromachining and wafer bonding), interface circuit design, and system partitioning. In addition to lecture courses, it is important that students have the opportunity to create a microsystem for themselves. This experience should include defining the microsystem function, designing it, fabricating it, and actually seeing it work. Going through this process allows the student to experience the pride of creating a chip from start to finish and to understand the interactions among design, fabrication, and testing. In no other way, can the importance of topics such as design for testability be fully appreciated nor can the tradeoffs in balancing an overall process flow be properly understood. For some students, this experience is the entry point into a doctoral program where it will be repeated in far greater detail, but for many it will be the only time in their careers that they have the opportunity to take an idea from inception to working silicon. Such an experience is even more valuable for these students, giving them a basis for working effectively across the boundaries that occur in industry among design, fabrication, and test.

This paper describes a one-semester course offered at the University of Michigan that allows undergraduate seniors and first-year graduate students to define, design, fabricate, and test a two-chip microsystem of their choosing. The MEMS chip is implemented using a six-mask dissolved-wafer process that includes two boron etch-stop diffusions and anodic silicon-

glass wafer bonding. Although alternative processes are possible (i.e., surface-micromachined, front-undercut or back-etched bulk processes), this process was chosen because of its ability to implement a wide range of different transducer functions while illustrating a wide set of process steps. The readout/interface chip is implemented in a five-mask doubly-implanted silicon-gate 1M/1P E/D NMOS LOCOS process. While a full CMOS process would be preferable, the added process complexity is not possible in a five-week fabrication cycle. The use of a two-chip combo as opposed to a single monolithic chip allows the two processes to be run in parallel, shortening the fabrication cycle. This course was run for many years as an integrated circuit laboratory but was broadened in 2001 to a four-credit *Integrated Microsystems Laboratory*. As the result of this topic shift, changes in prerequisites, and the creation of an important feeder course for our entire microsystems program (*Introduction to MEMS*), enrollment has gone from 15 in 2001 to 48 in 2006, shifting from mostly graduate students to mostly undergraduates. The course serves as a major design experience for undergraduates.

DESIGN

Entering the course, students are provided with a fixed die area for each chip (2mm x 2mm), with process flows for each chip, and with fixed pad positions consistent with the probe cards used during the testing phase of the course. Course prerequisites require that students enter the course with either a solid-state electronics background (a basic course in p-n junction theory and devices, and a circuits course) or a MEMS background (the introductory course mentioned above). They are asked to form project teams of four persons and are encouraged to include a mix of backgrounds and experience. While most students come from electrical engineering, it is common for students from biomedical, chemical, mechanical, and materials engineering to take the course as well. The use of teams allows the students to learn from each other and experience working in a (hopefully) synergistic group, where it is up to them to plan the project execution and to coordinate individual activities. Thus, the course attempts to teach interdisciplinary teamwork. Three-person teams would perhaps be preferable, but four person teams are helpful in handling enrollment pressures.

Figure 1 shows the activity flow in the course. After forming teams, the students select a microsystem function to implement. Typically a dozen or so project ideas are suggested, but the students are free to select something of their own choosing and often do. They are encouraged to define it in terms of a practical application and to consult the literature to learn about similar functions reported there. About two weeks are spent defining the microsystem function and reducing it to block diagram form. The course consists of two 80-minute lectures per week and one four-hour laboratory session. The laboratory sessions are used during the design phase of the course for group interactions, for one-on-one discussions with the instructor, and for supplementary lectures

on various topics as needed. With the block diagrams completed, the students proceed to fill in the blocks with

Fig. 1: Activity flow in the Integrated Microsystems Laboratory course.

specific transducer and circuit designs. These are full-custom designs done on workstations running Cadence or Mentor Graphics software, with simulations run in CoventorWare, SPICE, and SUPREM. The lectures present the details of MOS device and circuit design. Prior to 2001, a VLSI design course was required as a prerequisite, primarily so that students were familiar with the design tools. Since then, that prerequisite has been dropped and we have held an evening tutorial session on the design tools during the third week of the course. This has been adequate to allow the designs to go forward. The lectures are taped and accessible over the web, allowing the course to be taken at both Michigan State and Michigan Tech with an on-site instructor. Students at these participating universities go through the same procedures as the students at Michigan, submitting their completed designs over the web. All designs are incorporated into two multi-project mask sets, reflecting the MOS and MEMS chips. For example, with forty students at Michigan and eight at Michigan State, we would have twelve project chips per mask set. We also add test chips on each mask set that contain alignment marks, in-process test patterns, and test devices for process evaluation. For example, the circuit test chip contains resistors for determining the poly and diffused bulk sheet resistances, a transistor string for device characterization (enhancement, depletion, field), metal-to-poly and poly-to-substrate capacitors for oxide and C-V measurements, a ring oscillator (propagation delays), and test inverters.

At the end of five weeks, tape-out occurs and the designs are sent out for mask making. Graduate student mentors are sometimes used to help particular teams with their individual design challenges. First masks are typically returned within three days of submission.

FABRICATION

Figures 2 and 3 show the process flows for the MOS and the MEMS processes, respectively. Minimum features of 6µm and alignment tolerances of 3µm are used for the circuit chip, with somewhat larger features on the MEMS chip. These are adequate for the equipment used and allow 100-200 transistor circuit designs to be implemented as needed. Processing uses 100mm silicon and glass (Pyrex) wafers.

Fig. 2: Process flow for E/D NMOS circuits.

During lecture sessions, micromachining, wafer bonding, silicon oxidation, diffusion, metallization, and pattern transfer are discussed. Laboratory sessions are carried out in a dedicated Class 10,000 Instructional Laboratory equipped for lithography, wet oxide and metal etching, field and well oxidations, phosphorus source-drain diffusions, plasma etching, and metallization (sputtering). The field and depletion implants are done in a commercial foundry, and the chemical vapor deposition (CVD, nitride, poly, and LTO) steps, gate oxidation, boron etch-stop diffusions, and dry etching is done by engineering staff in the adjacent Class 10/100 research cleanroom. Wafer bonding and microstructure release etching are also done by staff but is videotaped and shown to the class. In a typical afternoon laboratory session, the section is split into two or three sub-sections to allow more students to be

are also done by staff but is videotaped and shown to the class. In a typical afternoon laboratory session, the section is split into two or three sub-sections to allow more students to be accommodated and to reduce waiting time in using the equipment. Students quickly learn to perform the various process steps themselves, although sessions are supervised by two people at all times. Those taking the course at remote sites (e.g., Michigan State) do processing in their own laboratories while their designs are fabricated as part of the multi-project activities at Michigan. Finished wafers are returned to them for testing. Figure 4 shows views of completed MOS and MEMS wafers in these process flows.

Fig. 3: Dissolved-wafer process flow for the MEMS chip.

TESTING

Testing is carried out by teams using two Suss probe stations equipped with television monitors and equipment racks that contain power supplies, pulse generators, oscilloscopes and other instrumentation. Students sign up for three-hour testing blocks and begin by characterizing the test chip (Fig. 5). A previous assignment prepares the students by asking them to characterize the test chip from a previous year. One week is therefore devoted to measuring a variety of device characteristics (thresholds, breakdown voltages, contact linearity, C-V characteristics) and comparing them to theory. Channel lengths and mobilities are extracted from these measurements. Students then move to testing their circuit chips, again at the wafer level, and then to their MEMS devices. The dissolved-wafer process is consistent with the realization of capacitive devices and the use of electrostatic self-test, both of which are advantageous. Capacitive devices, in particular, are significantly easier to read out because of their relatively high sensitivities and their compatibility with Schmitt

oscillators and other mostly-digital circuits as opposed to more difficult amplifier circuit designs. For final testing, the wafers are diced and the two-chip combos are mounted in packages to allow them to be tested as a complete microsystem.

Fig. 4: Views of completed MOS and the MEMS wafers.

Fig. 5: Top view of the MOS test chip used for device and process characterization.

Fig. 6: Top view and SEM side view of a silicon-glass g-switch realized in the dissolved-wafer process.

Figure 6 shows an example of a g-switch realized in the course. The diffused wafer process here uses a deep (10-12 μm) etch-stop for structural elements and a shallow diffusion (2-3 μm) for diaphragms and some beams. Here, a deep diffusion is used for the proof mass and the anchor areas while a shallow diffusion is used for the beam itself. The capacitive gap in this and other structures is targeted at 2-3 μm . Such devices are useful for shock sensing (e.g., in packages during shipment) and when combined with CMOS circuitry can do so with virtually no power dissipation. Figure 7 shows some of the

Fig. 7: Top views of four MEMS devices: (clockwise from top left) Pirani gauge, thermal mass sensor, tactile imager cells, and capacitive microphone.

Fig. 8: Views of several MOS interface chips realized in the course: (clockwise from top left) visible imager, Pirani gauge, micro-mirror display, accelerometer, microphone. All dice: 2mm x 2mm.

other MEMS devices realized in the course. Device yields vary by structure but are typically in the range of 40-60 percent, with most yield loss occurring due to handling of the relatively delicate microstructures. This yield is more than sufficient for class purposes.

Figure 8 shows a set of typical MOS interface circuit chips realized in the class. The process uses a recessed self-aligned field and a gate oxide thickness of 40nm. Aluminum metal is used with a 425 $^{\circ}\text{C}$ sintering step to improve the contacts. Circuit yields are typically greater than 80%.

CONCLUSIONS

Integrated microsystem development is taught in a one-semester laboratory course at the University of Michigan. The microsystems are implemented as two-chip combos using a dissolved-wafer MEMS process and an E/D NMOS circuit process, run in parallel. The students spend approximately five weeks in design, five weeks in fabrication, and three weeks in test. Homework assignments are used together with typically three quizzes, a mid-term report (covering design), a final report (covering design, fabrication, and test), and a presentation to the class. The class is very demanding and yet very popular with the students, typically being featured on resumes and in job interviews. In six years (2001-2006), the course has trained over 200 students with an average course evaluation ("this is an excellent course") score of 4.7/5.0. In 2003, one of the course projects was submitted to the ISSCC/DAC design contest and won second place in the conceptual category.

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