BACKSIDE RESISTIVE LOCALIZED HEATING FOR LOW TEMPERATURE WAFER-LEVEL BONDING AND PACKAGING

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ABSTRACT

A new method has been developed for localized heating of a bond region when bonding two wafers, while maintaining a low temperature where sensitive devices are located. Using this technique, access is only required to the backsides of the two wafers, thus making the process easier and wafer-level compatible. In this “differential” heating method, one of the two wafers to be bonded is heated from the backside, and the other is cooled from the backside. Heat flows through the bond areas where the two wafers are in contact, thus heating these regions more than other. Integrated temperature sensors were used to measure the temperature at different distances from the bond region while making a Au-Si eutectic bond between silicon and glass wafers. When bond regions reached ~ 410 – 475°C , the sensitive device regions $600\text{ }\mu\text{m}$ and $50\text{ }\mu\text{m}$ away from the bond were measured to reach only 92 and 250°C , respectively. Simulations using ANSYS were performed and used for the design of the wafer bonding setup and for predicting the needed input power and heater temperatures.

INTRODUCTION

Vacuum/hermetic sealing is required for a wide range of micro-systems. Current wafer-level encapsulation techniques such as frit bonding ($\sim 450^\circ\text{C}$), Au-Si eutectic bonding ($\sim 390^\circ\text{C}$) [1], and thin film encapsulation ($\sim 600^\circ\text{C}$) [2] require relatively high temperatures that often preclude their use in some applications. For this reason, researchers have investigated lower temperature bonding methods using polymers and solders at lower temperatures. Another option is to use a well established high temperature bonding method and use *localized heating* to heat the bond region to a high temperature, while maintaining a low temperature where devices that are to be encapsulated are located.

A number of localized heating methods have been reported in the literature using lasers, microwaves, resistive elements and induction. In *laser assisted* localized heating, a laser wavelength is chosen that is transparent to the substrate but heats the material at the bond region. Laser assisted bonding has been applied in solder and anodic bonds [3, 4]. In a similar manner *microwaves* have been used to fuse two Au surfaces to achieve silicon to silicon bonds [5]. Using *resistive heating*, substrates have been bonded through plastic, PSG, solder, fusion and eutectic bonding [6]. In this case, the resistor had to be fabricated on the front surface of one of the wafers, and then accessed electrically for heating. Therefore, using this technique at the wafer level is challenging. *Inductive heating* is a related technique in which an inductive coil creates a magnetic field, causing large eddy currents in a bond ring made out of a ferromagnetic material. This technique has been applied for silicon to silicon and silicon to glass wafer bonds [7]. The main draw back of this technique is that it limits the range of materials that can be processed on the bonded wafers.

We report a localized heating method in which heat is applied to the backside of one of the two wafers to be bonded (e.g., the “cap” wafer used to encapsulate the device), and removed from the backside of the second wafer (e.g., the “device” wafer) as illustrated in Fig. 1. Because most of the heat is drawn towards the heat sink in Fig. 1, the device region is heated less than the bond

region. This method is attractive because it can be applied on a wide range of materials and at wafer level. The heating of the cap wafer mentioned above could be achieved using a variety of techniques, including using a heater substrate with on-chip resistive heaters, as reported in this paper.

MODELLING AND DESIGN

A 3-D thermal model was constructed with the layers shown in Fig. 1 to aid in the design of the wafer bonding setup. The complete system consists of several substrates: a CogethermTM insulator plate (10.5 mm thick), a glass heater substrate with on-chip resistive heaters ($550\text{ }\mu\text{m}$), a silicon *cap wafer* ($550\text{ }\mu\text{m}$), a *device wafer* (modeled as either silicon or glass, $550\text{ }\mu\text{m}$) a copper plate heat sink substrate on top of the device wafer (3.1 mm thick), and a steel plate providing the bond force (modeled as 14 mm thick).

Figure 1: A schematic showing that using the differential heating method, most of the heat flows toward the heat sink as supposed to laterally, towards the device.

Figure 2 shows the structure of the to-scale 3-D model used for predicting necessary input powers and the resulting temperature distributions. In this model, there is symmetry along the planes perpendicular to the x and y axes so that the model represents a quarter of the actual assembly. As with the eventual test setup, arrays of heaters were used to heat up 4 bond rings at a time on a relatively small portion of the wafer. The picture of the assembly in Fig. 2 was made transparent to allow a view of a quarter of one of these $0.75 \times 10500 \times 13300\text{ }\mu\text{m}$ heaters which encompass 4 full bond rings (that is 1 bond ring in this quarter symmetry model). As also shown in Fig. 2, adjacent bond brings were incorporated into the final model. It was found with successive 3-D models, the addition of more and more detail (such as added assembly width and adjacent bond rings) resulted in lower predicted temperatures for a given input power and in results that more closely matched those seen in initial tests.

In simulating the model, a steady state solution was found by applying a uniform power density across the heater, while the top

Figure 2: The structure of the model used for simulation.

of the steel plate and the bottom of the insulator plate were held at 23°C. Figure 3 shows the results of a model for the case where a 110 W power is applied to the heater for a bond to a glass device wafer. As shown in Fig. 3b, temperature profiles were produced across different planes sliced through different portions of the assembly in order to analyze the results. The device cavities were 90 μm deep (Fig. 1 and 3d), each bond ring was 2.3x2.3mm square (Fig. 3e), and the bond ring widths were 100, 50 or 25 μm (Fig. 3e).

As shown in Figs. 3a and 3c, the temperature drops very quickly across the glass device wafer, and approaches room temperature at the copper heat sink. Furthermore as illustrated in Fig. 3a, due to lateral heat spreading, there is a large lateral temperature gradient across the assembly. As shown in Figs. 3c and 3e, this leads to a temperature gradient across the heater of 375 to 514 °C and across the bond ring of 410 to 473 °C. Figure 2e illustrates the effectiveness of this localized heating method, with the temperatures dropping to 250 °C and 99 °C at 100 and 600 μm from the bond ring.

Table 1 shows the power needed to heat the entire bond ring to above 410°C, the temperature at the heater, and the temperature 600 μm from the bond ring for bonds to glass and silicon device wafers. As shown, when silicon is used as the device wafer, the

Table 1: ANSYS Predicted power need to achieve a bond ring temperature of greater than 410°C, and the temperature at the heater and at a 600 μm distance away from the bond ring .

Device wafer Material	Power	Heater Temp.	Temp. 600 μm away
Glass			
Bond ring width:100 μm	110 W	Ave: 453 °C Max:514 °C	99 °C
Silicon			
bond ring width:100 μm SiO ₂ thickness: none	1900W	Ave: 932°C Max:1291°C	330 °C
bond ring width:100 μm SiO ₂ thickness:6 μm	600 W	Ave: 630°C Max: 881°C	118 °C
bond ring width:50 μm SiO ₂ thickness:6 μm	450 W	Ave: 605°C Max: 802°C	91 °C

model predicts a necessary power of 1800W, and a maximum heater temperature of 1291°C to achieve a bond ring temperature above 410 °C. Material selection for such a high power, high-temperature heater would be challenging. The higher necessary power and maximum heater temperature is due to the larger thermal conductivity of single crystal silicon (141 W/m·K) as compared to glass (1.4 W/m·K). In other words, silicon draws heat away from the heater more efficiently.

Figure 4 shows a simple 1-D representation of the heat flow, q , from the heater, through the bond ring, to the heat sink. When bonding to a glass device wafer, the thermal resistance directly above the bond ring, $R_{\text{bond ring}}$, is extremely large compared to the other thermal resistances because of: 1) the relatively small cross sectional area at the bond ring, A , and 2) the small thermal conductivity, k , of glass. This large thermal resistance leads to a large temperature drop directly above the bond ring (Fig. 2c) and therefore a relatively small necessary input power and maximum heater temperature. When bonding to a silicon device wafer, $R_{\text{bond ring}}$ can be increased by either using a dielectric layer (decreasing k) or decreasing the bond ring width (decreasing A). As shown in Table 1, using a 6 μm SiO₂ layer brings the necessary power down to 600W and the maximum heater temperature down to 881°C. This thickness of SiO₂ was chosen to approximate the combined

a) Model of the Assembly

b) Slice taken of the model

c) Heater slice (top)

d) Cross section slice

e) Bond ring slice (top)

Figure 3: a) A parametric view for the model of the differential heating test setup, b) an illustration of a slice taken out of the model, c) a slice showing a cross section of the heater and bond ring, d) a slice of the heater and e) a slice of the bond ring.

Figure 4: A schematic of heat flow in the bonder test setup.

thermal conductivity of the thin film stack in a CMOS wafer. As also shown in Table 1, reducing the bond width to 50 μm also reduces the necessary input power and the maximum heater temperature.

TESTING & RESULTS

In the first round of testing, bonds were made using differential heating to achieve a Au-Si eutectic bond. A Au-Si eutectic layer on the silicon *cap wafer* was bonded to a 5000 $\text{\AA}$ layer of gold on a glass *device wafer*. In Au-Si eutectic bonding, the temperature is raised to above the Au-Si eutectic temperature (363°C), causing silicon to diffuse into the Au bond ring. It then melts and can mate to either a polysilicon or a gold thin film [1].

In fabrication of the glass *device wafer*, a 1000 $\text{\AA}$ platinum layer was first deposited and patterned to form temperature sensors. A 5000 $\text{\AA}$ layer of plasma enhanced chemical vapor deposited (PECVD) Si_3N_4 was then deposited for electrical insulation. Finally a 5000 $\text{\AA}$ gold layer (which would later get bonded to) was evaporated and patterned over the top of the Si_3N_4 . On the *cap wafer*, 96 gold bond rings were electroplated onto a Cr/Au seed layer with a thickness of 4 μm . Each bond ring was 2.3x2.3 mm square, encompassing a 90 μm deep reactive ion etched (DRIE) cavity and had a 100 μm width—as in the case modeled. Furthermore, part of the *cap wafer* was diced away. Once the *cap* and *device wafers* were aligned, this allowed access to leads that were connected to the temperature sensors (Fig. 5b).

Figure 1 showed a cross-section of the wafer-level bonding test set up, where a 50 lb weight applies a 1 MPa pressure across the 96 bond rings arrayed across the wafer. After alignment of the wafers in a SUSS BA6 aligner, the two wafers were clamped with 4 small clips, placed on a copper heat sink, and wire bonded to two PCB as shown in Fig. 5a—thus providing connectivity to the temperature sensors.

According to the modeling results, bonding a silicon *cap wafer* with 96 bond rings to a *device wafer* made of either glass or silicon (with a 6 μm thick oxide) would require 2640 or 14400 Watts, respectively. Because of the large required heating power, an array of heaters was used, with each heater requiring a fraction of the total heating power to generate the required temperatures across the wafer. The heater array also allows heating of the different parts of a wafer to different temperatures. Figure 5c shows the heater arrays, laid out to heat 4 bond rings each. Heater arrays were fabricated by first evaporating a 0.75 μm film of Au onto a glass substrate. This thin film was patterned to form a 3x4 array of heaters on each wafer. Each heater consisted of a 100 μm wide, 700mm long, winding coil that encompassed a 10.5 x 13.3 mm area (as in the model). the heater substrate was diced into a 70 by 76 mm rectangle where two leads per heater ran out to bond pads at the periphery. In this manner, two heater substrates could encompass a 4" diameter wafer as in Fig. 5c.

The heaters and temperature sensors used in these experiments are essentially thin-film metal resistors that can

Figure 5: A picture of a) the leads which connect to the temperature sensors, b) the wafers sitting on the copper heat sink, c) two heater substrates sitting on top of the Cogethertm insulator plate, and d) the total assembly.

measure temperature, and that can heat up with a large input power. Before testing, the temperature coefficient of resistance (TCR) was measured for each of the heater and temperature sensor resistors. Figure 6 shows a view from the backside of the glass *device wafer* that was aligned to and clamped to the *cap wafer*. Each of the three temperature sensors in Figure 6 forms a 4-point probe, where the temperature is measured by applying a specified current across two of the leads and the voltage drop is measured across the other two. Given the measured TCR (where $\Delta T = [\Delta \text{resistance}] / [\text{initial resistance} * \text{TCR}]$) the temperature could be measured with a resolution of better than 1°C for the temperature sensors and heaters.

As illustrated in Fig. 6, there is a roughly 100 μm misalignment in the y-axis resulting in distances of 50, 100 and 600 μm between the temperature sensors and the bond ring. Figure 7 shows that for heater temperatures from 50 to 390°C, the temperatures measured at 50, 100 and 600 μm from the bond ring agree very well with those predicted from the model (the dashed lines in Fig. 7). Figure 8 shows temperature vs. time for the heater and at 50, 100 and 600 μm away from the bond ring. As demonstrated, it takes roughly 20 seconds to approach the steady state temperature and 5 second for the substrate to cool back down to room temperature.

To demonstrate that a bond could be achieved, two heaters were taken to approximately 110W with heater 1, achieving 446°C,

Figure 6: A view through the backside of the glass device wafer which was clamped to the Si cap wafer showing the 100 μm misalignment and temperature sensors at different distances from the bond ring.

Figure 7: A graph of the temperatures measured and predicted at the heater at 50, 100 and 600 μm from the bond ring where the dotted lines represent the predicted modeling results.

and heater 2, achieving 390 °C (this variation in temperatures could be due to a number of factors such as different contact resistances or their relative location near the center or periphery of the wafer). These temperatures were within 1% and 15% of the power predicted in the model (Table 1). After forcibly pulling the wafers apart, the bond rings were inspected. Figure 9 shows a bond ring before the bond experiment (Fig 9a); part of the horizontal *misaligned* portion, where the solder melted but had nothing to bond to (Fig. 9b); and part of the vertical *aligned* portion that mated with the gold and created a strong bond (Fig. 9c). Similar to Au-Si eutectic bonds in [1], Fig. 9c shows that when the wafers were pulled apart, silicon tore from the *cap wafer* and stuck to the *device wafer* via the Au eutectic layer—thus indicating a strong bond.

For the average temperatures of 446 and 390°C seen on heaters 1 and 2, the model predicts bond ring temperatures ranging from 410 to 474 °C and 353 to 407 °C. Therefore, all of the bond rings encompassed by heater 1 should melt/bond and only parts of the bond rings encompassed by heater 2 should melt/bond. This was confirmed in that under heater 1, 100% of the 4 bond rings melted and glass either transferred to the silicon wafer or silicon to the glass wafer in the *aligned* regions, whereas, under heater 2 roughly 80% of the 4 bond rings melted and either glass or silicon transfer was observed in the *aligned* regions. More extensive bonding tests will be conducted in the future.

CONCLUSION

A new method for localized heating of a bond region has been developed for bonding two wafers, while maintaining a low temperature where sensitive devices are located. In application of this technique, access is only required to the back sides of the two wafers, thus eliminating the need for access to wafer front side, as is sometimes needed in localized wafer bonding techniques. Integrated temperature sensors were used to measure temperatures at different distances from the bond region while making a Au-Si eutectic bond between silicon and glass wafers. Using a 3D ANSYS thermal model, the needed input power and temperature distributions were predicted for silicon to glass and silicon to silicon bonds. Using a heater array (10.5x13.3mm per cell), bonds were made on individual portions of the wafer using 110 Watts per heater to heat 4 bond rings at a time. When heating the bond ring to an estimated 410 to 475°C, the temperature 600 and 50 μm away from the bond region was measured and extrapolated to be 92 and 250°C respectively.

In future work, investigations will be made for silicon to silicon bonds using this bonding method. As illustrated from the

Figure 8: Temperature vs. time for the heater, and temperature sensors 50, 100 and 600 μm from the bond ring.

Figure 9: a) Misaligned Au on the cap and device wafers before bonding, b) after bonding. c) Silicon torn from the cap wafer, adhering to the device wafer via a Au-Si eutectic bond.

simulations, an oxide of around 6 μm (equivalent to the thermal resistance of some CMOS stacks) helps reduce the maximum heater temperature and the power necessary to achieve bond temperatures. Furthermore, this localized heating method may also be applied to other lower temperature solders.

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