A 0.8 μ m CMOS INTEGRATED SURFACE MICROMACHINED CAPACITIVE PRESSURE SENSOR WITH EEPROM TRIMMING AND DIGITAL OUTPUT FOR A TIRE PRESSURE MONITORING SYSTEM

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ABSTRACT

The development of an integrated process for the merging of a surface micromachined capacitive pressure sensor with a 0.8 μ m CMOS double metal, double polysilicon process is reported in this paper. A number of innovative pressure sensor designs with improved pressure linearity have been fabricated with this process. Designs with internal anchors and an optimum signal processing algorithm have demonstrated significant improvements in pressure linearity over more conventional designs. The system architecture and circuit implementation using EEPROM for pressure and temperature calibration are described. The results of the pressure and temperature behavior of the integrated sensors are described.

INTRODUCTION

The National Highway Transportation Safety Administration (NHTSA) is in the process of drafting a regulation (as of March, 2002) that will mandate some form of tire deflation monitoring, in response to the TREAD act, signed in 2000. The mandate is for this sensing capability to be in place by 2003. It is not yet clear whether differential wheel speed sensing in the ABS system or direct tire pressure monitoring (TPM) will prevail; however, it may be that both are needed for the near future (5-10 years). The direct TPM application is truly a micro-electro-mechanical system. Figure 1 shows an example of a microsystem with micromachined sensor, interface electronics, microcontroller, and rf output device. Motorola has developed a micromachined sensor device that is a CMOS-integrated (0.8 μ m) surface micromachined pressure and temperature sensor with digital output and is already in production with the MCU+RF in a single package. Furthermore, this package has an integrated harsh media compability packaging scheme built-in to provide protection from the tire environment.

Figure 1. Example of a tire pressure monitoring microsystem with micromachined sensor, interface electronics, microcontroller, and rf output device.

The TPM application, and drive to migrate from bipolar integrated pressure sensors to CMOS integrated pressure sensors, has prompted this development effort. The project is a system-level (MEMS) development. It includes the development of an integrated surface micromachined pressure sensor.

Other companies also have products that are targeted for the tire pressure monitoring market. Details of their product offerings can be found on their respective web-pages. Similar surface micromachined, CMOS integrated pressure sensor technology can be found for BiCMOS flows and CMOS technology [1-7]

In this paper, the CMOS integration of a surface micromachined capacitive pressure sensor into a 0.8 μ m double poly, double metal process is described [8]. The design and development of capacitive pressure sensors with considerably improved pressure linearity performance is also described [9]. The interface circuit for this capacitive sensor was designed to perform the calibration of the measured pressure and temperature using EEPROM. The interface circuit generates an output digital code for both the pressure and temperature sensor. The system configuration to form a TPM System is also described using a block diagram.

SYSTEM AND INTERFACE CIRCUITRY DESIGN

The system is designed for low power and low voltage operation. The supply range is from 3.6 to 2.1 V and is ratio metric. Low current consumption is used to allow battery operation for 10 years. In Standby mode only the low frequency oscillator runs to send a wake-up pulse to the MCU. Temperature measurement and DAC mode use less than 500 μ A. Pressure sampling consumes the most current at 1.5 mA, but uses high frequency bandwidth sampling to quickly return to sleep mode. This creates a larger noise bandwidth and shows the system constraints of power, noise, and speed. Algorithms can be used by the MCU to alleviate the design tradeoffs.

The control circuit function is to measure and calibrate pressure and temperature. The device performs an 8-bit A/D conversion of either signal. The MCU monitors the output and sets the control circuit's threshold for the conversion of the pressure or temperature to a digital signal or the detection of a specific threshold.

The pressure signal conditioning begins with a capacitance-to-voltage conversion using a nonlinearity reduction scheme in a switched capacitor amplifier. An EEPROM trim register is used to trim offset, gain, and temperature coefficients of the analog signal. Temperature is measured through a diffused resistor, with a positive temperature coefficient, using the same 8-bit current source that sets the threshold for the comparator. The EEPROM trim register trims the offset and gain. The pressure, temperature, and DAC signals are multiplexed to a sample

capacitor, which stores the value for A/D conversion. The wakeup pulse is multiplexed to the output pin with a parity check and the digital pressure or temperature output. A reset pin is used to hard reset the MCU and provide test vectors for circuit analysis. A block diagram representation of the system and the interface circuit is shown in Figure 2

Figure 2. Block diagram representation of interface circuit

TRANSDUCER DESIGN

The primary goals of the transducer design were the following: 1) Produce a sufficient base capacitance 2) Minimize pressure linearity errors 3) Maximize pressure sensitivity 4) Minimize the die area 5) Minimize temperature errors 6) Minimize the parasitic capacitance to the substrate

Perhaps the major design challenge for capacitive sensors is achieving a low linearity error, sufficient pressure sensitivity, and a small die size.

Traditionally, there has always been a trade-off between items 2 and 3; greater sensitivity usually produces larger linearity errors. Although linearity errors can be improved with reduced pressure sensitivity, more circuit gain is required, and circuit noise and other errors can increase. Thus, there is a desire to have a high pressure sensitivity and a low pressure linearity error, and therefore, other approaches were investigated to reduce linearity errors.

Figure 3. Figure 3 (a) Transducer using an internal post diaphragm design. (b) Transducer using a rectangular diaphragm design.

It is well known that first order linearization can be achieved by using a signal processing algorithm based on $1/C_s$, with C_s being the pressure sensitive capacitor element [1-2]. The signal processing algorithm used produces an output proportional to the quantity $1 - C_r/C_s$, with C_r being a fixed reference capacitor element. For an ideal C_r and C_s , i.e., C_r constant and C_s behaving

as a parallel plate capacitor with a linear pressure dependent gap, the linearity error can be substantially reduced. Using this algorithm, one major source of linearity error is non-uniform diaphragm deflection. Actual diaphragms are constrained at the edges, and this produces non-uniform deflection. As an example, a square diaphragm clamped at its perimeter and subjected to pressure has non-uniform deflection, with deflection greatest at the center, and zero at the perimeter. For this case the average deflection is only about 30% of the maximum deflection.

Figure 4. The pressure linearity error and normalized die area for several designs.

Finite element simulations were used to evaluate candidate diaphragm shapes for uniformity of diaphragm deflection. In addition to previously used shapes, such as circles and squares, “internal post” configurations were evaluated. Internal post designs anchor the diaphragm both at its perimeter and at internal locations. Simulations showed that some configurations of internal posts could produce more uniform diaphragm deflection, and significantly reduce linearity error at a given sensitivity level [7]. Figures 3(a). and (b). show photographs of an internal post design and a rectangular diaphragm design. Figure 4 shows the measured linearity error for several different design types. All designs have the same pressure sensitivity. The relative die area for the various designs normalized to the size of the Internal Post #1 design is also shown in this figure. The advantages of the internal post and the rectangular diaphragm designs are clear from the improved pressure linearity error and relatively small size.

PROCESS INTEGRATION

The process integration and fabrication of the CMOS integrated pressure sensor is described in this section. The details of the CMOS processing that are not relevant to the sensor integration have been omitted.

The methodology used in the insertion of the sensor module into the CMOS process was based on the requirements that there is no impact, either thermally or topographically, on the CMOS fabrication. This is done by insertion of the micromachining steps before the temperature sensitive process steps of the CMOS process. It was identified that the source/drain

implants and the subsequent thermal processing were the temperature sensitive steps. In addition, the process integration was designed to reuse, as much as possible, the fabrication steps of the CMOS process. The cross-section of the CMOS and sensor devices is shown in Figure 5 illustrating the key features of the process integration.

The fabrication process starts with the standard CMOS fabrication process in which the active areas are defined using an isolation field oxide using a LOCOS process. In addition to defining the active area of the CMOS devices, the field oxide is used as the area where the sensor is to be formed. The next step is the formation of the floating gate of the EEPROM. The required extension implant of the EEPROM is completed followed by the deposition of the thin tunnel oxide. The EEPROM floating gate is then deposited using a doped LPCVD polysilicon film. The floating gate polysilicon is patterned and etched so that it also forms the bottom fixed plate of the capacitive pressure sensor. The isolation of the fixed electrode to the substrate is provided by the CMOS field oxide isolation. The CMOS transistor gate oxide is then deposited followed by the gate polysilicon deposition.

Figure 5. Selected cross-sections of CMOS integrated capacitive pressure sensor process flow.

At this stage, the CMOS fabrication is suspended and the sensor fabrication steps are inserted. The first step is the deposition of a layer of PECVD oxide to protect the CMOS gate Poly from future sensor processing. The next step is the removal of the PECVD oxide, gate polysilicon and the gate oxide from the sensor area. This is done in such a way that the bottom polysilicon plate is not affected by the etching process. After the gate oxide is removed, an isolation layer of low stress silicon rich nitride is deposited using an LPCVD process. The silicon rich nitride is chosen for its excellent etch resistance to HF based chemistries. The silicon nitride is used to isolate the top and bottom plates of the pressure sensor and also protect the CMOS area from subsequent micromachining steps.

The sacrificial layer of the sensor is next deposited using a phosphorus-doped glass. The thickness of this layer defines the spacing between the bottom fixed electrode and the moveable diaphragm. The spacer layer is also patterned for transducer designs, which utilize internal support posts for improved pressure linearity. The sensor diaphragm is then formed by deposition of a LPCVD polysilicon layer. The polysilicon is then doped, patterned and etched to define the diaphragm.

The pressure sensitive diaphragm is then released by removing the sacrificial layer below the diaphragm polysilicon. Etch ports located at the periphery allow the HF based chemistry to completely remove the phosphorus-doped glass. The etch ports are then sealed using a line of sight sealing with a PECVD deposited oxide layer. The thickness of the PECVD oxide is chosen to ensure that the etch holes are plugged and the cavity between the fixed plate and the diaphragm is sealed at the deposition pressure of the PECVD oxide. This completes the formation of the sensor module.

The next step is the resumption of the CMOS fabrication process. This is done by first removing the sealing oxide, isolation nitride and protective oxide over the CMOS device area. The CMOS device formation is then resumed with the formation of the source/drain regions, and the subsequent thermal treatment to provide the activation anneal and definition of the junctions. This thermal treatment also serves to activate the dopants and provide the stress relief anneal in the sensor polysilicon film.

The first interlayer dielectric layer is next deposited, patterned and etched to allow for the subsequent first metal layer to contact the various CMOS devices as well as provide the interconnect for the sensor to the circuit. The second interlayer dielectric layer is then deposited, patterned and etched to form vias for the second metal to contact the first metal with the routing required for the circuit blocks. Finally, the passivation layer is deposited over both the CMOS and sensor device area. The passivation layer is then patterned and etched to expose the bond pads. In addition, the passivation layer, second, and first dielectric layers are then removed over the pressure sensitive element but not from the reference sensor element. This exposes the polysilicon diaphragm of the sensitive element leaving it free to deflect under an applied pressure. The reference element has very little deflection since it has a very thick composite diaphragm. Both the pressure sensitive element and the reference elements are used by the circuit to generate the output of the sensor. This completes the description of the process integration of the capacitive pressure sensor with the CMOS devices. Figure 6 shows a die picture of a typical CMOS integrated pressure sensor.

Figure 6. Microphotograph of CMOS Integrated pressure sensor

EXPERIMENTAL RESULTS AND DISCUSSION

The stand-alone pressure sensors designed for the tire pressure monitoring system were tested using a capacitive readout test setup. The capacitance vs. pressure characteristics were obtained for a large number of devices. A family of curves of Capacitance vs. Pressure for one of the designs is shown in Figure 7. The pressure sensitive devices a good linearity behavior with pressure while the reference devices do not show any pressure sensitivity as designed.

Figure 7. Family of capacitance versus pressure characteristics for pressure sensitive and reference devices.

The digital output data for the integrated devices were also obtained for a variety of designs over a wide range of temperature.

Figure 8. Digital output of a typical sensor with applied pressure at 25C.

Figure 8 shows a typical plot of the digital output count of a typical device as a function of the applied pressure at room temperature. The linearity, temperature coefficient of offset and sensitivity of the integrated devices were also measured. A summary of the performance of a typical device is given below in Table 1.0

Table 1.0 Performance summary of a typical device

Pressure Range	Temperature Range	Full Scale Output	Pressure Linearity Error	TC Offset	TC Sensitivity	Thermal Hysteresis
[kPa]	[C]	[Counts]	[%FSS]	[Counts/C]	[%FSS/C]	[%FSS]
0 to 637.5	-40 to 125	0 to 255	-1.5	0.01	-0.005	0.04

CONCLUSIONS

The development of a CMOS integrated surface micromachined capacitive pressure sensor for a tire pressure monitoring system has been reported in this paper. The design of pressure sensors with improved pressure linearity as well as a block diagram description of the interface circuitry has been described. The process integration steps for inserting the pressure sensor into a double poly, double metal CMOS process was described. The performance of the pressure sensor devices itself was presented. In addition, the digital output behavior of the interface circuit for both the pressure sensor and temperature sensor was presented.

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