MICROMACHINED JET ARRAYS FOR LIQUID IMPINGEMENT COOLING OF VLSI CHIPS

Evelyn N. Wang, Lian Zhang, Linan Jiang, Jae-Mo Koo, Kenneth E. Goodson, and Thomas W. Kenny
Mechanical Engineering, Stanford University
Stanford, CA 94305-4085

James G. Maveety and Eduardo A. Sanchez
Intel Corporation
Santa Clara, CA 95052-8119

ABSTRACT

Two-phase cooling of VLSI chips with microjet heat sinks promises a new, effective heat removal method. Microjet arrays can achieve improved temperature uniformity in the presence of chip hotspots. This paper describes the development and assesses the performance of micromachined single and multi-jet arrays with orifice diameters less than 100 μm . The devices were tested in a confined geometry with a dedicated heater test chip, as well as in an open geometry with a standard 1 cm^2 Intel test chip. In the confined geometry, a 76 μm diameter four-jet array at a flow rate of 8 ml/min removed over 90 W/cm^2 . Experimental comparisons of microjet and microchannel performance show that microjets have improved thermal uniformity, offer a significantly more stable two-phase region, and do not exhibit superheating. These advantages suggest that microjet arrays are the preferred micro heat sinks for effective device cooling.

INTRODUCTION

The continuing increase in the power density of VLSI chips necessitates the development of novel heat removal technology. Thermal resistances less than 0.1 $^\circ\text{C/W}$ for heat sinks will be required in the next few years [1]. Micromachined heat sinks such as microchannels and microjets are compact and offers low thermal resistances [2]. However, microjet impingement has been of particular interest because the direct cooling onto the chip surface eliminates conduction resistances associated with the packaging and promises high heat removal rates. Furthermore, with microjet arrays, greater surface temperature uniformity can be achieved.

Past microjet research has focused on single-phase air impingement, which provides relatively low heat removal rates. Single and multi-air jet arrays with orifice diameters ranging from 50-800 μm have been studied [3-6], including integration with heat sink modules [5] and actuation by magnetically driven membranes [6]. Heat transfer coefficients of 2500 $\text{W/m}^2\text{K}$ were achieved with 1.3E7 ml/min air flow rate [4].

Two-phase liquid microjet impingement is advantageous because the latent heat associated with phase change of the working fluid can be utilized to yield higher heat transfer coefficients. Macro scale jets with diameters greater than 0.28 mm using two phase heat transfer has been extensively studied in the past with several liquids, including water, R-113, and RC-72 [7]. Our past work characterized single microjet liquid impingement with orifice diameters less than 50 μm in an open geometry, and demonstrated removing over 40 W/cm^2 . Heat

transfer coefficients of 2200 $\text{W/m}^2\text{K}$ at 2-3.5 ml/min water flow rate were attained [8].

In this paper, heat transfer performance of single and multi-jet arrays with orifice diameters less than 100 μm is examined in confined and open geometries. The characterization of these microjets allows comparison with past microchannel research to investigate the advantages of using microjet heat sinks for future chip cooling. This work aids in developing an optimal design for micro heat sinks in closed-loop, pumped cooling systems.

DESIGN AND FABRICATION

The fabricated single and multi-jet arrays have circular orifice diameters ranging from 40 μm to 76 μm . The lengths of the jets are 300 μm . The fabricated test heater chip emulates a high power VLSI chip with an effective heating area of 1 cm^2 . As shown in Figure 1, seven polysilicon doped resistance thermometers are defined along the centerline to measure the one-dimensional chip surface temperature profile. Because the resistance of doped polysilicon changes as a function of temperature, the surface temperature can be monitored as a function of the resistance change through calibration. The heater has a resistance of 500 Ω and the thermometers have a resistance of 7 $\text{k}\Omega$ each, with a temperature sensitivity of ranging from $-6 \Omega/^\circ\text{C}$ to $-20 \Omega/^\circ\text{C}$. On the other side of the heater chip, a 1 cm^2 , 200 μm deep reservoir collects the impinging water from the jets.

Figure 1. Schematics of the top and cross-sectional views of a bonded confined jet impingement test chip, consisting of a four-jet array and a heater chip. The crosses on the top view show the configuration for the four-jet array.

The design and fabrication for both the jet and heater devices are similar to the ones described in [8]. However, the previous devices were only tested in an open geometry, where the fluid was not contained. The configuration is not practical for realistic microelectronic applications due to electrical shorting problems. In this study, the heater and jet chips described above are bonded together to form a confined geometry test chip. The chip fully encloses the impinging liquid and there are clear fluidic inlet and outlet paths. Figure 1 shows a schematic of the bonded test chips. The fluid enters the inlet to the jet chip, and after jet formation, fluid impinges onto the heater surface, and the heated fluid is collected from the outlet. The jet orifice to the heater surface separation is 200 μm .

Detailed fabrication procedures for these jet and heater chips are described in [8], so the steps will be discussed briefly here. For the jet chips, the jets are first formed by deep reactive ion etching (DRIE) into single crystal silicon substrates. From the backside, a deep reservoir and inlet are then plasma etched. Finally, to seal the inlet and reservoir, a Pyrex glass slide is anodically bonded to the silicon substrate. For the heater chips, the outlet and reservoir are plasma etched with DRIE into single crystal silicon substrates. A nitride insulation layer is deposited. Polysilicon is then deposited, doped with Boron, and annealed to form the resistors. Finally, aluminum is deposited to form electrical contacts to the resistors. Once the jets and heater chips are fabricated, they are bonded together using 5-minute cure epoxy to make confined geometry test chips.

EXPERIMENTAL SETUP

The experimental setup for testing the microjet heat sinks is shown in Figure 2. The syringe pump continuously delivers deionized water to the test fixture. Water was chosen because it has a high latent heat of evaporation. A pressure sensor at the entrance to the test fixture monitors the pressure drop across the jets.

Figure 2. Schematic of the experimental setup with the Intel standard test chip board. For the confined geometry jet experiments, the jet test fixture and thermal chip board are replaced with the bonded chip and fixture.

Measurements were performed using a dedicated fixture for the confined geometry test chips that fully encloses the impinging liquid, as well as with another fixture for the open geometry

experiments with a 1 cm^2 Intel test chip. In both cases, the fixture clamps the jet test chip, and an O-ring seals the inlet.

Figure 3(a) is a picture of the bonded test chip with its designated fixture. A small printed circuit board is glued onto the resistor side of the heater chip, so that electrical connections can be made from the aluminum contacts on the chip to a breadboard, where the resistances are measured. The heated water from the outlet is collected into a reservoir. Figure 3(b) shows the open geometry test fixture to which the microjet array is attached. The Intel test chip board is placed directly under the fixture. Because the experiments are performed in an open geometry, slots on the chip board allow the excess fluid to flow into a reservoir below the board. The Intel 30 W thermal chip with an area of 1 cm^2 has a temperature sensor at the chip center, which measures the average surface temperature. This test chip is analogous to a Pentium 4 processor chip and is a standard test chip currently used for experiments with metal heat sinks.

The data from these experiments are collected by a 16-bit 16-channel PCMCIA A/D card through a signal conditioning circuit. The measurements are recorded by LabView.

(a). Fixture for bonded jet experiments. The jet chip is on top, and the heater chip is on the bottom with the wire-bonded printed circuit board to make electrical contacts to the resistors.

(b). Fixture for Intel setup, which is placed directly on top of the Intel thermal chip board.

Figure 3. Pictures of test fixtures for confined and open geometry experiments.

EXPERIMENTAL RESULTS

The effects of using a single and a four-jet array to distribute cool fluid over the hot surface in the confined geometry were examined. Data are provided for varying levels of power and as a reference, for the case of no liquid impingement. Figure 4(a) clearly shows a distinct temperature drop at the impingement point on the chip surface, located at 5mm. For the case of the jet array, as shown in Figure 4(b), with the same liquid flow rate per jet (2 ml/min), the temperature profile along the centerline of the chip is more uniform. These confined jets use a combined cooling effect of both jet impingement and forced convective flow. As a

result, the fluidic removal route introduces the asymmetry in both of the temperature profiles because the heated water flows toward the outlet. The outlet is located on the right end of the graphs, which results in the chip surface temperatures to be the highest near that region.

(a). Temperature profile for a single jet. The impingement point is located at 5 mm. The data are for a flow rate of 2ml/min with a pressure drop of 5.4 psi.

(b). Temperature profile for a jet array. The data for flow rate of 8ml/min with a pressure drop of 6.9 psi.

Figure 4. One dimensional temperature profiles for a single and an array of four 76 μ m diameter jets. The data with no jet is taken for comparison.

In Figure 5, the average temperature rise of a single jet and the four-jet array are compared as a function of the applied power. The experimental results confirm the anticipated surface temperature behavior. There is an initial linear temperature rise indicating a combination of forced convection and jet impingement single-phase heat transfer. The temperature plateau signifies the two-phase heat transfer region where the latent heat is being used. The final sharp temperature rise is due to dry out. The flow rates for the single jet and jet array could not be directly compared, because each jet requires a certain flow rate in order to form a jet stream [8]. However, the results show that as the flow rate is increased, more power can be removed. The 76 μ m diameter four-jet array removes 92 W/cm² with an 80°C temperature rise at a flow rate of 8 ml/min and 6.9 psi pressure drop. The estimated heat transfer coefficient for the four-jet array is over 10,000 W/m²K at 8ml/min. Higher flow rates and a more

optimized heat sink design will facilitate even higher heat flux removal and heat transfer coefficients.

Figure 5. Comparison of average chip surface temperature with increasing power for a single 76 μ m diameter jet to a 76 μ m diameter four-jet array in a confined jet configuration.

COMPARISONS TO MICROCHANNEL PERFORMANCE

Figure 6. Comparison of temperature uniformity for a single channel and a four-jet array. The single channel is 74 μ m wide, 52 μ m deep, 76 μ m hydraulic diameter tested at 0.1ml/min flow rate [9]. The jet array consists of four 76 μ m jets tested at 8ml/min.

To assess the advantages of microjet heat sinks, the performance of single jets and multi-jet arrays is compared with the results of our past microchannel research [9, 10] using our own heater chips with integrated thermometer and a standard Intel test chip. Figure 6 compares the temperature uniformity along the length of the heated area for a single 61 μ m hydraulic diameter microchannel and a four 76 μ m diameter jet array. The channels and jets were not fabricated and tested with the intention of a direct comparison, so the scaling is normalized to account for the differences in power levels and thermometer placement of the heated area. Steeper temperature gradients are present in the microchannels than in the jet array and maximum temperature difference of 47 °C at 2.6 W is recorded due to the lateral fluid motion in the channels.

Figure 7 compares the performance of forty parallel microchannels with a hydraulic diameter of 100 μ m [10] to a single 70 μ m diameter jet at similar flow rates using the standard Intel test chip. The microchannels are placed directly on top of

the thermal chip with thermal grease. The results show that microjets are more effective because they can remove larger heat fluxes at lower surface chip temperatures. Also, the surface temperature plateau observed in microjet impingement is more stable and more easily attainable, indicating better chip temperature uniformity. The temperature fluctuations in the two phase region are a result of the open geometry, and can be eliminated with confinement. In addition, wall superheating of almost 30°C is apparent in the microchannels, which is not present in the microjets.

Figure 7. Average surface temperature measured with increasing power for microchannels and microjets at comparable flow rates. A single 70 μ m diameter jet has a pressure drop of 6.7psi pressure drop. Forty parallel microchannels have dimensions of 100 μ m width, 100 μ m depth, and 15 mm in length.

CONCLUSIONS

This paper presents new heat transfer measurements with microfabricated jet arrays in a confined geometry. Heater chips with thermometers are fabricated to measure the local temperature distribution and to study the effects of using single jets and multi-jet arrays in two-phase liquid impingement cooling. A careful comparison of uniformity and heat transfer in microchannels and microjets shows clear advantages for the microjets, including a stable two-phase region and the absence of superheating. Removal of 90 W/cm² is demonstrated at a flow rate of 8 ml/min using a microjet array, extending our performance to meet most upcoming industrial requirements for microprocessor packaging.

ACKNOWLEDGEMENTS

This work is supported by DARPA HERETIC Program under DARPA Contract F33615-99-C-1442, National Defense Science and Engineering Graduate Fellowship (Evelyn Wang), and Stanford Graduate Fellowship (Lian Zhang). The project made use of the National Nanofabrication Users Network facilities funded by the National Science Foundation under award number ECS-9731294. Travel support has been generously provided by the Transducers Research Foundation and by the DARPA MEMS and DARPA BioFlips programs.

REFERENCES

1. C. D. Patel, "Enabling Pumped Liquid Loop Cooling: Justification and the Key Technology and Cost Barriers,"

Proceedings of 2000 International Conference on High-Density Interconnect and Systems Packaging, Denver, CO, USA, April 25-28, 2000, pp.145-152.

2. D. B. Tuckerman and R. F. W. Pease, "High-Performance Heat Sinking for VLSI," *IEEE Electron Device Letter*, EDL-2, 126-129, (1981).

3. S. Wu, J. Mai, Y. C. Tai and C. M. Ho, "Micro heat exchanger by using MEMS impinging jets," *Proceedings of the IEEE Micro Electro Mechanical Systems (MEMS)*, 171-176, (1999).

4. Q. Lin, S. Wu, Y. Yuen, Y. C. Tai and C. M. Ho, "MEMS Impinging-Jet Cooling," *Proceedings of 2000 ASME International Mechanical Engineering Congress and Exposition*, Orlando, FL, USA, Nov. 2000, pp.137-142.

5. S. Stefanescu, M. Mehregany, J. Leland and K. Yerkes, "Micro jet array heat sink for power electronics," *Proceedings of the IEEE Micro Electro Mechanical Systems (MEMS)*, pp.165-170.

6. D. J. Coe, M. G. Allen, B. L. Smith and A. Glezer, "Addressable micromachined jet arrays," *International Conference on Solid-State Sensors and Actuators, and Eurosensors IX, Proceedings*, 2, 329-332, (1995).

7. D. Wolf, F. P. Incropera and R. Viskanta, "Jet Impingement Boiling," *Advances in Heat Transfer*, Academic Press, New York, 23, pp.1-132, (1993).

8. L. Zhang, et al, "Microscale Liquid Impingement Cooling," *Proceedings of 2001 ASME International Mechanical Engineering Congress and Exposition*, New York, NY, USA, November 11-16, 2001, pp.23820.

9. L. Zhang, et al, "Enhanced Nucleate Boiling in Microchannels," *Fifteenth IEEE International Conference on Micro Electro Mechanical Systems*, Las Vegas, Nevada, U.S.A, January 20-24, 2002, pp.89-92.

10. L. Jiang, J.-M. Koo, S. Zeng, J. Mikkelsen, L. Zhang, P. Zhou, J. Maveety, A. T. Quan, T. W. Kenny, J. G. Santiago and K. E. Goodson, "Two-phase microchannel heat sinks for an VLSI cooling system," *Seventeenth Annual IEEE Semiconductor Thermal Measurement and Management Symposium*, San Jose, CA USA, March 20-22, 2001, pp.153-157.