Ultra Deep Anisotropic Silicon Trenches Using Deep Reactive Ion Etching (DRIE)

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Abstract. This paper reports solutions to the problem of profile control of narrow trenches in the vicinity of wider topographic features, as well as for etching high aspect ratio, anisotropic trenches with depths in the 300 to 500 μm range, and of widths between 12 to 18 μm .

Background.

Deep Reactive Ion Etching (DRIE) is being increasingly recognized as an enabling MEMS technology [1] and it is, in fact, playing a crucial role in the emerging field of Power MEMS [2]. An extensive characterization database has been reported recently [3, 4] for tailoring operating conditions in order to obtain prescribed profiles as well as targeted silicon etching rates and uniformity when using a DRIE tool that employs the Bosch process. This technique can be briefly described as consisting of sequential etching and passivating steps using an appropriate gas chemistry in each step (SF_6 for etching, C_4F_8 for passivating). However, solutions to the problem of etching high aspect ratio trenches located in the vicinity of wide trenches that locally deplete the availability of etching species are absent in the literature. Furthermore, the issue of etching highly anisotropic, narrow silicon trenches (measured widths of 12 to 18 μm) with etched depths in the range of 300 to 500 μm has not been scrutinized and no reported practical guidance can be found in this respect.

Narrow Trenches Adjacent to Wide Features

This exercise involved 4" single crystal silicon wafers, $\langle 100 \rangle$, standard thickness, n-type, with resistivity 10-20 $\Omega\text{-cm}$. The masking material was photoresist AZ4620 spun at 3000 rpm (thickness $\approx 6 \mu\text{m}$). The mask consisted of arrays of trenches 3 to 5 μm wide adjacent to trenches 30 to 50 μm wide. The separation between the trenches was 10 to 15 μm , and the length of all trenches was fixed at 2000 μm . The exposed area was estimated at 10%. Etching was performed in a time multiplexed etcher from Surface Technology Systems that has been described elsewhere [3, 4].

While it is possible to locate reported operating conditions enabling users to obtain high silicon etching rates [3, 5], i.e., in excess of 3 $\mu\text{m}/\text{min}$ and with reasonable etching selectivities, i.e., exceeding 70:1, and good anisotropy, it is frequently observed that it is problematic to

etch high aspect ratio trenches in the vicinity of wide trenches because the latter locally decrease the availability of etching species as shown in figure 1.

Figure 1. It is common to encounter problems while etching narrow trenches in the vicinity of wide features. Operating conditions were: 105 sccm of SF_6 (15 sec active cycle, 1 sec overlap, 12 W electrode power and 600 W of coil power), 20 sccm of C_4F_8 (11 sec of active cycle, 6 W electrode power and 600 W of coil power), the APC set at 65°. Etching conditions known as MIT47. This operating point has also been reported as producing smooth walls [5].

Additional steps have to be taken to regain control of the profile in applications exhibiting such geometries. One solution to this problem is to increase the ion flux reaching the wafer surface during the etching cycle to promote a more efficient removal of the protective polymer layer at the

bottom of the trench. The ion flux is controlled by the applied coil power during the corresponding cycle [3, 4], thus, subsequent process optimization studies concentrated on this variable. Figure 2 illustrates the dramatic improvement obtained by using the aforementioned approach.

Figure 2. Results obtained after optimization of the operating conditions for etching narrow trenches (width = $3.7\text{ }\mu\text{m}$) in the vicinity of wide trenches (width = $38\text{ }\mu\text{m}$). Operating conditions were: 105 sccm of SF_6 (14 sec active cycle, 0.5 sec overlap, 12 W electrode power and 750 W of coil power), 40 sccm of C_4F_8 (11 sec of active cycle, no overlap, 6 W electrode power and 600 W of coil power), the APC set at 65° . Etching conditions known as MIT59. Trenches observed to widen at the rate of approximately $1\text{ }\mu\text{m}$ for every $100\text{ }\mu\text{m}$ etched down.

The set of operating conditions known as MIT59 described in figure 2, has found widespread application in accelerometers [6], micro-gas turbine engines [7], tethered motors [8], Power MEMS [9] and, in general, for etching through wafers.

Other variations of MIT59 have been used to etch through wafers with thickness in excess of $525\text{ }\mu\text{m}$. In these instances the strategy is to lower the electrode power during the etching cycle from 12 W to 10 W (variation known as MIT69) [10], thereby increasing the selectivity at the

expense of a slight deterioration in etching rate and anisotropy. By increasing the coil power during the etching cycle to 800 W (variation known as MIT56) it has been possible to fabricate successfully $10\text{ }\mu\text{m}$ wide trenches up to $200\text{ }\mu\text{m}$ deep. These trenches are important in forming forward and aft thrust nozzles for microturbomachinery applications [7, 11].

Ultra Deep Trenches

The mask used in these experiments consists of an array of 12 circular trenches with a diameter of $4200\text{ }\mu\text{m}$ and measured width of $10\text{ }\mu\text{m}$ after photolithography. Standard vacuum theory applied to narrow (width $\leq 13\text{ }\mu\text{m}$), very high aspect ratio (>15) silicon trenches, reveals that the conductance of these features decreases (see figure 3) as the depth of the trench increases [12, 13]. Decreasing the conductance of the trench impedes both the transport of etchant species to the surface bottom and the removal of etching byproducts [13-15]. The combined effect is reflected in the noticeable profile deterioration when depth increases beyond $200\text{ }\mu\text{m}$, as shown in figure 4.

Figure 3. As the depth of etched trenches increases, the neutral flow conductance decreases drastically, affecting trench profile and silicon etching rate.

This problem can be alleviated by dynamically compensating the neutral flux reduction reaching the feature bottom during processing and by quickly removing the etching byproducts that dissociate and redeposit. This type of control is natural in tools employing the Bosch process because in the standard mode of operation, the throttle or

automatic pressure control (APC) valve remains fixed and the chamber pressure is controlled by the flow rate of the respective gas species during the etching or passivation cycles. Thus, the pressure during the etching cycle can be systematically increased throughout a particular process simply by increasing the SF₆ flow rate (see figure 5). The chamber pressure sets the neutral flux via the following,

$$N_f = p / \sqrt{2\pi m K_B T},$$

where N_f is the neutral flux, p the chamber pressure, m the mass of the neutral species and T its temperature. Additional advantages of operating at higher pressures include higher collisional and dissociation rates which increase the availability of etching species. The higher SF₆ flow rates associated with high pressure operation facilitate the replenishing of etching species and the quick removal of etching byproducts. Thus, increasing the SF₆ flow rate was the approach selected to locate processing conditions that permitted the repeatable microfabrication of trenches with depths in excess of 300 μm , with measured widths ≤ 13 μm and good profile control, as the trench shown in figure 6.

Figure 4. Trench profile quickly deteriorates as the depth of a high aspect ratio trench increases. The trench in the left SEM micrograph was obtained during a 4-hour etch using MIT56. Profile deterioration becomes more noticeable as the depth extends beyond 300 μm as can be observed in the right SEM micrograph. At its widest point, the trench on the right measured ~ 20 μm .

These trenches serve as journal bearings [7, 11] for microturbomachinery elements rotating at speeds in excess of 10^6 rpm, for which, the profile is critical for achieving the

desired performance. The manufacturer of the etching tool used in this work now offers software controlled upgrades that allow the automatic modification of operating conditions during etching using parameter ramping schemes [16]. However, the equipment utilized in this work lacked such capabilities and the processing variations were implemented by creating a process with a number of 60-minute steps where the SF₆ flow rate was monotonically increased by 2 sccm, every 1-hour step.

Figure 5. By increasing the SF₆ flow rate during processing, the chamber pressure is increased, and, consequently, the neutral flux to the wafer surface is increased. Residence time is given by pV/f , where V is the chamber volume (36 l) and f the SF₆ flow rate.

The carefully selected operating conditions described herein, have also been tested on trenches reaching depths in excess of 500 μm . One example of such an effort is shown on the right SEM micrograph in figure 6. As the depth of etched trenches extends beyond 300 μm , it is increasingly more difficult to control the anisotropy of narrow, high aspect ratio silicon trenches, note, however, that it is feasible to produce profiles with a slight positive taper that are acceptable for many applications (see figure 6, SEM micrograph on the right). It is thought that the profile variation for trenches with depths in excess of 500 μm , can be understood in terms of the widening of the ion angular distribution function at the entrance of the trench due to the increased chamber pressure, and also to the loss of ion flux reaching the feature bottom as the depth of the trench becomes a larger fraction of the mean free path typical at these operating pressures.

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Figure 6. Operating conditions are based on MIT56, with +2 sccm increase in SF_6 flow rate every hour. The average width of the trench is about $11.8 \mu\text{m}$. Normally, a 4-hour etch delivers a 315-320 μm deep trench.

Conclusions.

We have demonstrated the ability to control the profile of narrow trenches ($\leq 5 \mu\text{m}$) in the vicinity of much wider features by tailoring the ion flux reaching the wafer surface. We have also demonstrated the etching of ultra deep anisotropic silicon trenches in the range of 300 to 500 μm by dynamically controlling the neutral flux arriving at the wafer surface during processing.

Together, the manufacturing processes described herein are critical for the construction of micro-turbomachinery and bi-propellant micro-rocket engines.