Application of Micromachining Technology to Lateral Field Emission Devices

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Abstract - We demonstrate a range of novel applications of micromachining and microelectromechanical systems (MEMS) in achieving efficient and tunable field emission devices (FEDs), and in improving their ease of integration. In each case, arrays of lateral field emission tips are fabricated with submicron spacing utilizing deep reactive ion etch (DRIE). Tip density of over $150 \cdot 10^6$ tips/cm² can be achieved, and current of over 150 A/cm². By utilizing sacrificial sidewall spacing, electrodes can be placed at arbitrarily close distances. We further utilize MEMS actuators to laterally adjust electrode distances. To improve integration capability of the FEDs, we demonstrate batch bump-transfer integration of working FEDs onto a quartz target substrate.

I. INTRODUCTION

The research field of vacuum microelectronics strives to combine the best features of highly advanced solid-state fabrication technology and vacuum tube electronics [1],[2]. The goals and potential applications vary from high-temperature and high-radiation amplifiers; RF oscillators and amplifiers and field emitter displays [2]-[7], to a variety of sensors such as ion gauges [6]. To date, the proposed and fabricated field emission devices (FEDs) have been largely divided into two groups: vertical and lateral structures. Vertical FEDs were frequently fabricated by the use of silicon or Spindt-type metal tips [5]. To our knowledge, the achievable currents per device with silicon as emitting material have been limited to below or the order of 1 μ A. Hence, in most proposed applications, large field emitter arrays (FEAs) of up to tens of thousands of tips are required to achieve milliamps of electron current. Significantly higher currents have been achieved by the use of metals with lower work functions [5]. FEAs are commonly characterized by turn-on voltages above 60 Volts.

Lateral field emission devices (LFEDs) [7]-[9] may have many advantages in high-speed and RF applications owing to the simple fabrication, precise control of electrode distances, and lower capacitance. They have been demonstrated with relatively high current densities and turn-on voltages as low as 22 Volts [9]. Lateral silicon emitters with currents on the order of tens of microamps per tip have been demonstrated.

Utilization of micromachining technology presented in this work allows for more than an order of magnitude increase in achievable current for each individual device than in the previous work with silicon emitters. With the use of deep reactive ion etch [10],[11] (DRIE) which cyclically alternates between etch and deposition steps forming scalloped sidewalls, each fabricated lateral device can consist of dozens of tips vertically stacked with <0.5 μ m distance. The methodology is very simple, and requires only 1 mask and 1 trench etch with DRIE. It also provides for very accurate electrode distance control via photolithography, oxidation self-alignment, or sacrificial sidewall spacer self-

alignment. These are discussed in detail in Sec. III. Diodes with turn-on voltages between 25 and 40 V emitting currents up to 400 μ A were fabricated in a 2 μ m process.

The new approach is moreover directly integrateable with MEMS actuators which provide a *mechanical tuning* feature and open numerous possibilities in the area of inertial sensing. Electrodes can be placed at closer, arbitrary distances by lateral actuation using comb drive, gap-closing, or thermal actuators as described in Sec. IV.

Finally, the approach provides integration capability for these types of devices by implementing batch-transfer methodology for fully fabricated diodes and triodes. This methodology, described in detail by Maharbiz *et al* [12] has the advantage of decoupling circuit and MEMS processes. In our case, CMOS fabrication can therefore be completed independently of FED fabrication on separate wafers and in separate, optimized, processes. After completion of both processes, FEDs are batch-transferred onto the CMOS wafer for integration with sense/drive and digital circuits. The methodology and results are detailed in Sec. V.

II. THEORETICAL BACKGROUND

Emission of electrons from a cold metal cathode is characterized by the Fowler-Nordheim tunneling equation [13]. In most cases the equation closely approximates current-voltage characteristics for relatively highly doped semiconductors and is frequently used to extract physical parameters such as cathode sharpness, material work function, and field enhancement factor. We utilize an approximation by Spindt *et al* [4] of the current I in terms of the operating voltage V , work function ϕ [eV], emission area α [m²] and the local field conversion factor β [m⁻¹]:

$$I = aV^2 \exp(-b/V), \quad (1)$$

where

$$a = \frac{\alpha A \beta^2}{1.1\phi} \exp\left(\frac{1.44 \times 10^{-7} B}{\phi^{1/2}}\right), \quad (2)$$

$$b = 0.95 B \phi^{3/2} / \beta$$

and A and B are dimensionless constants, $A = 1.54 \times 10^6$ and $B = 6.87 \times 10^7$. The parameter β can be expressed as the ratio of field enhancement to the cathode-anode distance

$$\beta = \frac{\kappa_{tip}}{d_{cathode-anode}}. \quad (3)$$

The dimensionless κ_{tip} represents the geometrical enhancement of electric field E [V/m] at the emitter tip due to its small radius of curvature, $\kappa_{tip} = E/(V/d)$. In the high voltage regime, the exponential term in the current equation may be neglected and current is simply $I = aV^2$. Integration of FEDs with MEMS actuators allows for electrode distance adjustment and modulation. To understand these effects on current, we differentiate current in high voltage regime with respect to d ,

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yielding:

$$\begin{aligned} \frac{\partial I}{\partial d} &\approx V^2 \cdot \frac{\partial a}{\partial d} = \frac{2\alpha\beta AV^2}{1.1\phi} \exp\left(\frac{1.44 \times 10^{-7} B}{\phi^{1/2}}\right) \frac{\partial \beta}{\partial d} \\ &= -\frac{2\alpha AV^2}{1.1\phi} \exp\left(\frac{1.44 \times 10^{-7} B}{\phi^{1/2}}\right) \frac{\kappa_{ip}^2}{d^3} \end{aligned} \quad (4)$$

As evident in the equations above, there are five physical ways of increasing the emitted current:

- 1) Increasing voltage
- 2) Decreasing inter-electrode distance
- 3) Decreasing material work function by increasing the dopant concentration in the n-type silicon or by changing materials
- 4) Increasing the effective field at the tip through sharpening
- 5) Increasing the number of tips in a given area, i.e. tip density

Our fabrication efforts, as detailed in the Sec. III, are directed at simple and low-cost ways of optimizing 2), 4), and 5).

III. DEVICE FABRICATION AND CHARACTERIZATION

A. Deep reactive ion etch for tip fabrication

This method of tip fabrication is based on the cyclical nature of the time multiplexed inductively coupled plasma etch (DRIE) [10], i.e. the patented Bosch process [11]. The process etches deep, high aspect ratio trenches in silicon by alternating an SF_6 plasma etch with a teflon-like C_4F_8 deposition. As a consequence, trench sidewalls are not smooth but undulate with the process' periodicity with so-called sidewall *scallops*, as illustrated in Fig. 1b and also shown in Figs. 2 and 3. The scallop is commonly an undesired property of DRIE. However, when the mask layout defines an acute angle as shown in Fig. 1a, two scalloped sidewalls meet at the corner of the structure and form relatively sharp tips. Therefore, with a simple layout as shown in Fig. 1a and a single etch of an SOI wafer down to the oxide etch-stop, a field-emission diode is obtained with dozens of tips vertically stacked at submicron distance. Varying etch and deposition time in the etch cycle results in varying vertical tip density. Three of the recipes used were characterized in a SEM and yielded the results listed in Table 1. The highest vertical tip density achieved to date is ~ 3 tips/micron. When mask layout includes many such devices at small lateral spacing (e.g. in Fig. 12,) extremely high overall tip density is achieved. If, for example, a $50 \mu\text{m}$ thick SOI wafer is used each edge includes ~ 150 tips, and since there would be 5000 such edges/cm length (at $2 \mu\text{m}$ spacing), a total of 750,000 tips would result. This methodology, based on present achievements can therefore fabricate $150 \cdot 10^6$ tips/ cm^2 . We believe that further optimization of the vertical etch process and most recent photolithography can far exceed this estimate.

Tip depth is a function of layout tip sharpness. Even with high density recipe, tip depths in excess of 900 nm have been achieved. Radii of tips following DRIE vary between 15 nm and 30 nm. While apparently sharp, such tips have turn-on voltages well over 100 V rendering them inadequate for low-power FED applications. Images of tips formed with each of the three recipes are shown in Figure 2. All three SEMs were taken at a magnification of 40k.

For a given recipe, tip density and depth varies visibly down the device. In a final device, this affects the cathode-anode distance and consequently the turn-on voltage of individual tips. The variation is up to the order of 100 nm, and its overall effect is still being investigated. We believe, however, that when devices are operated in the high voltage regime all tips contribute

Figure 1. Fabrication of LFEDs by DRIE etching of SOI wafers: (a) microphotograph of the top view of a diode test structure, and (b) schematic cross-section of the SOI wafer.

DRIE tip recipe	SF_6 etch time [s]	C_4F_8 dep. Time [s]	Vertical tip dens. [μm^{-1}]	Tip Depth [nm]
High density	6	5	2.9 - 3.1	350 ± 70
Std. density	9	7	2.0 - 2.2	510 ± 50
Low density	14.3	11	1.3 - 1.5	700 ± 100

Table 1. Details of different DRIE tip recipes. In all recipes, the overlap time between etch and deposition is 0.5 seconds. Quantities are for layout of 60 degree tips. In all cases, coil power=600 W, platen power=120W, and SF_6 flow=130 sccm.

Figure 2. Three SEM images taken at the same magnification: (a) low density tips, (b) standard density tips and (c) high density tips.

to the total current nearly equally.

Depending on the mask layout, two types of geometry can result after the etch. In one case, as in Fig. 2, the anode is separated from the cathode in the layout and does not affect the formation of the tips. The electrode distance in that case is defined photolithographically. In the case where there is a slight ($< 0.5 \mu\text{m}$) overlap in the mask, the etch results with the form shown in Figure 3, where cathode and anode electrodes are not separated, but connected via silicon nanowires. Oxidation and subsequent oxide removal, as detailed in Sec. IIIB, results in self-aligned cathode and anode where both sides are lined with sharp

Figure 3. Silicon nanowires extend between blocks overlapping in layout. DRIE alone does not result in tips with submicron spacing.

B. Oxidation sharpening

To increase the electric field at the cathode surface, the tips are sharpened by thermal oxidation [14], i.e. by repeatedly growing and removing (wet etching) a thermal oxide at temperatures not exceeding 1000 °C. Since tip radii after DRIE are already <30 nm, wet oxidation of ~700Å is sufficient to achieve atomically sharp tips. Due to the stress-dependent nature of oxidation, tip depth is relatively unaffected.

Additionally, since oxidation consumes silicon, the oxidation sharpening cycle can be exploited to separate the aforementioned self-aligned tip geometries. This is similar to the methodology in [9]. The nanowires in Fig. 3 become symmetrically sharpened tips on the cathode and anode in Fig. 4. Not only does this result in electrode distances closer than those possible through lithographic definition and etch aspect ratio alone, but sharpened tips on both ends of the gap effectively double the electric field. In terms of (3), this doubles parameter β for the same tip sharpness resulting in a fourfold increase in current.

Devices fabricated via above methodology were characterized in a vacuum probing station with an HP4145 IV curve tracer. Results of a typical device from a 22 μm SOI wafer are shown in Fig. 5. The diode shows hundreds of microamps of current at relatively low voltages. To our knowledge, this is the highest achieved current from a single silicon FED. The data was fit to (1) extracting $a=4.76 \cdot 10^{-6}$ and $b=247$.

C. Reducing distance by VHARM methodology

The above methodology does not provide a means of reducing electrode separation below 0.5 μm . Further reduction of the cathode-anode gap is possible using the VHARM methodology [15] by depositing polysilicon over the sharpened and aligned tips. Deposition thickness can be accurately controlled to nanometer distances allowing for gap distances that greatly surpass lithographic and etching limits. Following DRIE, approximately 3000 Å of doped n-type polysilicon is deposited in an LPCVD furnace. Oxidation sharpens the tips and a blanket RIE etch removes the oxide and polysilicon from the top and bottom of the electrode structures. A typical result of VHARM is shown in Fig. 6. While the tips are extremely close, there is a tip radius penalty associated with the polysilicon deposition. Additionally, there is less tip uniformity following the deposition and further sharpening. Tip radius was further decreased with the same sharpening cycle as detailed previously (Sec. IIB).

Figure 4. SEM images of an LFED after DRIE etching and oxidation sharpening, showing multiple tips along the vertical edge. The main image at 2,500 x, and the inset at 15,000x magnification.

Figure 5. Measured current-voltage characteristics of a typical diode. Cathode-anode separation of 2.2 μm separation was measured on a SEM.

Figure 6. Electrode tips following VHARM processing and one oxidation sharpening step. While tip radius is decreased, distance between the top tips is reduced to less than 50nm.

Large vertical non-uniformity is apparent with tips of differing depth (Fig. 7).

Emission has been observed following VHARM and repeated oxidation sharpening similar to the results in previous methodology. In one device, current of 618 μA was observed at

Figure 7. Multiple oxidation sharpening cycles restore some sharpness to the tips following VHARM.

50 V, and after FN fitting, parameters $a=1.41 \cdot 10^{-5}$ and $b=210$ were extracted. That device was fabricated on a $22 \mu\text{m}$ SOI wafer using the standard density recipe (~ 45 tips.)

Assuming a current of $1 \mu\text{A}/\text{tip}$ for reliable device operation, and using the estimated tip density from Sec. IIIA, we estimate a total of $150 \text{ A}/\text{cm}^2$.

D. Submicron self-alignment of electrodes by oxidation spacing

Minor advantages and a large increase in non-uniformity in resulting devices render the VHARM methodology inadequate for our goals. Another approach was taken utilizing micromachining technology to preserve sharpness while maintaining a constant inter-electrode distance through the vertical length of the device. Moreover, this new approach offers arbitrary cathode-anode spacing. Namely, after DRIE and the oxidation sharpening cycle of the SOI wafer, an additional low-temperature oxide layer is deposited to define the inter-electrode spacing without removal of the thermal oxide. This is followed by an n-type doped polysilicon deposition which covers the top, the sidewalls and trenches surrounding the devices. Subsequent chemical mechanical polishing removes the polysilicon from the top of the devices to expose the underlying single crystal silicon (SCS) blocks. Over-polishing through the polysilicon, oxide and first micron of SCS can be exploited to remove the upper tips of the device which are often inconsistent. An HF removal of the sidewall oxide between the sharpened SCS tips and the polysilicon walls completes this method of fabrication. Typical resulting devices of this process are shown in Figs. 8 and 9, where cathode-anode spacing was set to $4000 \text{ \AA}$ and $8000 \text{ \AA}$, respectively.

This single-mask three-dimensional fabrication methodology allows for arbitrary cathode-anode spacing with the polysilicon walls acting as the anode and SCS block as the cathode. Maintaining cathode tip sharpness while reducing electrode distance results in decreased turn-on voltages. One measured device (Fig. 8b) with $8000 \text{ \AA}$ distance resulted in turn-on voltage of $\sim 22 \text{ V}$. Furthermore, the cathode-anode distance is now constant over the height of the device at exactly the oxide spacing that should result in all tips having a similar turn-on voltage.

Appropriately choosing the geometry of a self-separating SCS diode yields a triode in this process with the polysilicon walls acting as the gate. Application of potential to the polysilicon modulates the cathode-anode current. Furthermore, a sufficiently high potential can be used to extract electrons from the cathode in an electron source configuration. With the cathode grounded, different extraction potentials are controlled

Figure 8. Diode with $4000 \text{ \AA}$ spacing between SCS cathode and poly anode (a) footing is apparent at the base of the structure, and (b) a similar device with $8000 \text{ \AA}$ spacing has a turn-on voltage of 22 V .

Figure 9. An SCS diode can operate as either a triode or an electron source using the polysilicon walls as gates.

Figure 10. Triode operating in electron source mode – increased gate potential extracts more current from the cathode to the anode.

by the gate voltage as illustrated in Fig. 10.

Another attempt at controlling emission current, as in classical vacuum triodes, is with silicon microgrids fabricated in the same process. Grids are designed in layout as very thin and modulated photoresist patterns, such that the vertical scalloping effect is sufficient to periodically etch through the structure and create airgaps. The horizontal width modulation in layout results in the microgrid structure shown in Fig. 11. This same phenomenon can be observed in Fig. 3.

IV. MICROELECTROMECHANICAL FEDs (MEMFEDs)

MacDonald *et al* [17] have demonstrated utility of integration of cold cathodes with MEMS actuators. In their work, and that of Kenney *et al* [16], numerous advantages of

Figure 11. Multi-tip cathode and anode pictured with a microgrid in between to modulate emission current.

Figure 12. Microelectromechanical field emission diode with multiple columns of submicron spaced tips. The cathode-anode separation of $\sim 3 \mu\text{m}$ can be adjusted with the comb-drive down to $< 0.5 \mu\text{m}$.

sensors based on tunneling are discussed. Due to the lateral structure of our proposed devices, and high achievable currents, these FEDs lend themselves to numerous related applications. They are easily integrated with electrostatic actuators and fabricated in the same DRIE/oxidation process on SOI wafers. While the work is in initial stages, the result will be a variety of tunable diodes, triodes, and other vacuum devices. The example in Fig. 12 is a diode with ~ 600 atomically sharp tips with electrostatically adjustable cathode-anode distance. Preliminary results in Fig. 13 show an increase of diode current in this device with the application of actuation voltage to the comb-drive structure, which brings the cathode to a submicron distance from the anode. One goal of this research is a fully tunable RF-capable triode in which either placement of both gate electrodes (as shown in Fig. 14) or of all electrodes is adjustable electrically. Gap distances are varied electrostatically either with comb-drives or gap-closing actuators. In combination with methodology for arbitrary cathode-anode spacing discussed in Sec. IIID, effort is under way to develop highly sensitive and reliable accelerometers as in Fig. 15.

V. BATCH TRANSFER OF DEVICES

Fabrication of vacuum microelectronics is typically incompatible with other processes, e.g. CMOS, due to high-temperature oxidation sharpening. For most applications that may utilize the proposed MEMFED methodology it would be

Figure 13. Measured current-voltage characteristics of an electrostatically tunable field emission diode.

Figure 14. Triode with gate actuation in two dimensions using gap-closing actuators. The gates are controlled independently in both x and y to $< 0.5 \mu\text{m}$ relative to the fixed anode and cathode.

Figure 15. Accelerometer device with acceleration sensed by differential current change with gap distances.

advantageous to have the capability of integration with CMOS drive/sense circuits via batch transfer of the former from separate wafers. We utilized the methodology of Maharbiz et al [12] on a variety of devices such as diodes, triodes, and electron sources.

The devices were fabricated in the following four-mask process: starting with a 100 mm silicon wafer (*donor wafer*), $1.8 \mu\text{m}$ of low-stress nitride is deposited and patterned as the structural material over $2 \mu\text{m}$ of sacrificial oxide. This structural pattern was used to etch the sacrificial oxide as well to expose the wafer surface outside of device areas. Next, $4 \mu\text{m}$ of doped polysilicon was deposited. This polysilicon material was

Figure 16. Poly triode fabricated for batch transfer to other substrates: (a) on donor substrate, released with gold staples holding it in place, and (b) after transfer to quartz target substrate, upside down; electrodes still visible through the nitride.

Figure 17. Transferred polysilicon diode performance.

subsequently patterned and etched (DRIE) with a "FED" mask to achieve diodes and triodes over the structural nitride islands.

After cycles of oxidation sharpening, as described in Sec. IIIB, the thermal oxide on top surfaces was removed in a blanket etch. At this point the device fabrication is complete and bumps are added for release and bonding. A 150 Å/600 Å Cr/Au layer is evaporated as a seed layer; 6-8 μm gold bumps are then electroplated in a resist mold. The donor wafers are then diced. After resist-stripping, the structures on donor wafers are then released in concentrated HF for ~4 minutes. The released structures remain on the individual chips due to the small gold bump *staples* [12], which were plated over the structures and surrounding silicon as shown in Fig. 16a. At that point, the devices are batch-transferred using a flip-chip bonder after careful alignment of *donor* and *target* chips, as illustrated in Fig. 16b. Target quartz wafer for the demonstration was plated with gold and patterned with pads in areas where FEDs would be transferred to. Although the process is designed for wafer-level transfers, at this time only chip-level transfers were considered and implemented. The target and donor substrates are aligned and pressure is applied to form a gold-gold compression bond; the donor substrate is then removed, leaving the switches in place over the pads. We verified that the devices continue to operate, as shown on a measured transferred diode in Fig. 17. This emission curve is similar to those found on pre-transfer polysilicon diodes. Diodes fabricated in polysilicon are significantly less consistent in emission characteristics and tip shape than those fabricated in SCS suggesting that batch transfer methods should be explored for the latter material.

VI. CONCLUSIONS

The use of the scalloping formed in DRIE for sharp emission tips has been reported, resulting in achievable tip density of over $150 \cdot 10^6$ tips/cm², and current of over 150 A/cm². By utilizing sacrificial sidewall spacing, electrodes were placed at 4000Å. We further utilized MEMS actuators to laterally adjust electrode distances. To improve integration capability of the FEDs, we demonstrated batch bump-transfer integration of working FEDs onto a quartz target substrate.

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