SPUTTERED SILICON FOR INTEGRATED MEMS APPLICATIONS

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ABSTRACT

This paper describes a new fabrication process for creating electrostatic microstructures that are compatible with prefabricated aluminum-metallized CMOS circuitry. The process uses sputtered silicon to make released microstructures similar to those commonly made using LPCVD polysilicon but does so at much lower temperatures ($\sim 350^\circ\text{C}$). The low-temperature nature of sputter deposition makes it possible to use polyimide sacrificial layers that can be released in an oxygen plasma. This dry-release process eliminates the need for critical point drying or similar methods. Average strain gradients in released sputtered silicon cantilevers were found to vary with the inverse square of thickness. At a thickness of $5.0\ \mu\text{m}$, the radius of curvature of released cantilevers was in excess of $80\ \text{mm}$. Improvements in the electrical conductivity of completed structures were realized by cladding the sputtered silicon structural layers in symmetric, $50\ \text{nm}$ thick layers of titanium-tungsten. Underlying CMOS transistors showed no more than a 3% increase in their maximum saturation current after mechanical layer processing. As a demonstration of the integratability of the sputtered silicon process, electrostatically actuated variable-capacitors were fabricated above CMOS capacitance detection circuitry.

INTRODUCTION

Integration is vital to the performance of many types of microsensors, since as dimensions decrease, sensitivity often falls off precipitously. The sensitivity of a torsional capacitive accelerometer, for example, scales as the fifth power of the lateral dimension. Large arrays of transducers also benefit from integration since the number of bondpads and the external circuitry needed to control each device can be reduced through the use of on-chip multiplexers.

LPCVD polysilicon has been the material of choice for most surface micromachined structures since the early 1980's [1] and has been integrated with on-chip circuitry for nearly as long [2]. Unfortunately, the high deposition and annealing temperatures of LPCVD polysilicon (~ 580 - 630°C and $>900^\circ\text{C}$, respectively), have required either depositing metal layers after the polysilicon structural layers have been deposited in etched pits [3] or using refractory metals such as tungsten instead of aluminum for the circuits [4]. Both approaches increase the overall fabrication complexity and may require re-engineering the CMOS process to accommodate the new thermal budget, metal layers, and/or lithography changes.

In contrast, sputtered silicon can be used to fabricate released microstructures atop standard, aluminum-metallized CMOS at temperatures below 350°C . By avoiding the temperature extremes of LPCVD polysilicon, greater flexibility is allowed in creating or selecting a circuit process, resulting in potentially significant cost-savings and performance advantages.

Most LPCVD polysilicon processes have used oxide sacrificial layers and wet-releases based hydrofluoric acid (HF). Previous high temperature work on sputtered silicon microstructures [5] and our own low-temperature process [6] have followed in a similar vein. Figure 1 shows a sputtered silicon comb fabricated using an oxide sacrificial layer.

Figure 1: A comb structure fabricated in sputtered silicon atop silicon dioxide. The wafer was cleaved beneath the structure after it was released in buffered HF.

Investigating oxide sacrificial layers has led to an interesting discovery. HF porosity in sputtered silicon is evident at thicknesses far in excess of those reported for LPCVD polysilicon [7], making it a potential encapsulating material as well as a structural material. Figure 2 shows a buried cavity formed in an SiO_2 sacrificial layer underneath a $2.0\ \mu\text{m}$ sputtered silicon layer.

One issue of concern is that the attack of the sputtered silicon during exposure to HF may weaken the film structurally. This is in addition to the problems associated with protecting the underlying CMOS during the release and capillary forces that can cause the structure to stick to the substrate if critical point drying [8] or self-assembling monolayers (SAMS) [9] are not used.

However, because sputtered films avoid the temperature excursions of LPCVD polysilicon, they are not only compatible with conventional oxide sacrificial layers, but also with organic sacrificial layers, such as polyimide. These organic layers can be removed in an oxygen plasma, thus avoiding the stiction and selectivity problems associated with wet releases and alleviating the concerns over chemical attack in HF.

Figure 2: SEM image of a cleaved cavity formed in SiO₂ by selectively masking the top sputtered silicon layer with resist and exposing it to 20:1 buffered HF for approximately 1 hour.

DRY-RELEASED FABRICATION SEQUENCE

The basic process flow is illustrated in Figure 3 and begins with completed and tested CMOS circuitry. For convenience, the second metal layer of the underlying CMOS was used as the lower electrode layer for the mechanical structures. This electrode layer consisted of a bi-layer of 400 nm of aluminum and 100 nm of titanium. The titanium capping layer serves to minimize hillocking during the sacrificial polyimide cure cycle.

After patterning the lower electrode layer (Figure 3-a) and opening contact holes in the titanium over the bondpads, an adhesion promoter (*Dupont PIQ-13 coupler, Wilmington, DE*) was spun on and cured at 350°C for 30 minutes. Dupont PIQ-L100 polyimide resin was chosen for the sacrificial layer because of its low thermal expansion coefficient (3ppm/K) and clean release characteristics. This is in contrast to some other polyimides which, as a result of incorporating adhesion promoters within the resin, often leave behind a visible residue when etched in oxygen plasma. The PIQ-L100 resin was spun on for 30 s at 2200 rpm and cured at 350 °C for 1 hr. These spin parameters produced a polyimide film that was approximately 2.5 μm thick. Thicknesses were established using an optical measurement system (*Nanometrics, Sunnyvale, CA*) which was calibrated relative to the results from a profilometer (*Veeco, Plainview, NY*).

The polyimide was then etched back to 2.0 μm in oxygen plasma and coated with 200 nm of aluminum, which served as a hard mask. Etching back the polyimide both improved the adhesion of the aluminum mask and provided more precise control of the sacrificial layer thickness.

After patterning the aluminum mask (Figure 3-b), contact vias were etched in the polyimide using an oxygen plasma. The

anisotropy of this etch was increased by reducing the pressure to the minimum practical limit of the plasma etcher (in this case, 100 mTorr). The photoresist used to pattern the aluminum mask was intentionally left in place to provide a more uniform loading during the etch. Care must be taken to avoid overetching the polyimide at this step, since once the resist and the polyimide in bottom of the vias is cleared away, the lateral etch rate increases significantly due to changes in loading.

Figure 3: Dry release process flow incorporating conductive TiW cladding: Lower metallization (a); Polyimide sacrificial layer and patterned aluminum hardmask (b); Etched polyimide layer (c); Structural layer (TiW, Si, TiW tri-layer shown) (d); Oxygen plasma release (e).

During the course of the sacrificial via etch, the photoresist mask was etched away, leaving the aluminum mask exposed to the oxygen plasma. The oxidized aluminum mask was then removed by immersing the wafers in 50:1 HF for 10 s followed by a wet aluminum etch (Figure 3-c). This HF dip also helped remove any oxidized titanium from the bottom of the vias.

In order to improve the electrical contacts, the wafers were back sputtered in an argon plasma immediately prior to depositing the structural layer. This structural layer consisted of either 0.6 – 5.0 μm of boron-doped sputtered silicon or a tri-layer of 50 nm of TiW, followed by 2.0 μm of doped sputtered silicon and a second, symmetric, layer of TiW. By making the TiW layers symmetric, thermal bi-morph effects were minimized. Stresses in the films were controlled by varying the power and working gas pressure of the deposition. Films with stress values lower than 100 MPa were routinely obtained.

The TiW layers decrease the electrical resistivity of the resultant film significantly, as can be seen from Table 1.

TABLE 1: Comparison of electrical resistivity

Technology	Resistivity
Unannealed sputtered Si	6-50 x 10 ⁶ Ω/□
Annealed sputtered Si	7-50 x 10 ⁹ Ω/□
Sputtered TiW-Si-TiW	25 Ω/□

The wafers were annealed at 300 °C for 1 hr in a dry nitrogen ambient to sinter the contacts between the mechanical layer and the lower electrode and to stabilize the stresses in the structural layers.

The structural layers were patterned using an SF₆-C₂ClF₅ plasma (Figure 3-d). This chemistry etches both TiW and silicon

so there is no need for separate plasma steps when etching the tri-layer.

Following this etch, the wafers were diced and the individual chips were release in an oxygen plasma. The release etch took approximately 4 hrs to undercut $15\text{ }\mu\text{m}$ at an input power level of 200W and a pressure of 3 Torr (Figure 3-e). Release times could be decreased by using a more aggressive plasma etcher, but circuit damage may become a concern.

STRAIN GRADIENTS

Control of warping in released structures is a major concern during microstructure fabrication. This warping is caused by the presence of residual strain gradients throughout the thickness of the structural layer. The sputtered silicon in this work was not completely free of these strain gradients, as evidenced by the curvature of the released cantilevers in Figure 4. However, the gradients were observed to be a strong function of film thickness, with thicker films having smaller average values for the gradient. At a $5.0\text{ }\mu\text{m}$ film thickness, the average radius of curvature of a cantilever beam was in excess of 80 mm.

Figure 4: Dry-released pure sputtered silicon cantilever beams. The top set of beams is $0.6\text{ }\mu\text{m}$ thick. The center set is $2.0\text{ }\mu\text{m}$ thick. The bottom set is $5.0\text{ }\mu\text{m}$ thick and has the least curvature. All beams were released in a 1.3 W/cm^2 oxygen plasma.

Figure 5 shows data from interferometer scans of six cantilever arrays which appears to match a theoretical curve based on surface strains as the dominant contributor to the gradient. The moment caused by these proposed surface strains is proportional the thickness of the film and acts against the

stiffness of the cantilevers which is proportional to the cube of thickness. The radius of curvature is thus proportional to the inverse square of the thickness in this model.

Figure 5: Sputtered silicon stress gradient as a function of thickness for dry-released cantilever beams. Each data point represents typical beams from six arrays. Error bars represent two standard deviations. The solid line represents a theoretical curve based on surface effects, which are postulated to dominate the stress gradients in the films.

The TiW layers used to increase the conductivity of the sputtered silicon can also be used to adjust the curvature of the released structures. By adjusting the stress in the top layer to be more compressive, the released structures can be made more convex. Similarly, by making the stress more tensile, the structures can be made more concave.

CMOS COMPATIBILITY

As expected, the post-CMOS fabrication steps have little measurable effect on the underlying CMOS circuitry. Figure 6 shows transistor curves from transistors fabricated at the Stanford University Center for Integrated Systems before and after the mechanical layer processing. Out of the 30 NMOS and PMOS transistors measured, none showed more than a 3% change in maximum saturation current.

Figure 6: NMOS transistor curves before and after mechanical layer processing. Not more than a 3% increase in maximum saturation current was observed in any of the 30 nmos or pmos transistors tested.

Some of this change can be attributed to sintering of the contacts during the curing and annealing steps since no barrier layers were used between the silicon and the Al-1%Si metallization layers.

INTEGRATED VARIABLE CAPACITOR

As a demonstration of the process, TiW-clad sputtered silicon was used to create variable capacitors with integrated capacitance detection circuitry. This type of device was chosen because most integrated surface micromachined sensors operate using some variation on capacitance detection. Figure 7 shows an optical scan of one such device, an array of $100\ \mu\text{m}$ plates, each suspended by four springs. A simple buffer circuit, with a reset switch to control charging, was used to measure changes in capacitance caused by electrostatically deflecting one set of capacitors. For small deflections, the relationship between deflection, capacitance change, and the output voltage should be linear.

Figure 7: Variable capacitors with integrated detection circuitry. (a) An optical image of the two reference and two variable capacitors next to the capacitance detection circuit. (b) Schematic representation of the capacitance detection scheme.

Figure 8: Deflection as a function of voltage for a $100\ \mu\text{m}$ square variable capacitor. The solid line shows the output of on-chip capacitance detection circuitry. The discrete points show the deflection as measured by six scans of an interferometric microscope. Error bars represent the standard deviation.

Figure 8 shows a graph of the amplified output of the capacitance detection circuit and the deflection of the plates, as simultaneously measured by an interferometer. The measured deflection and circuit output correspond to each other, indicating that the circuit is transducing as expected.

CONCLUSIONS

Sputtered silicon is a promising material for integrated microstructures. When clad in TiW, the resistivity is only $25\ \Omega/\square$. The radius of curvature of released structures depends on the film thickness and can be made lower by using thicker films or by tailoring the stress in the TiW cladding layers. Curvature radii in excess of $80\ \text{mm}$ were demonstrated with $5.0\ \mu\text{m}$ thick samples. The process does not adversely affect threshold voltage or saturation currents of underlying CMOS transistors. Because the sacrificial layer is removed in an oxygen plasma, there are none of the stiction problems associated with wet-releases. Finally, the TiW-clad sputtered silicon process can be used to make many of the same types of devices currently made using LPCVD polysilicon.

ACKNOWLEDGEMENTS

The authors would like to thank Chris Storment and Elaheh Sigari for their assistance during fabrication. Funding for this work was provided by the DARPA Composite CAD Program (Contract #F30602-96-2-0308-P0001).

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