Side-wall Feature Definition For Through-wafer Interconnects Using 45° Mirror Surfaces

Chang Liu†, Mark A. Shannon† and Ilesanmi Adesida

Microelectronics Laboratory, 208 N. Wright Street

†Mechanical and Industrial Engineering Department, 1206 W. Green Street

University of Illinois at Urbana-Champaign, Urbana, IL 61801

ABSTRACT

A novel scheme of patterning vertical chip surfaces using a 45° mirror structure has been explored. We demonstrate, for the first time, straight line paths on the vertical edges of diced wafer chips to achieve front-to-back electrical interconnection; these present significant advantages in packaging MEMS systems. Photoresist is electroplated uniformly on all surfaces (including sidewalls); it is then exposed with collimated UV-light beam reflected off a 45° mirror surface placed near the side walls. The minimum line-width resolution is limited by shadow-mask diffraction and mirror-surface scattering; currently the line width loss is on the order of 25 μm with a 320-nm UV light source.

INTRODUCTION

Traditionally, microelectronics chips are packaged in an enclosed environment and bonding wires are used to connect bonding pads to pins on a package. Many MEMS sensors and actuators are, however, directly exposed to the physical environment and the traditional IC packaging scheme will present problems. In many MEMS applications (e.g. fluid mechanics and bio-medicine), exposed bonding wires can have serious disadvantages: bonding wires can disturb the physical environment and are subjected to physical damages. For instance, a shear-stress sensor based on thermal-transfer principles [1] must be placed flush with the wind-tunnel surface; any surface protrusions (such as bonding wirings) will be highly undesirable.

As one alternative, wafer through-hole interconnects have been demonstrated [2-4]. These are fabricated using an-isotropic silicon etching to obtain through-wafer holes bound by {111} surfaces. There are two major disadvantages. First, the hole opening on the backside of the silicon wafer is typically several hundred micrometers wide; it consumes large space, renders the wafer fragile and generally prohibits further processing. Secondly, the through-wafer hole typically takes approximately 10 hours to complete using wet etchant; the time consumption will not allow the wide use of such a technique for today's large-sized ($\geq 6\text{in}$ diameter, and therefore thick ($\geq 500\text{ }\mu\text{m}$ in thickness) silicon wafers.

We propose a novel scheme for achieve front-back interconnection - by patterning metal leads on the vertical edges of the diced silicon chips. With this new technology, interconnects take little space and can be made in a much shorter time. Density of interconnects can be

potentially higher than previously mentioned methods.

In high-density packaging where chips will be in contact with each other, interconnect paths can be recessed to prevent electrical shorting; recess structures can also be achieved with this patterning technology. This new exposing scheme can potentially be applied to pattern sidewalls *within* a wafer and create three-dimensional MEMS structures to achieve added processing flexibility and device functionality.

SCHEMATIC

The schematic of the exposure setup is shown in Fig. 1. A *mirror chip* with a 45° mirror surface is placed next to a *device chip* to be patterned. Incoming collimated UV light beam (inside a contact aligner system) is reflected off the 45° mirror surface and directed toward the photoresist material on the sidewall of the device chip. Due to the light beam diffraction and mirror-surface scattering, it is advantageous to place the two chips as close as possible in order to achieve optimum resolution. In industrial applications, a pre-manufactured frame with four mirror surfaces facing inward can be placed outside of a device chip and expose all four edge surfaces and the front surface simultaneously.

Fig. 1 Schematic diagram of exposing side-wall photoresist with a 45-degree mirror surface.

SAMPLE FABRICATION

A silicon device chip (500 μm in thickness) with smooth edge surfaces is used. These vertical surfaces can be created using proper wafer dicing techniques. The metal layer is either evaporated aluminum or electro-less deposited Ni or Cr (Transene Co.) In the first case, Al is evaporated separately on the front/back surfaces and side-walls. The chip is then placed in a photoresist electroplating bath (positive working PEPR 2400 from Shipley Co.) to grow approximately 2 μm of resist; it is then baked at 120 °C using a convection

oven. A special chip holder is used to avoid damages to the photoresist surfaces. The device chip and the mirror chip are placed immediately adjacent to each other on a vacuum chuck in a Karl-Suss contact aligner; the exposure is done under hard-contact mode.

MIRROR FABRICATION

A first 45° mirror is made from a blue tempered spring steel (SAE-1095) and the mirror surface is produced by conventional machining and finally mirror-polished using buffing wheels. Figure. 2 is an SEM micrograph of the finished mirror surface. The arithmetic mean roughness (Ra) over a 80 μm scan distance is measured to be 20-40 nm. Close SEM examination reviews micro-scale voids on the surface. We concluded this mirror surface is not adequate; in the future, polished optic glass can be used to improve this technique.

Fig. 2 SEM micrograph of the conventionally machined mirror surface.

Micro mirrors with atomic smoothness can be formed using an-isotropic etching [5, 6] of semiconductor substrates. Using silicon substrate, for example, the best optical quality is obtained by etching a silicon wafer unconventionally cut with a 9.7° offset to the <100> crystal orientation [6]. Unfortunately, wafers of this particular specification are not readily available. To demonstrate the principle of side-wall patterning, we used EDP etched {111} surfaces from <100> oriented, 500 μm -thick wafers. The mirror surface is therefore 54.7° from the base plane and offset the deflected beam from the horizontal position; it is subsequently used to expose wafers that are no more than 400 μm thick. The mirror surface roughness is 1-2 nm, significantly better than that of the conventional machined surface. To increase the surface reflectivity, high reflective metal (Al or Ag) can be evaporated in the future.

PATTERNING EXPERIMENTS

The minimum line width is determined by two factors: diffraction associated with shadow-mask proximity printing and light scattering at the mirror surface.

The minimum line width determined by diffraction (l_d) is

$$l_d \cong \sqrt{\lambda t}$$

where λ is the wavelength of the exposure radiation and t is the distance of the gap. Besides, l_d will not change with the vertical height because the optical path length is constant. In our experiments, $\lambda = 320\text{nm}$ and $t \approx 500\mu\text{m}$, therefore the diffraction-limited minimum

line width is 12.6 μm . Mirror surface scattering contributes to expose intended masked region and causes a line-width loss. The exact amount will be linearly dependant on the horizontal distance from the mirror surface to the device chip edge. Detailed analysis will be presented elsewhere; detailed process can also be experimentally characterized [7].

Straight vertical interconnect paths, 50 μm in width, are shown in Fig. 3. The original line width on the mask is 100 μm ; light beam expansion therefore accounts for 25 μm of line-width loss on each side. This is confirmed because original 50- μm wide lines disappeared near top surface of the device chip. Currently, we are improving on the optical exposure technology in order to obtain higher resolution, developing theories and design/fabrication guidelines.

Fig. 3 Optical micrograph of interconnect paths on the sidewall of a 400 μm -thick silicon chip.

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