ANISOTROPIC SINGLE CRYSTAL SILICON ETCHING IN HIGH DENSITY RFIC PLASMA WITH HIGH ASPECT RATIO AND HIGH SELECTIVITY

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ABSTRACT

A high density Radio Frequency Inductively Coupled (RFIC) plasma etcher has been used to etch single crystal silicon with high aspect ratio and high selectivity. Silicon etching with fluorine based simple chemistry and controlled temperature of the wafer has been investigated on etch rate, trench profiles and selectivity. The trade-off of each process parameter to end result is a well-known phenomenon in the etch technology. Silicon etch rates up to 8 microns/min have been achieved with good results and extremely high selectivities to thermal oxide that range from 200 -1000. High aspect ratios, greater than 30:1, have also been achieved with very vertical profiles. This type of process performance has been offered for both new and existing applications, such as (microelectro-mechanical systems) MEMS devices, high-voltage isolation devices and semiconductor IC's. This paper reviews some of the plasma etching fundamentals and some of the complexities associated with RFIC etching.

INTRODUCTION

Silicon trench etching plays an important role in a wide range of applications in IC and MEMS device fabrication. A quick review of traditional semiconductor IC silicon etching requirements compared to MEMS etching requirements reveals the need to expanding into a truly three dimensional etching technology for MEMS devices. These three dimensional requirements in a MEMS device increase the importance of understanding and optimizing the trade-offs typically seen between each etch process parameter.

Current IC Approach	MEMS Approach
Surface etching	Bulk etching
Feature size < 1 μ	Feature size 1 μ - > 100 μ
Etch deep < 10 μ	Etch deep 10 μ - 600 μ or through wafer
Etch on single wafer	Etch on single and bonded wafers
Etch on one side	Etch on single and both wafer sides.
Etch rate < 1 μ /min	Etch rate > 2 μ /min
Oxide selectivity > 20:1	Oxide selectivity 100:1
Aspect ratio < 10:1	Aspect ratio > 10:1
Toxic and corrosive gases (Chlorine and Bromine chemistries)	Non toxic and non corrosive gases (Fluorine Chemistries)
Require special facility installation, such as scrubber, gas cabinet and pumping system	Less requirement on facility installation

EXPERIMENTAL

The wafers used for this work are silicon substrate, P type, {100} orientation, pre-patterned with a variety of materials by a wafer supplier. The wafers' sizes range from 100 mm to 150 mm. An Alcatel 602E system is used for this investigation. A member of the Alcatel 600 modular family of vacuum systems, the major components of the Alcatel 602E include a process chamber, load lock, transfer chamber, pumping system and electrical and computer control units. The system features a vacuum cassette load lock with robotic transfer of wafers between the cassette and the single wafer process chamber. Plasma etching of the wafers is performed on a temperature controlled pedestal, which can be varied from -120 C to +20 C. The plasma source uses a patented RFIC source design that generates a high density plasma (up to 10¹² ions/cm³ in argon) at a low pressure of about 10 mTorr. Substrate bias is separately applied with another RF power supply at 13.56 MHz. Fluorine based chemistries are controlled by mass-flow controllers. A variable conductance gate valve controls the process pressure. A set of permanent magnets in the process chamber walls magnetically confine the plasma. Process parameters were varied as follows: pressure range from 10 to 30 mTorr, plasma source power from 500 to 1400 watts, gas flow rate up to 200 sccm, pedestal temperature range from -120 to +20 C and substrate bias from -20 to -80 volts. Mask materials used were thermal oxide, CVD oxide, low temperature oxide, silicon nitride and photoresist. The mask openings were etched by dry etching and the feature sizes ranged from sub-micron to a few hundred microns. The etch depths and profiles were determined by an Hitachi SEM and a Dektak profilometer.

RESULTS AND DISCUSSION

To etch silicon, SF₆ was used because of its ability to ionize easily under an RF discharge, giving a lot of radicals F*, which are the main silicon etching species [1]. The anisotropic etching mechanism has been extensively studied and discussed. The etching chemistries based on fluorine and O₂ addition produce a passivation layer on the sidewalls of the feature during the etching [2]. This thin oxide passivation layer protects the sidewalls from attack of the fluorine neutrals. As such, a truly vertical anisotropic silicon etch can be successfully achieved. In the case of fluorocarbon chemistries used, a polymerized fluorocarbon layer deposits efficiently under low temperature and the polymer passivates the sidewall, controlling lateral silicon etching[3]. Both techniques have been proven to be very effective for control of sidewall erosion during etching. It is important to understand the benefits and drawbacks of each of these two techniques in order to be able to optimize the etching parameters, thereby achieving the optimum process performance for any given application.

Surface charging can indeed develop due to an imbalance of electrons and ions. Negative profiles have been observed when silicon etching in high density plasma [4]. Obviously, increasing the sidewall passivation while increasing the ion energy should reduce the deflection and yield a more vertical profile.

An effect of substrate bias on mask selectivity has also been investigated. Thermal oxide is one of the best mask materials to be used for very deep silicon trench etching. It provides an extremely high selectivity that ranges from 200 to 1000. It is a good candidate for these MEMS applications because of its properties and the well-known technology for oxidation, patterning and mask opening. Higher substrate bias will reduce the mask selectivity, as shown in Fig. 1.

Fig. 1. An effect of substrate bias on selectivity to oxide

Different mask materials have been also investigated. The selectivity of silicon to these materials has been established as seen in the table below.

Mask Materials	Mask Selectivity to Silicon
Thermal oxide	200 - 1000
CVD oxide	20 - 50
Low temperature oxide	30 - 100
Silicon plasma nitride	20 - 50
Photoresist	30 - 100

The types of mask patterns and exposed areas play an important role in what type of process conditions are required for specific mask patterns. These etch characteristics are optimized through the combination of hardware configuration and process parameter adjustments. These allow the desired good results of anisotropic profiles, high etch rates and high selectivity to the mask to be achieved.

Various trenches and pillar structures have been studied to produce high aspect ratio, vertical profiles. Fig. 2(a) shows a SEM micrograph of sub-micron pillar features ($0.6\mu\text{m}$) with an aspect ratio greater than 30:1. Fig. 2(b) shows $1.5\mu\text{m}$ pillars at $54\mu\text{m}$ depth with truly vertical profile and smooth sidewalls. Finally, plasma source power is one of the dominant process parameters in terms of etch rate, as can be seen in Fig. 3.

CONCLUSION

High etch rates with high quality, high aspect ratio features have been achieved by using Alcatel 602E system. With this technology, very deep structures with high aspect ratios and very small feature sizes can be applied to new applications for both the MEMS and the semiconductor industries. A high mask selectivity allows the etching of a very deep silicon trench with a minimum

mask thickness. The control of process parameters with optimal hardware is essential to produce the best quality etch result.

Fig. 2. (a) a SEM micrograph of $22\mu\text{m}$ depth submicron pillars with $>30:1$ aspect ratio.

Fig. 2. (b) a SEM micrograph of $54\mu\text{m}$ depth of $1.5\mu\text{m}$ pillars.

Fig. 3. Effect of source power on etch rate

REFERENCES

- [1] E. Cabruja, Sensors and Actuators A, 37-38 (1993) 766.
- [2] H.H. Wang, Plasma etching of poly Si in SF_6 - O_2 mixtures, Proc. Int. IEEE V-MIC Conf., June 25-26 1985, pp 335-341.
- [3] Shinichi Tachi, J. Vac. Sci. Technol. A9 (3), 1991.
- [4] S. Murakawa, Appl. Phys. Lett. 64, 1558 (1994).