A Micromachined Silicon Condenser Microphone With On-Chip Amplifier

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ABSTRACT

Monolithic silicon microphones have been fabricated which include on-chip JFET buffer amplifiers, providing a complete microphone plus electronics on a single silicon chip. Test data is presented showing sensitivities as high as 40 mV/Pa (-48 dB ref. 1V/ μ Bar), with routine sensitivity of 15 mV/Pa (-57 dB ref. 1V/ μ Bar) and bandwidth of 70 Hz to 20 kHz. Noise measurements show that electronics noise from the gate bias resistor is dominant, leading to $1/f^2$ noise spectral density.

The fabrication of these microphones uses both surface and bulk micromachining (Fig. 1). Surface micromachining (precision electroforming) is used to make the perforated bridge electrodes, while bulk micromachining is used to form the diaphragm and through-hole. Diaphragms of P⁺ doped silicon from 1 to 2 mm in diameter have been tested. A monolithic ion implanted JFET and polysilicon resistors are fabricated on-chip.

An analysis of the theoretical attainable sensitivity of a micromachined condenser microphone will be presented. A theoretical Figure of Merit proportional to the microphone signal to noise ratio is derived, which allows the microphone design to be optimized.

INTRODUCTION

Today's microphones are of four types: dynamic, condenser, condenser - electret, and piezoelectric. Most previous micromachined microphone work [1-14] has focused on condenser microphones because of their high sensitivity, simplicity, potential for miniaturization, and compatibility with thin film fabrication techniques.

Condenser microphones use a thin membrane as one plate of a variable capacitor, and can achieve sensitivities as high as 100 mV/Pa with a 25 mm diameter diaphragm. A bias voltage is applied to the sense capacitor, which produces an output voltage when attached to a high input impedance buffer amplifier.

Condenser-electret microphones use an electret material in the sense gap to produce the bias electric field, hence no polarizing voltage is required. Electrets render the bias voltage unnecessary, but it is not clear if the electret process is compatible with on-chip IC processing. Electrets are a major advantage in low cost battery powered systems where providing the bias voltage (5 to 20 volts) is an undesirable cost.

The work reported here concerns the fabrication of silicon condenser microphones and their optimization using a monolithic JFET source follower amplifier.

Fig. 1. Cross section of monolithic microphone with on-chip JFET and poly-resistor.

THEORY

The theory of condenser microphones is well developed in the literature [15]. What follows is a procedure for optimizing the design given system constraints such as bias voltage, buffer input capacitance, maximum SPL and package volume.

The diaphragms used in this work are sufficiently complicated that they can only be analyzed by finite element analysis. However, the theoretical analysis of the microphone is best carried out using a simple spring-mass-damper model in which the diaphragm is assumed to move as a rigid piston. The equivalent compliance C_{SP} (m^3/Pa) of a real diaphragm can be calculated (using FEA) as the volume displacement divided by the static pressure.

The acoustic compliance C_{SP} is given in terms of an average spring constant k_{SP} (N/m) as:

$$C_{SP} = \frac{A^2}{k_{SP}} \quad (1)$$

The compliance of the package interior is given in terms of the internal volume V_{CAV} , atmospheric pressure P_0 and the ratio of specific heats γ :

$$C_{CAV} = \frac{V_{CAV}}{\gamma \cdot P_0} \quad (2)$$

The series compliance of the diaphragm and cavity is

$$\frac{1}{C_{SER}} = \frac{1}{C_{CAV}} + \frac{1}{C_{SP}} \quad (3)$$

The gap capacitance is $C_{gap} = \frac{\epsilon_0 A}{x_0}$. The total inductance

L_{TOT} (kg/m^4) is given by the sum of the diaphragm plus radiation inductance:

$$L_{TOT} = \frac{\rho_{Si} \cdot t}{A} + \frac{1.7 \cdot \rho_{air}}{\sqrt{\pi} \cdot A} \quad (4)$$

where $\rho_{Si} \cdot t$ is the mass/area of the diaphragm. The fundamental resonant frequency is given by

$$v_0 = \frac{1}{2\pi \sqrt{L_{TOT} \cdot C_{SER}}} \quad (5)$$

The collapse voltage of the capacitor is given by

$$V_C^2 = \frac{8 \cdot x_0^3 \cdot A}{27 \cdot \epsilon_0 \cdot C_{SP}} \quad (6)$$

The sensitivity M (V/Pa) of a condenser microphone is given by [15, 16]

$$M = \left(\frac{8 \cdot V_{Bias} \cdot x_0^2}{27 \cdot \epsilon_0 \cdot V_C^2} \right) \cdot \left(1 + \frac{C_{SP}}{C_{CAV}} \right)^{-1} \cdot \left(1 + \frac{C_L}{C_{Gap}} \right)^{-1} \quad (7)$$

where C_L is the load capacitance including both stray and buffer amplifier input capacitance. The advantages of writing the sensitivity in this form are that the dependence on cavity volume and load capacitance is very clear. If the package is made too small, or the load capacitance is made too large, the signal is reduced.

Eq. 6 can be used to eliminate C_{SP} in favor of the collapse voltage, which is a typical product specification. This allows the sensitivity to be plotted as a function of area A and zero bias gap x_0 , with bias voltage, collapse voltage, cavity volume, and load capacitance as parameters. The number of parameters can be further reduced by taking V_{bias} as a fixed fraction of V_C , e.g., $V_{BIAS} = 0.6 \cdot V_C$.

Fig. 2 shows a plot of sensitivity vs. area and gap, using a collapse voltage of 2 volts and a bias voltage of 1.2 volts, a cavity volume of 15 mm^3 , and a load capacitance of 0.6 pF. Such small bias voltages are interesting because of the possibility of using these microphones in small battery powered applications such as hearing aids. The maximum sensitivity is 32 mV/Pa, which is quite respectable for a hearing aid microphone.

Fig. 2. Sensitivity (mV/Pa) vs. diaphragm area and sense gap for a condenser microphone with $V_{Bias} = 1.2 \text{ V}$ and package volume = 15 mm^3 .

Fig. 3 shows sensitivity vs. area and gap using a package volume of 40 mm^3 , a collapse voltage of 8.3 volts and a bias voltage = 5 volts, all other parameters the same as Fig. 2. The peak sensitivity is 56 mV/Pa. This is much higher than available in current commercial electret microphones with wide bandwidth (20 kHz).

The noise of a condenser microphone with source follower buffer amplifier is usually dominated by resistor and JFET noise. Gate leakage current at the JFET and other current leakage terms lead to white current noise which can be lumped in with the gate resistor noise term. With careful design, the Brownian motion limit (due to air-damping of the diaphragm) can be achieved for higher frequencies.

The voltage noise V_n^2 (V^2/Hz) from the JFET and gate resistor is [10]

$$V_n^2 = \left(\frac{C_{Gap} + C_L}{C_{Gap}} \right)^2 \cdot \left(\frac{K}{f} + \frac{8kT}{3 \cdot g_m} \right) + \frac{4kT}{R_g \cdot (\omega \cdot C_{Gap})^2} \quad (8)$$

Fig. 3. Sensitivity (mV/Pa) for microphone with bias voltage of 5 V, package volume = 40 mm^3 .

where $\omega = 2\pi f$, g_m is the JFET transconductance, k is Boltzman's constant, C_L is the buffer plus stray capacitance and K is the flicker noise coefficient of the JFET.

From Eqn. 8, we see that the resistor noise term (which is usually dominant) is inversely proportional to the microphone capacitance, hence the S/N ratio of the microphone is proportional to the product of sensitivity and output capacitance. The charge figure of merit $FOM_Q = M \cdot C_{GAP}$ is therefore the quantity to maximize if maximum S/N is the goal. Given an input sound pressure P_{in} and considering only the gate resistor noise, we have

$$\frac{S}{N} = \frac{P_{in} \cdot M \cdot C_{Gap} \cdot \sqrt{R_g}}{\omega \sqrt{4kT}} \quad \text{is in numerator?} \quad (9)$$

Fig. 4 shows FOM_Q for the 5 volt bias case. The optimum design for S/N is shifted towards larger capacitance, resulting in an optimum at $x_0 = 4 \mu\text{m}$ and $A = 4 \text{ mm}^2$, whereas the sensitivity is maximized at $x_0 = 9 \mu\text{m}$ and $A = 0.8 \text{ mm}^2$. The sensitivity at optimum S/N drops roughly in half to 25 mV/Pa, but the S/N is increased by a factor of 5.5 compared to the sensitivity maximum. If a post amplifier with noise level lower than the source follower is available, then the overall S/N of the system can be improved significantly by choosing the optimum FOM_Q design.

The microphone must operate at a maximum pressure P_{max} without collapsing or excess distortion. If we assume that the gap changes 10% at the maximum pressure, we can derive a very simple and useful equation bounding the performance of the microphone:

$$P_{MAX} = \frac{A \cdot x_0}{10 \cdot C_{SER}} \quad (10)$$

$$M \leq \frac{V_{Bias}}{10 \cdot P_{MAX}} \quad (11)$$

Therefore once the bias voltage and maximum SPL are given, the maximum sensitivity is determined.

Fig. 4. Charge Figure of Merit (FOM_Q , 10^{-13} C/Pa) for microphone. Parameters same as Fig. 3.

EXPERIMENTAL DETAILS

Fabrication

Fabrication started with 3" n-type silicon wafers. A thermal field oxide 700 nm thick was used to mask a P⁺ solid source boron diffusion used for the acoustic membranes. The same diffusion was used for the source and drain of the JFETs.

Polysilicon 0.5 μ m thick was deposited for both doped and undoped poly-resistors. These were implanted with phosphorus through a photoresist mask and then dry patterned by RIE using SF₆.

Channel and gate of the P-channel JFETs were formed by ion implantation of boron and arsenic, respectively. After an implant activation anneal, metal 1 (TiW/Au) was deposited and patterned using liftoff photolithography.

Electroplated gold bridge electrodes were formed using standard thick photoresist processing [13, 17]. A seed layer of Ti/Au was sputtered on a temporary photoresist spacer layer. The plating mold resist (25 μ m thick) was spun on top of the plating seed layer, and patterned. Gold was electroplated into the mold to a thickness of 20 microns. The plating mold, seed layer, and spacer layer were then stripped in acetone, gold etch, Ti etch, and positive resist stripper respectively.

The final fabrication step is a six-hour anisotropic etch in EDP (Ethylene-Diamine, Pyrocatechol, and water), which creates the through-wafer holes and frees up the diaphragm. V-grooves are formed which allow the chips to be snapped apart without dicing.

Test Procedures

The microphone sense capacitors were characterized by an I-V (snap-down) test and by capacitance-voltage curves, using an EG&G PAR 410 C-V meter controlled by an HP 4145A semiconductor parameter analyzer. The snap-down voltage was measured using 40 M Ω series resistors to avoid harming the electrodes.

JFETs were characterized using the HP 4145A to determine SPICE parameters such as LAMBDA, R_{OUT} and I_{DSS}. A program was written to plot both $\sqrt{I_D}$ and I_G vs. V_G , with V_D held at -9 volts. The intercept of the $\sqrt{I_D}$ vs. V_G curve with zero current was used to determine the pinchoff voltage. Gate leakage current is measured at the same time. DC-coupled gain of the source followers was measured from gate to source as 0.91

to 0.94. Using a series 5 pF capacitor, the AC coupled gain was measured as 0.84 to 0.86. This allows a computation of the effective input capacitance of the active source follower as 0.5 pF.

Microphones were packaged in custom small kovar packages with holes drilled for acoustic inlets. Wirebonding was used to attach the JFET to the four external leads. The acoustic inlets were covered with small circles of clean room paper to prevent dust from entering.

An acoustic test station was used to calibrate sensitivity. Two 9-cm thick layers of Sonex (Illbruck, Inc.) acoustic foam line a (60 cm)³ wood box containing a small headphone speaker, reference microphone and DUT. Miniature optical rail was used to hold the speaker and a black thread cross-hair used as a position reference to repeatedly locate the microphones. Microphones were suspended by their cables from the top of the test chamber.

The speaker is driven by the output of an HP 3562A Dynamic Signal Analyzer. A B&K 4135 condenser microphone and type 2804 pre-amp were used as a reference microphone with sensitivity of 3.2 mV/Pa. The DUT and reference microphone were positioned adjacent to each other and 13 cm from the speaker. Simultaneous measurement did not introduce any errors below 20 kHz, compared to measuring each microphone alone and forming the ratio of the responses.

TEST RESULTS

JFET's

The ion implanted JFET test results are summarized in Table 1. Leakage current on some wafers averaged 0.25 pA, while on other wafers was as high as 30 - 40 pA. The variation in leakage current is probably due to heavy metal decoration of dislocations resulting from the boron diffusion.

Low noise JFET's are typically formed in epitaxial silicon with no implants, however, good low leakage JFET's can be formed by ion implantation [18-20]. An implanted channel and gate were chosen for this process to avoid an epi step and enable tight control over threshold voltage. Pinchoff voltage is chosen at 1 V to allow FET operation with a single dry cell, although a larger bias voltage (5-10 V) is typically required to obtain good sensitivity.

Table 1: JFET Parameters

Parameter	Typical Value
W/L	576 μ m/3 μ m
Gate resistance	12 G Ω
Source resistance	50 k Ω
V _{PO}	1.0 V
I _{DSS}	680 μ A
Early Voltage	20 V
Effective Input Capacitance	0.5 pF
DC coupled gain	0.91 - 0.94

Figure 5 shows a microphone chip with a 1.8 mm diaphragm and radial support springs. Several alternative JFET buffer amplifiers are located on the device edges. Fig. 6 is a close-up of a microphone with a 1 mm diaphragm, showing the bridge electrode and an oval-shaped JFET.

Fig. 5. Microphone with 1.8 mm Diaphragm on a 3 mm chip, showing perforated, electroplated bridge electrode and various designs of buffer amplifiers at periphery.

Fig. 6. Microphone with 1 mm diaphragm, showing close-up of oval JFET and perforated bridge electrode.

Sensitivity vs. bias voltage is shown in Fig. 7 for the 1.8 mm diameter radial spring design. This data was taken using hybrid JFET chips sawn from JFET process development wafers.

The frequency responses of 1.0 mm and 1.8 mm diameter diaphragm microphones is shown in Fig. 8a and b. The fundamental resonance of each is at 15 kHz, and sensitivity is 16 mV/Pa mid-band.

Environmental testing was performed on prototype microphones by several outside laboratories. The microphones survived both "cap-gun" and "balloon-burst" stress testing. Microphones were exposed to 95% R.H. at 60°C for 2 weeks, with no change in sensitivity. Total Harmonic Distortion was less than 0.5% at 1 kHz and 100 dB SPL. These microphones and pre-amps had no protective passivation layers, hence units with passivation layers are expected to better withstand environmental stress.

NIST [21] also performed calibration tests on early prototypes, confirming the sensitivity data of Draper's in-house calibration tests. THD was shown to be < 1% at 1 kHz and 114 dB SPL. A-weighted noise of these devices was as low as 25 dB SPL.

Fig. 7. Sensitivity vs. bias voltage for several microphones with 1.8 mm diameter diaphragms and 4 radial springs.

(a) 1 mm Diaphragm

(b) 1.8 mm Diaphragm

Fig. 8. Frequency response of microphones with (a) 1 mm diaphragms, and (b) 1.8 mm diaphragms.

CONCLUSIONS

Monolithic silicon microphones with on-chip JFET source followers have been fabricated and tested. The monolithic buffer amplifier results in the lowest stray capacitance and good control over leakage currents. Future developments may include CMOS circuitry if the trend towards system integration on a chip continues, or a hybrid system may be more economical.

According to theoretical analysis, a bias voltage of 5 to 10 volts is required to achieve high sensitivity, wide dynamic range and high signal to noise ratio. A voltage multiplier circuit will likely be necessary for single cell applications such as in-the-ear hearing aids.

The sensitivity and bandwidth of these microphones can be optimized for any application by changing the diaphragm compliance, area, gap and damping. The bandwidth demonstrated on prototype devices (20 kHz) is wider than standard hearing aid microphones (typically 6 kHz), yet their sensitivity is higher than the low cost electrets. These microphones could find a niche in voice recognition or other

applications where both high fidelity and moderate cost are required.

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