A 4-Channel Multi-Standard Adaptive Serial Transceiver for the Range 1.25–10.3 Gb/s in CMOS 65 nm

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Abstract — The article presents a fully adaptive serial 4-channel transceiver for the standards 10G Base-R, SATA, PCI Express, FC, RapidIO, DisplayPort. The unit is capable of operating in the range 1.25–10.3125 Gb/s with a bit error rate less 10^{-12} . The total jitter of the transmitter output signal $TJ_{TX} < 26$ ps for $BER=10^{-12}$. The receiver tolerance to high-frequency jitter $JTH_{RX} > 0.3$ UI (30 % of the unit interval) with 24 dB channel loss for polynomial PRBS31. The transceiver demonstrates error-free data processing at a speed 10.3125 Gb/s for a channel with a total attenuation of 33 dB. The unit is designed using CMOS 65 nm technology and has power consumption of 760 mW. The features of this transceiver are: 1) the decision feedback equalizer with direct access with reduced power consumption, 2) the adaptive auxiliary clock controller to increase the receiver tolerance, 3) the pseudo-differential cascode output driver, 4) the controller of the minimally admissible differential voltage of the output driver.

Keywords — equalizer, decision-feedback equalizer, receiver, transceiver, DFE, direct-feedback architecture, active inductor, CML, SSLMS, sign-sign least mean square.

I. INTRODUCTION

A wide variety of standards for electrical communications (cable/printed circuit board) leads to an increase in the area, power consumption and number of pins of the integrated circuit. This problem is solved by designing a transceiver that covers as many standards as possible.

The degree of degradation of a transmitted signal in the connecting channel varies significantly depending on a number of physical effects. To ensure correct operation, the transceiver must have a wide tolerance range, adaptively adjusting the system depending on the integrity of the signal.

Section II presents the top-level transceiver architecture. The receiver and transmitter implementations are shown in Sections III and IV, respectively. The measurement results are given in Section V.

II. TRANSCIEVER ARCHITECTURE

The transceiver's architecture implemented in this work is shown in Fig. 1.

Fig. 1. Four-channel transceiver architecture

The transceiver has two phase-locked loops (PLLs), each PLL includes two different LC-based voltage-controlled oscillators (VCOs). Central frequencies of 5.0, 6.3, 8.0, 10.1 GHz and a tuning range of $\pm 12.5\%$ for each VCO cover the frequency range from 4.5 to 11.3 GHz. A CLKI/CLKQ quadrature clock is formed by dividing the PLL output signal by 2 and it comes to the input of each channel. The duty cycle and quadrature of the CLKI/CLKQ degrade in the propagation process. The DQC recovers the clock signal to improve the interpolator's linearity.

The input parallel data bus TIN with N (40/32/20/16/10/8) bits width is serialized into a 2-bit sequence. A bundle of SREG, PRE, DRIV forms a 4-tap feed-forward equalizer (FFE) based on the non-recursive filter with finite impulse response. SREG is a shift register, PRE is a multiplexing matrix that redistributes the

contribution of each tap in the output stream, DRIV is the output driver with the summation operation. SWC adjusts output signal swing. The digital delay lock loop (DLL) synchronizes the internal clock phase with the input signal TCLKIN by controlling the transmitter interpolator PI. An additional duty cycle corrector (DCC) was added to the interpolator output, which eliminates residual effects during a pulse clock signal converting to a rail-to-rail. Programmable output divider DIV by 1, 2 or 4 allows to generate clock signals for data processing in the range of $1.25 \div 10.3125$ Gb/s.

The analog front-end (AFE) of the receiver consists of input network TERM, variable gain amplifier (VGA) and 2-stage continuous time linear equalizer (CTLE). The TERM ensures input impedance matching with the channel and the transmitter, provides a sufficient level of electrostatic protection, applies a fixed de-emphasis at low frequency and shifts common mode level. The VGA provides the optimal swing and the CTLE compensates inter-symbol interference (ISI) in the middle of the frequency spectrum of input signal. Then the signal is fed to 4-tap decision feedback equalizer (DFE) which contains three paths: Boundary, Data and Auxiliary, clocked by CLK_B, CLK_D and CLK_A signals respectively. A DFE is able to compensate for non-linear attenuation of the input signal without increasing noise and crosstalk. The signal is then sampled, de-multiplexed and processed in the low-frequency domain by clock data recovery (CDR) and sign-sign least mean square (SSLMS). The CDR generates the

BCode, DCode, and ACode control codes for three independent interpolators PI, adjusting the frequency and phase of the CLK_B, CLK_D, and CLK_A. The SSLMS generates VGACode, CTLECode, DFECODE control codes to adjust VGA gain, CTLE gain peaking, DFE coefficients, common mode offset.

III. RECEIVER

A. Analog front-end

Fig. 2 shows the AFE, which is tunable digitally. The input port TERM contains T-coil that decreases return loss caused by ESD protection capacitance. Termination R_{term} is automatically calibrated in range $\pm 25\%$ to compensate process-voltage-temperature (PVT) effects. Capacitance C_B allows creating independent common mode for VGA to improve linearity and bandwidth. Target DC value is determined by resistance divider R_A/R_B . TERM attenuates the low-frequency component of the signal by 3.5dB, compensating for the skin-effect seen on printed circuit board (PCB) already at 50MHz. The VGA gain is regulated in range from -4.5 to 7.5dB by resistor R_{VGA} . To prevent influence of parasitic zero in attenuator mode, an adjustable capacitor C_{NVGA} is added to VGA output. The gain peaking of a 2-stage CTLE is varied within 11dB on 5GHz frequency by C_{CTLE} capacitor. DC gain CTLE is fixed about 1dB. This feature allows to decrease VGA gain for channels with high losses or mitigate DFE nonlinearity for channels with low loss.

Fig. 2. AFE schematic and frequency response of TERM, VGA, 2-stage CTLE

B. Decision feedback equalizer

In [1] power-hungry DFE was implemented using current mode logic (CML). The high power consumption was a bit decreased by replacing resistance load with active inductance [2]. In [3], equalizer was fully implemented with precharged logic which drastically decreased power consumption but led to decrease in speed. Moreover, DFE was clocked by complex-shape signal, increasing the consumption of the clock driver.

Fig. 3. DFE implementation

Fig. 3 shows DFE of proposed receiver circuit. The scheme contains two identical parallel pipelines to reduce requirements for bandwidth by two. Even and odd input sequence streams are proceeded by EVEN and ODD pipelines respectively. For DFE to function correctly, it is necessary to ensure timely arrival of data in the feedback loop to the input of the first slices. Total delay time should be within UI for the first tap ($k = 1$) and within $2UI$ for the remaining taps ($k \geq 2$). In proposed DFE, $deven(2n)$ path for capturing the data of the first and higher taps is implemented in parallel. The same for $dodd(2n+1)$. The first tap is implemented using CML with active inductance on load (represented by dashed line in Fig. 3). Sense amplifiers (SA) [4] are used for higher taps to decrease power consumption. The first tap delay:

$$T_{TAP1} = T_{SUM} + T_{BUF} + T_{SETUP_CML} < UI,$$

where T_{SUM} – adder delay, T_{BUF} – buffer delay, T_{SETUP_CML} – CML latch setup time. The second and higher taps delay:

$$T_{TAPK} = T_{SUM} + T_{BUF} + T_{SETUP_SA} + T_{C2Q_SA} < 2UI,$$

where T_{SETUP_SA} – SA setup time, T_{C2Q_SA} – SA delay.

In case when CML latch and SA are clocked by CLKD simultaneously, the time constraint UI would be decreased by value $T_{SETUP_CML} - T_{SETUP_SA}$, because their values are not equal, T_{SETUP_CML} is positive, T_{SETUP_SA} – negative. To compensate for this time difference, the CLKD to the CML latch is delayed relative to the SA.

C. Receiver adaptive algorithms

The algorithms necessary to restore the input signal integrity are based on sign-sign least mean square (SSLMS) method [3]. The threshold level and the DFE taps are adjusted according to the equations:

$$h(n,0) = h(n-1,0) - \mu * \text{sign}[e(n)],$$

$$h(n,k) = h(n-1,k) - \mu * \text{sign}[e(n)] * d(n-k),$$

where k – tap number from 1 to 4, μ – adaptation gain and $\text{sign}[e(n)]$ – prediction error sign.

The common mode offset correction is based on error number comparison of “1” in EVEN pipeline and “0” in ODD pipeline:

$$h_{OFFC}(n) = h_{OFFC}(n-1) - \mu * (-1)^n * \text{sign}[e(n)].$$

The frequency response in Fig. 2 shows that CTLE behaves like an equalizer in the range from 0.6 to 5 GHz. Consequently, to calculate the CTLE gain peaking, it is enough to accumulate eight taps:

$$h_{CTLE}(n) = h_{CTLE}(n-1) - \mu_{CTLE} * \text{sign}[e(n)] * \sum_{k=1}^8 d(n-k),$$

μ_{CTLE} – CTLE adaptation gain.

After adjustment of the DFE taps, the CTLE gain peaking and the offset, a single check of $h(0)$ is performed on the condition:

$$h_{MIN}(0) \leq h(0) \leq h_{MAX}(0).$$

The VGA gain does not change (default value) if the condition is met. Otherwise, the gain changes depending on the current value of $h(0)$ using lookup table. Next, the receiver resets all adaptive settings and recalibrates again with respect to current VGA gain value.

D. Adaptive auxiliary clock controller

Fig. 4 shows an EVEN pipeline diagram after convergence of all receiver algorithms. The data are sampled by three clock signals. CLKD captures $deven(2n)$ in the center, forming the original data transmitted through the channel. CLKB captures $deven(2n)$ at transition

Wrong CLKA position causes error Δe . As a result, ISI of the input signal $z(n)$ seems larger than in reality. The total value of $h(k)$ is slightly more, and the value of $h(0)$ is underestimated. Non-optimal $h(k)$ coefficients lead to poor system performance. Possible causes of the Δe error:

- 1) quadrature of CLKA to CLKB may be violated, for example, due to technological variation,
- 2) correct position of the CLKB phase is also not guaranteed, due to possible asymmetric distribution of deterministic jitter in the input signal [7],
- 3) comparator and buffer delays are not identical.

Auxiliary clock optimal phase searching approach proposed in this work is based on monitoring of threshold value $h(0)$. This approach in essence is a maximum value $h(0)$ searching using forced variation of CLKA phase in range overlapping possible deviation. The maximum value of $h(0)$ means that the error e_0 is minimized and the coefficients $h(k)$ are optimal. To implement this approach, adaptive auxiliary clock controller (AACC) is developed and built in between SSLMS and CDR, as shown in fig.5.

Fig. 5. AACCC interconnection

The CDR in fig. 6 consists of binary phase detector (PD), majority vote (MV), proportional integral filter (PIF), phase shifter SHIFT and decoder TC. The PD generates information about the shift direction of the receiver clocks using Boundary and Data. The MV performs decimation, reducing frequency of data

processing. The PIF accumulates data to control the frequency and phase of clocks in integral and proportional paths, respectively. The integral gain K_I and the proportional gain K_P set the bandwidths in these paths. The TC converts binary code to thermometer code BCode, DCode and ACode, used by interpolators. Kd and Ka are used to set DCode and ACode shift in respect to BCode.

In normal CDR mode, all coefficients are constant. When AACC is active, coefficient K_A is a variable. The controller uses the value of $h(n,0)$ to estimate the direction of the shift CLKA. Tab. 1. shows algorithm of AACC. At each step, a set of three variables is analyzed: the current value $h(n,0)$, previous value $h(n-1,0)$ and the sign of the increment coefficient $\text{sign}[a(n-1)]$ at the previous step. Based on these data, the current sign $\text{sign}[a(n)]$ is formed with increasing or decreasing the coefficient $K_A(n)$. Note that the K_A coefficient changes at every step, even when $h(n,0) = h(n-1,0)$, which allows to stimulate the state machine to search. After a certain time, AACC stops and the K_A value is fixed.

Fig. 6. CDR block diagram

Table 1

AACC algorithm

Comparison	sign[a(n-1)]	Trend	sign[a(n)]
$h(n,0) > h(n-1,0)$	+1	improvement	+1
$h(n,0) > h(n-1,0)$	-1	improvement	-1
$h(n,0) = h(n-1,0)$	+1	without changes	+1
$h(n,0) = h(n-1,0)$	-1	without changes	-1
$h(n,0) < h(n-1,0)$	+1	degradation	-1
$h(n,0) < h(n-1,0)$	-1	degradation	+1

Fig. 7. AACCC block diagram

Fig. 7 shows the implementation of the controller. The comparator compares two seven-bit codes — the current $h(n,0)$ and previous $h(n-1,0)$. A logical zero or one of the increment coefficient $a(n)$ represents its sign, depending on the result at the output of the comparator and the previous $a(n-1)$. The K_{IA} settles AACC bandwidth. Data is

accumulated in a 24-bit signed adder with saturation, where the 7 most significant bits represent $K_A(n)$.

IV. TRANSMITTER

The features of the transmitter implemented in this work are following: the controller of the minimally admissible differential voltage of the output driver [5] and the pseudo-differential cascode output driver (fig. 8). Similar to the receiver input, an adjustable terminator RTERM and a differential T-coil are built into the output. The driver is a current adder of 64 identical parallel-connected cells. The M1/M2 transistors are implemented on thick oxide and form the tail current. The switches M3/M6 are connected to M1/M2 in series. The feature of the driver is the auxiliary current source M7, which controls voltage at the nodes V1 and V2 through the switches M4/M5. This approach has two advantages. Firstly, the data dependent jitter of the output driver is reduced by eliminating residual charge in V1/V2 during the process of leaving the M3/M6 cut-off. Secondly, it allows to avoid possible overloads on M3/M6 drains.

Fig. 8. Pseudo-differential cascode output driver

V. MEASUREMENT RESULTS

The four-channel transceiver is designed and fabricated in 65 nm CMOS technology. The layout is shown in Fig. 9 and it has a size of $2.22 \times 1.3 \text{ mm}^2$. The LCPLL and the transmitter output driver operate at a supply voltage of 2.5 V, the remaining blocks operate at 1 V. The 1890VG19Y integrated circuit, which has 10 four-channel transceivers, was explored.

Receiver sinusoidal jitter tolerance is measured with a J-BERT N4903B from Agilent Technologies. The pseudorandom binary sequence (PRBS) generator produces a data sequence and feeds it to the receiver input, the PRBS checker takes data from the transmitter output and performs error searching, while the transceiver operates in the parallel feedback loop mode. In this mode,

the control codes come to the input of the transmitter interpolator from the receiver's CDR (not from the DLL, as in Fig. 1). Fig. 10 shows the measured characteristic for 10.3125 Gb/s. The PRBS31 polynomial data is fed to the receiver input through a 40 cm long (16 inches) PCB Nelco 4000-6 embedded in J-BERT. The total loss of the channel at the Nyquist frequency is about 24 dB (18.4 dB for PCB Nelco 4000-6 and 5.6 dB for connectors, daughterboard and package). The margin of high frequency jitter tolerance beyond the tracking bandwidth is approximately 0.3UI (30% of the unit interval).

Fig. 11 demonstrates the efficiency of AACC. Measurements were taken from 32 receivers. The result of each sample is presented as statistical distribution of difference in high frequency sinusoidal jitter tolerance with turn on and turn off AACC. Improvements weren't approved in 20 measurement cases. The maximum effect was 0.015 UI. No negative influence of the controller on the receiver tolerance has been registered. The average value for all samples is approximately 0.0026 UI.

The results of complex measurement analysis are shown in fig. 12. It shows the receiver's tolerance margin for high frequency ($> 20 \text{ MHz}$) sinusoidal jitter for four speeds with various PCB Nelco 4000-6 lengths. For example, the margin is 0.36 UI for a 5 Gb/s stream passed through a 110 cm board.

Differential input return losses for the receiver are measured using the Tektronix DSA8300, results are shown in fig. 13. The return loss are below -10 dB for the range from 0 to 6 GHz.

Fig. 14 shows an eye diagram taken from the transmitter output using the Keysight DSAZ254A. Total jitter for 10.3125 Gb/s stream is 26 ps for $\text{BER} = 10^{-12}$, which is less than 27% of the unit interval. Note that in order to compensate the package and the PCB losses the transmitter's equalizer was programmed at 4.1 dB at the Nyquist frequency.

At the final stage of testing two modules were connected by a 50-cm PCB. The total channel loss at 5.15 GHz was about 33 dB (23 dB — the test board in Fig. 15, 10 dB — the other components). The transmitter equalizer is programmed with 4.5 dB post1-tap and 2.7 dB pre-tap. Transceivers demonstrated error-free operation for 72 hours, exchanging data at a speed of 10.3125 Gb/s.

Table 2 shows the main characteristics for this and prior art four-channel transceivers. The presented transceiver is inferior in power efficiency [1], but it has the best FOM taking into account the channel loss at Nyquist frequency.

Fig. 9. Four-channel transceiver layout

Fig. 10. Measured sinusoidal jitter tolerance receiver

Fig. 11. Statistical distribution of difference in high frequency sinusoidal jitter tolerance with turn on and turn off AACC

Fig. 12. High frequency sinusoidal jitter tolerance vs length of Nelco 4000-6

Fig. 13. Receiver's differential input return loss measurement

Fig. 14. Measured eye diagram at 10.3125 Gb/s PRBS7 data

Fig. 15. Measured channel loss for test PCB 50 cm long

Table 2

Comparison with prior art four-channel transceivers

Publication	This work	[1]	[7]	[8]
Technology, nm	65	32	90	90
Data rate, Gb/s	1.2÷10.3	14.025	8	1.25÷10.3
Channel loss at Nyquist, dB	33	22	36.8	41
Area, mm ²	2.89	2.925	2.56	3.04
Supply voltage, V	1.0/2.5	1.0	1.2	1.2/2.5
Power, W	0.76	0.88	0.928	1.264
Power efficiency, mW/Gbps	18.43	15.69	29.0	30.65
FOM, mW/Gbps*dB	0.56	0.72	0.79	0.75

VI. CONCLUSION

A multi-standard fully adaptive serial four-channel transceiver for electrical links was designed. The unit is capable of operating in the range 1.25÷10.3125 Gb/s with channel loss 33 dB and bit error rate less 10^{-12} .

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