Analysis of Power Consumption of Matching Signals Summation Circuits for 65 nm CMOS Content-Addressable Memory Registers

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Abstract — Power consumption of two registers of content addressable memory based on STG DICE memory cells is analyzed. Considered content addressable memory registers have different summation circuits of matching signals – the scheme based on combinational logic and the scheme based on match line. Power consumption of combinational logic circuit depends on number N of inputs of the circuit that change their logical states, because the number of switched logical gates inside the combinational logic circuit depends on the N value. Analysis showed, that the value of power consumption of combinational logic differs from 2 to 104 μW as a function of N value. Power consumption of circuit based on match line does not depends on N value and it practically equals the value of combinational logic power consumption when a half of the inputs switches. So if in the step of content addressable memory development, it is known that input data words differs from each other in average by less than a half of all bits, then combinational logic is preferable to save power in registers. Analysis of topology and simulation results showed, that match line takes 35% less area on the chip and has 22% less output bit of matching delay compared to combinational logic.

Keywords — combinational logic, content addressable memory, design, logical element, power consumption, simulation, topology

I. INTRODUCTION

Content addressable memory (CAM) is used in high-performance data processing systems and in translation lookaside buffers (TLB) of microprocessors. Content addressable memory registers provide bitwise comparison of stored data word with sequence of input data words and consist of elements of matching (CAM cells), elements of masking (mask cells) and summation circuit of matching signals. Content addressable memory devices has great power consumption compared with power consumption of traditional RAM because of simultaneous switching of elements of matching and elements of summation circuits in all registers of memory device. Reducing of power consumption of summation circuits is priority goal of CAM development.

Conventionally, circuits based on match line (ML) are used in CAM registers for summing of matching signals. Outputs of all elements of matching are connected to the match line, and the output signal of matching depends on match line voltage. For today, there are summing circuits

[1], [2] for CAM registers that allow to reduce power consumption by more than 5 times compared to conventional CAM registers. In paper [1] short current pulse precharges the match line and differential amplifier forms the output signal of matching depending on match line voltage. In paper [2] precharge of match line is activated only if the first seven bits in register match, therefore power consumption of precharge circuits decreases. In work [3], there is an analysis of problems of CAM register with match line design. With increasing of number of bits, delays increase and the problem of charge sharing becomes significant. Also, the advantages of summing circuits based on combinational logic compared to conventional match line are justified. In work [4], modified scheme of CAM register with match line is proposed to decrease power consumption and eliminate charge sharing problem.

Conventionally, content-addressable memory devices are based on 6-transistor memory cells. In [5], methods used for design of CMOS 28 nm TLB are described. With technology node decreasing to 65 nm and less, 6-transistor memory cells sensitivity to impact of single nuclear particles have greatly increased. New STG DICE (Spaced Transistor Groups Dual Interlocked Cells) memory cells [6], [7] have high tolerance to effects of single nuclear par-

Fig. 1. Schematic of the element of matching based on STG DICE memory cell and logical gate XOR based on two tri-state inverters TRInv 1 and TRInv 2. This element of matching is a half of the base element “2 CAM cells”

tics impacts and they are promising for using in content-addressable memory registers with increased tolerance to single event effects.

In this work, we analyze the power consumption of CAM registers based on STG DICE memory cells, compare summation circuits for matching signals – circuit based on combinational logic and circuit based on match line.

II. ELEMENTS OF CONTENT-ADDRESSABLE MEMORY REGISTER

Content-addressable memory register includes elements of matching and elements of masking. Fig. 1 presents the schematic of element of matching based on STG DICE memory cell [8]. Logical gate “Exclusive OR” (XOR) based on two tristate inverters TRInv 1 and TRInv 2 provides comparison of stored bit and input bit from Input 1 and Input 2. Output state of the element of matching depends on values of bit stored in STG DICE and input bit.

Transistors of element of matching are separated into two joint groups, so the impact of single nuclear particle with linear energy transfer to its track up to $60 \text{ MeV} \times \text{cm}^2/\text{mg}$ on only one joint group does not lead to the failure of memory cell state. Only short noise pulses on the output of element of matching can occur, which is confirmed by TCAD modeling [9]. On the layout, one joint group of every element of matching is placed between two joint groups of another element of matching. With every joint group sizes of $2.4 \times 2.45 \text{ } \mu\text{m}$ this interleaving provides the distance between mutually sensitive nodes of STG DICE memory cell of more than $4 \text{ } \mu\text{m}$. It practically excludes the possibility of simultaneous impact of single nuclear particle on both joint groups of one element of matching. Two elements of matching with interleaving of their joint groups on the layout form the base element “2 CAM cells”.

Element of masking (mask cell) includes STG DICE memory cell and a decoder for data reading in stable and

Fig. 2. Schematic of element of masking (mask cell) based on STG DICE memory cell and the decoder for reading data in both stable and unstable states of the STG DICE

unstable states of STG DICE that consists of two inverters Inv 1, Inv 2 and two tristate inverters TRInv 1, TRInv 2 [10]. Schematic of the element of masking is presented on fig. 2.

III. SUMMATION OF SIGNALS OF MATCHING IN CONTENT-ADDRESSABLE MEMORY REGISTERS

Summation circuit forms an output signal of matching for the CAM register from signals of matching of all elements of matching in the register. Registers considered in this work consist of 8 mask cells, each of them provides logical masking of signals of matching for two elements depending on data kept in the mask cell.

Register with summation circuit based on combinational logic includes three blocks of matching (BM) and two blocks of matching and masking (BMM) [11]. BM block consists of eight elements of matching (i.e. four base elements “2 CAM cells”) and logical element 8NAND with noise pulse compensation [12]. Fig. 3a presents the functional diagram of BM. BMM block consists of four base elements “2 CAM cells”, four mask elements and combinational logic circuit that provides summation of signals from eight elements of matching taking masking into account. Fig. 3b presents the $\frac{1}{4}$ part of BMM block. Fig. 4 presents the functional diagram of the register with summation circuit based on combinational logic. Logical element 5OR provides summation of blocks BM and BMM outputs and forms the signal of matching result for whole register – Output bit of matching. Thereby, combinational logic summation circuit consists of elements 8NAND in BM blocks, logical elements in BMM blocks and logical element 5OR. This summation circuit represents multiple input combinational logical element NAND with possibility of masking of certain inputs.

In register with the summation circuit based on match line, the “current race scheme” [4] is realized. Diagram of register with match line is presented on fig. 5. Register includes three blocks of matching BM_{ML} and two blocks of matching and masking BMM_{ML} . Fig. 6a and fig. 6b present the schemes of BM_{ML} and BMM_{ML} respectively. Block of

Fig. 3. Functional diagrams of the blocks of the register with summation circuit based on combinational logic: (a) – block of matching (BM); (b) – $\frac{1}{4}$ part of block of matching and masking (BMM)

Fig. 4. Content-addressable memory register with summation circuit based on combinational logic including three blocks of matching BM and two blocks of matching and masking BMM

The diagram illustrates the proposed 1T1C1D1E1S1B1A1 architecture. It features a word line (WL) connected to a series of memory blocks, labeled BM_{ML} and BMM_{ML} . The output of the final memory block is connected to a source follower (SE) and a precharge transistor (Prech). The source follower is connected to the source of the precharge transistor, which is connected to the source of a matching transistor (ML). The output of the matching transistor is the 'Output bit of matching'.

In cycle of data comparison in the register, match line ML already precharged to the supply voltage connects to the ground through the N_{SE} transistor with the high level of SE signal. In case of match of stored in register word and input word from “Input for lookup” bus, all PMOS transistors of blocks BM_{ML} and BMM_{ML} are closed, ML discharges to the ground potential and output comes to logical

IV. ANALYSIS OF POWER CONSUMPTION

In a register with summation circuit based on match line, power is consumed by the elements of matching and by the match line. Power consumption of elements of matching is equal in both registers because the elements are the same in both registers. Power consumption of scheme with match line depends on result of compare operation in register – match or mismatch. In case of match, ML is disconnected from the supply bus and discharges through the N_{SE} transistor. Therefore, the power consumption does not exceed the value of $P_{ML} = V_{DD}^2 \cdot C_{ML} / T_S$, where V_{DD} is the supply voltage, C_{ML} is the value of match line capacity, T_S is the duration of search operation. In case of mismatch, there is a short through current from the supply to the ground through the opened PMOS transistors of summation circuit and N_{SE} transistor. Therefore, power consumption depends on: SE pulse duration that opens N_{SE} transistor, short through current value that depends on parameters of PMOS transistors in summation circuit and the number of opened PMOS transistors. This number equals the number of elements of matching in logical “0” state (mismatch state).

Values of power consumption of registers with combinational logic (CL) and with match line (ML) for different output states of elements of matching, μW

Output state of the element of matching	Elements of matching	CL	ML	Register with CL	Register with ML
All bits mismatch $\rightarrow$ all bits match	268	97	48	360	316
All bits match $\rightarrow$ all bits mismatch	99	104	57	202	155
All bits mismatch $\rightarrow$ 1 bit mismatch	264	75	52	345	316
All bits mismatch $\rightarrow$ 1 bit match	6	3	57	9	63
1 bit match $\rightarrow$ all bits mismatch	3	2	56	5	58

Table 1 presents the values of power consumption of registers with different summing circuits for different output states of elements of matching. For example note “all bits mismatch $\rightarrow$ all bits match” means that all elements of matching initially was in mismatch state and then come to the match state. Simulation results was got with Spectre CADENCE simulator for devices designed with 65 nm CMOS technology. Parameters of simulation: supply voltage is 1 V, clock frequency is 1 GHz, temperature is 25 °C. Power consumption values for elements of matching are equal in both registers (with combinational logic and match line) because the elements are the same in both registers.

Power consumed by the combinational logic circuit depends on number of switched logical gates in the circuit because of changing of their input logical states. For this reason, value of power consumed by the combinational logic depends on sequence of input data words from “Input for lookup” bus. This value varies from 2 to 104 μ W. Minimum value corresponds to the case “1 bit matches $\rightarrow$ all bits mismatch”, when only one input of summation circuit changes its logical state. Maximum value of power consumption corresponds to the case “all bits match $\rightarrow$ all bits mismatch”, when all inputs of summation circuit change their logical states. Power consumed by the scheme with match line depends on number of matched bits in current cycle of comparison and vary from 48 to 57 μ W. Minimum value of power consumption corresponds to the case “all bits mismatch $\rightarrow$ all bits match” when all PMOS transistors of summing circuit are closed and match line discharges to the level of “0”. Maximum value of power consumption corresponds to the case “all bits match $\rightarrow$ all bits mismatch” when all PMOS transistors are opened and short through current from the supply to the ground is maximum. The interval from minimum value to maximum for scheme with match line is 11.3 times less compared to scheme with combinational logic.

Fig. 7. Power consumption P of summing circuits based on combinational logic and based on match line as functions of number N of inputs of summing circuit that change their logical state. Curves “0 $\rightarrow$ 1” corresponds to the switching of N inputs from “0” to “1”, while other inputs remain in “0” state. Curves “1 $\rightarrow$ 0” corresponds to the switching of N inputs from “1” to “0”, while other inputs remain in “1” state

Fig. 7 presents the power consumption P of summing circuits as function of number of inputs N that changed their logical state in current comparison operation. For the circuit based on combinational logic there are two curves. Curves “0 $\rightarrow$ 1” correspond to the switching of N inputs from “0” to “1”, while other inputs remain in “0” state. Curves “1 $\rightarrow$ 0” correspond to the switching of N inputs from “1” to “0”, while other inputs remain in “1” state. In case “1 $\rightarrow$ 0” circuit with combinational logic consumes less power than in case “0 $\rightarrow$ 1”, because in case “1 $\rightarrow$ 0” for any value of N , more logical gates in combinational circuit change their state. For example, if all inputs of NAND element are in logical “1” state than changing the state of only one i -th input to the “0” leads to changing the output state of all circuit. In this case, all logical gates whose state depends on the state of i -th input switch. In case of switching inputs from “0” to “1”, all inputs initially are in logical “0” state and switching one i -th input in “1” state does not change the output state of the circuit. In this case, no one logical gate in whole circuit switch.

As it seen on fig. 7, when switching of more than half of inputs, the value of combinational logic power consumption is greater than match line power consumption. Number of inputs of summation circuit that change their logical states is equal the number of bits of “Input for lookup” bus that change their state. If input words for search in content-addressable memory differs from each other by more than a half of the bits, then register with combinational logic will consume less power than register with match line.

Table 2

Values of the parameters of summation circuits with combinational logic (CL) and with match line (ML)

Parameter	CL	ML
N_{TR}	280	108
$S, \mu m^2$	110	72
$P_{MIN}, \mu W$	2	48
$P_{MAX}, \mu W$	104	57
t_{DEL}, ns	0.23	0.18

Table 2 presents the parameters of summation circuits. Here N_{TR} is a number of transistors in circuit, S is area on a chip, P_{MIN} is the value of minimum power consumption in dependence of input data, P_{MAX} is the value of maximum power consumption in dependence of input data, t_{DEL} is the output signal of matching delay. Interval of values of power consumption for circuit based on match line is 11.3 times less than for circuit based on combinational logic. For circuit based on match line, output delay is 22% less and area on a chip is 35% less than for circuit based on combinational logic.

V. CONCLUSION

Power consumption of content-addressable memory registers with summation circuit based on combinational logic and based on match line are analyzed. Power consumption of circuit based on combinational logic depends

on number N of inputs that change their logical states in current comparison operation. Power consumption of circuit based on match line does not depend on N and practically equals the power consumption of combinational logic while switching a half of inputs. If in the step of content-addressable memory development, it is known that input data words differ from each other in average by less than a half of all bits, then combinational logic allows to save power in registers.

Analysis of topology and simulation results showed that summation circuit based on match line takes 35% less area on a chip and have 22% less output delay compared to summation circuit based on combinational logic.

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