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ADVANCEMENT OF SCHOTTKY BARRIER SOLAR CELLS: A REVIEW

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ABSTRACT

Schottky barrier solar cells are a promising alternative to conventionally fabricated solar cells. Diffusion process used in conventional fabrication is high temperature and sophisticated process with high thermal budget. With the motive to overcome this problem fabrication of Schottky barrier solar cells were initiated with low temperature and less cost back in 1970s. From that time investigation is going on suitable material, optimum structure of Schottky barrier cells. In this paper, different aspect of Schottky barrier solar cells prior to performance enhancement are discussed with significant research outcome from the researchers in chronological order. From the studies it is found that work function difference between base semiconductor and Metal/TCO layer, Interfacial layer thickness are the key parameters of these cells. With advanced technology and materials like BSF, Surface texturing, carrier selective contacts, advanced deposition process etc. cell performance can be enhanced further.

KEYWORDS

Schottky, Barrier, Interfacial layer, MIS, SIS.

1. INTRODUCTION

Generally solar cells have a structure of p-n junction diode when placed in a radiation produces electric power. There are various structures of solar cells based on different texturing, BSF, different materials used but all the structures are based on p-n junction. Solar cell is conventionally fabricated by high temperature diffusion process with process temperature ranges from 800-1100 °C. The base material conductivity type is changed to opposite type with higher degeneracy level. The dead layer formed due to high temperature process reduces the ultra-violet response of the cell. Si is the most common material used as base material for cell fabrication. Due to expensive diffusion process there has been search of alternative processes with lower cost and simplicity. One of such low cost and simple process is to change the conductivity of the surface of the base material by using thin metal layer or comparatively thick transparent conducting oxide layer. Such cell depends on the ultra-thin insulating layer generally of insulating material. The changing of conductivity type can be done by applying suitable metal or semiconductor on the base surface. Suitable materials are determined by work function or electron affinity of the materials. The carrier generation of this kind of cell happens in the bulk region of the base semiconductor and the top metal/ conducting semiconductor with interface serves for photovoltaic collection process.

The above mentioned solar cells are basically Schottky junction solar cell. Actually, the first successful solar cell was fabricated by Charles Fritts in 1883 was a MS (Metal-Semiconductor) structured cell. The cell was fabricated by a coating of selenium over thin gold layer gave efficiency of about 1% (Fritts, 1883). Since that time the research on solar cell didn't get prior attention by the researches. The attention on this type of solar

cell has been started from last few decades. The name, Schottky barrier or junction solar cell came from the name of scientist Walter H. Schottky. He developed Schottky diode with metal-semiconductor junction.

2. CELL MECHANISM

The barrier formed between a semiconductor and a metal layers is predicted by Schottky-Mott rule that is basically proportional to the difference between the metal's work function and semiconductor's electron affinity in vacuum. Often the barrier depends on work function of metal or electron affinity of semiconductor. If the Schottky barrier is quite high and significant fraction of the semiconductor's band gap then the device acts as a minority carrier device and is favorable for solar cell application.

The charge transport in the cell is happened by tunneling through the interfacial layer. The tunneling process is sensible to shape of the barrier at the interface and provides ohmic contact. Thicker interface increases tunneling resistance and decreases the cell performance. The charge transport by tunneling determines the basic I-V characteristics of these cells.

2.1 Structures

Schottky barrier Solar cells generally have three structures given below,

- 1) MS- Metal Semiconductor.
- 2) MIS- Metal Insulator Semiconductor.
- 3) SIS- Semiconductor Insulator Semiconductor.

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In MS structured cell thin metal layer is deposited on base semiconductor material. It is the basic structure of Schottky barrier solar cell. Though it is Metal-Semiconductor structure but a very thin oxide layer of Si is formed in between base semiconductor and top metal layer. Presence of metal top layer reduces number of front contacts but due to high reflectivity of metal proper ARC layer is required.

Due to the mismatch between two different types of material (metal and semiconductor) in MS structured cell, defects are formed in the interfacial layer. Defects are nullified by implementing insulating layer in the interfacial region and cell performance can be enhanced. This structure with presence of insulating layer in the interfacial region is MIS (Metal-Insulator-Semiconductor) structure.

Metals used in MS/MIS cells have low level of transparency and high reflectivity which reduces the light input and as well as power output. To increase the light input thin layer is required whereas thin layer reduces Voc and cell performance. To overcome this issue metal or semiconductor oxide layer with high degeneracy are used with the advantage of high transparency. This structure with degenerative metal or semiconductor oxide layer is called SIS (Semiconductor-Insulator-Semiconductor) structure. The oxide layer acts as semiconductor in this structure. Due to high transparency level of the top layer, requirement of ARC layer is reduced.

Figure 1: a) MS structure b) MIS/SIS structure

2.2 Suitable Materials for top layer

As previously mentioned suitable material for the top layer is decided by the metal or conductive semiconductor's work function and electron affinity. The energy difference between metal or conductive semiconductor layer and interfacial insulating layer (ϕ_{mi} or ϕ_{osi}) controls the degree of inversion of the base semiconductor of the cell. A low value of ϕ_{mi} or ϕ_{osi} is required to invert a p-type base material and high value is required for n-type base. So, for p-type and n-type base materials, low work function and high work function top layer materials are required respectively. When this above mentioned condition is satisfied, the cell will act as a minority carrier MIS/SIS cell otherwise it will work as majority carrier Schottky diode. The following table gives some clear idea about the materials of the top layer.

Table 1: Materials used in top layer		
Type of Material	p-type	n-type
Metal	Al, Cr, Ta, Ti, Mg	Ag, Au, Pt
Oxides	ZnO, ITO	AZO, SnO ₂ , ITO, Graphene

Though these are the possible materials those can be used in MIS/SIS cells but mainly ZnO^[18], AZO (Fuchsel; Jia et al., 2013; Bethge), ITO (Cheek et al., 1978; Ashok et al., 1980; Saha et al., 1983; Saim et al., 1987; Simashkevich et al., 2004; Malik et al., 2008; Bruk et al., 2009; Liu et al., 2010; Du et al., 2015; Du et al., 2017) are used by most of the researchers. Another material which is very popular for n-type base material is Graphene (Li et al., 2010; Feng et al., 2012; Miao et al., 2012; Liu et al., 2015; Song et al., 2015). Graphene is a 2D material made by Carbon. Rapid increase of PCE of Graphene based cells is achieved within very short period of time by the various researchers over the world.

2.3 Effect of Interfacial layer

In Metal-Semiconductor cells direct, contact of two different type of material create defects at the interface and gives lower performance than the expected. Though there is always an insulating layer sandwiched in between the metal and semiconductor to some degree (Fonash et al., 1976). During the deposition of metal layer some oxidation takes place on

the Si surface resulting in SiO_x layer of fewer degrees in the interfacial layer. The defects in the MS cells can be nullified by implementing proper insulating layer in the interfacial region. A properly chosen thin-film insulating or semi-insulating layer can give one or more advantageous effects like Control of carrier transport, shaping of electric field in the device, and introduction of fixed charge. Adding to this, an insulating layer having low thickness can also influence the nucleation and broadening of the metal-electrode film as a result directly influences the light transmission to the semiconductor. SiO₂ is the most used insulating material for this purpose. More materials like SiO, SiNx, MOx, Al₂O₃ etc can be used. Al₂O₃ has the property to introduce fixed charge in the insulating layer resulting in hole selective layer which is beneficial for n-type base material (Smit et al., 2014). Thickness of the interfacial layer has a vital role to play for MIS/SIS cells. The optimum thickness of this layer is 15 Å (Shewchun et al., 1977). If the thickness is lower than the limit it becomes patchy, incomplete and the defects between the two different materials become more prominent which causes lowering of the cell performance. On the other if the thickness is higher than the limit then charge carrier could not pass through the interfacial layer and proper carrier transport does not happen and cell will not work properly.

2.4 Process Description

The process involved in cell fabrication has a vital role on forming proper material properties suitable for MIS/SIS cells. Lowering of Voc is a prominent loss in Schottky solar cells and this due to work function loss. Work function of the top layer used is dependent on the process involved. There are several processes can be used for top layer deposition, which are

- Sputtering
- Spray Pyrolysis
- Spray deposition
- Spin on doping
- Atomic Layer Deposition (ALD)
- Screen Printing
- Electron beam evaporation

Out of these five deposition processes Sputtering is mostly used by the researchers though it has some drawback of reducing cell performance with formation of some defects. ALD has the capability of forming most clean and defect free layer but it is most expensive than the other mentioned processes. Though top metal/TCO layer can be deposited by the remaining three processes but they produce very low quality cells. All the aspects of these different processes are observed from the previous works and discussed in the later section.

2.5 Research works on Schottky Solar cell in Chronological order

Researchers have been investigating MIS/SIS structured cell back from 1970s. Most of the papers from the early days were on validation of the structure, their mechanism and mathematical modeling. The boost on MIS/SIS cell fabrication came later after theoretical validation. Chronological progression of such significant works is discussed in this section.

Anderson et al. was one of the first scientists who developed Schottky barrier solar cell. He developed several cells with Al, Cr or AuCr barrier metals with 0.5-10 Ω-cm p-type Si and got potential efficiency in between 4.8 to 12 % and by evaluating computer study of several cells he concluded that reduction of the thickness of metal layer would be beneficial for cell efficiency (Anderson et al., 1972).

The problem of using metal layer over Si is higher cost and low transmittance of the thin metal layer. Thin metal layers increased the ohmic loss on the contrary if the layer became thick it decreased the light penetration I the cell. So Researchers were thinking of thin metal layer with metal grids. Thin metal layer increases transmission and grid lowers the ohmic loss. To address this issue Green et al. proposed grid like structure for Schottky solar cell above thin metal layer. He proposed two structures one is continuous grid with ARC and another is discontinuous grid with ARC to decrease the ohmic loss. He concluded that the characteristics if these cells are similar to conventional p-n junction cells

and with higher L/B ratio of the grid better result can be obtained.

Anderson et al. also studied the optical property of the metal thin film for the application on Schottky solar cell by varying the material and thickness to get optimum sheet resistance and transmission. He got 9.5% efficiency by depositing 50 Å Cr adjacent to the Si for good adhesive property and high Voc and a 50 Å Cu over layer to produce lower sheet resistance.

Researchers also proposed to use metal oxide layer instead of metal layer. Metal oxide layers have more transmission property than metal layers so it causes greater light penetration and less reflection from the upper surface. Though this metal oxide layers are semiconducting layer but they create Schottky barrier solar cell when deposited over Si and performs like MIS structures and the dark I-V characteristics of the cell attributes by both thermionic and diffusion.

Theoretical analysis of such structure was done by Fonash et al. The author concluded that if the presence of insulator layer results the field shaping and transport control by tunneling, then a non-unity ideality factor would result sensitivity to thickness. Field shaping is a unique advantage as it permits the possibility of minimum band-bending distortion in the semiconductor for a given voltage developed in the device. The following figure represents the band diagram of MIS cell on n-type base.

Figure 2: Schematic energy band diagram of MIS cell on n-type base [5]

Shewchun et al. examined in detail, the tunneling behavior of MIS solar cell of Al-SiO₂-p Si structure and evaluated the key parameters which plays key role in optimizing this structure. Author found that insulator thickness around 15 Å gave the maximum efficiency and Voc changed slowly in linear fashion with the change in insulator thickness. In case of doping density, efficiency reached its peak at $3 \times 10^{23} \text{ m}^{-3}$ and then fell down. Dependence of efficiency on surface charge density and insulator charge were also carried out in this work and optimum result found for surface charge density of $4.7 \times 10^{14} / \text{m}^2 \text{ eV}$ and insulator charge of $1.0 \times 10^{16} / \text{m}^2 [6]$.

Ghosh et al. fabricated SIS structured cell of noticeable efficiency with SnO₂ and Si and obtained maximum efficiency of 8.8% with Isc of 125 mA, Voc of 0.515 V and FF of 55%. He also calculated theoretical limit of efficiency to be 20% and practical limit considering all losses to be 15%. The benefit of using SnO₂ as top layer can be seen in the following figure. Reflection is reduced to 15% which is quite lower than the reflection of polished cell. This in turn reduced the requirement of ARC layer on the top (Ghosh et al., 1978).

Figure 3: Reflection profiles of polished Si wafer and SnO₂/nSi cell

Check et al. fabricated ITO based the SIS structured on polycrystalline Si base for the first time and obtained efficiency of 6.25% with grain size 0.02-0.04 mm² sputtering process. It also revealed that, reduction of output of polycrystalline cells is not directly depends on grain boundaries as their area of impact is low compared to total area. In contrary, a notable reduction in photocurrent and barrier height can be caused by the background defects (Cheek et al., 1978).

Van Halen et al. developed SIS solar cell by depositing of TiOx on self grown SiO₂ layer over p type Si. The steps involved for TiOx based cell were different from the regular steps. In this case metallization was done first and then TiOx layer was deposited by spin on doping. Author had found efficiency of about 8% for TiOx based cell and performance of the cell increased with the increment of light intensity. On the other SiO₂ based cell possessed efficiency above 12% but the process was expensive and complicated than the TiOx based cell fabrication (Van Helen et al., 1978).

Check et al. analyzed the possibility of MIS/SIS cells on polycrystalline base material and concluded that MIS/SIS based polycrystalline cells have better blue response than the diffused cells. In diffusion process high temperature forms dead layer in polycrystalline cells but due to lower process temperature in fabrication of MIS/SIS cells no dead layer is formed and incase of diffused cells, four times higher grain boundary is required than the SIS/MIS cells to obtain same cell efficiency (Cheek, 1979).

Srivastava et al. calculated the performance of Schottky based cells on different parameters like interface layer thickness, doping density of the substrate, surface states and the work function of metal. The author evaluated that the cell efficiency is increasing initially with increment of interfacial layer's thickness, density of surface states and donor density then after some increment it is decreasing. The optimal parameters were found to be thickness in between 2-2.5 Å, optimal density of surface states of $10^{13} \text{ cm}^{-2} \text{ eV}^{-1}$ and donor density of 10^{16} cm^{-3} . For high density of surface states metal work function has negligible effect on efficiency but for low density of surface states efficiency increases with increase in metal work function.

Ashok et al. fabricated SIS based cell by depositing ITO over n-Si with inexpensive spray deposition method. An insulating SiOx is also deposited in between ITO and n-Si which is grown in a dry-oxidation furnace. Maximum cell efficiency of 11.5% is obtained with Voc = 0.52 V, Jsc = 31.5 mA/cm² FF = 0.70 and optimal thickness of insulating layer=15 Å.

Nagatomo et al. studied the SIS structure consisting of SnO₂-SiOx- n Si and evaluated the dependency of the opto-electric characteristics on different parameters. The SnO₂ layer was obtained spraying SnCl₄ and water in vapor phase. The fabricated cell did not exhibit the exact minority carrier diode characteristics due to presence of surface states between Si and SiOx layer which tunnels the majority carrier more than the minority carrier. If insulating layer having low surface state density can be formed then a better minority carrier characteristics could be obtained.

Saha et al. had analyzed the barrier height enhancement of SIS solar cell due to surface states and fixed charges. A comparison study was evaluated by the author with varying parameters of insulator thickness, donor density and density of fixed charge. In a sputtered ITO--SiO₂-p-Si cell it was noted that the lower value of the substrate doping require higher value of density of fixed charge to produce a specified rise of the barrier height. This phenomenon is same for the case of spray deposited cells but for same enhancement of barrier height more density of fixed charge is required in case of spray deposited cells than sputtered cell.

Saim et al. fabricated ITO-p Si cell by thick film technique with screen printing and firing process which is conventionally used for metallization. To obtain good ohmic contact Aluminum paste had been used to the silicon and silver had been used for o contact to the ITO and Al as well. At optimum firing temperature of ITO at 650 °C for 35 min, interfacial oxides (SiO₂) are supposed to develop sandwiched between silicon substrates and ITO layer. The estimated thickness of the oxide layer using Auger techniques was $\approx 60\text{-}100 \text{ Å}$. Typical values of the SIS cells under an illumination of 80 mW/cm² are: Voc = 0.50-0.57 V; Jsc = 0.70-0.75 mA/cm²; FF = 0.41-0.47 and efficiency $\approx 0.19\text{-}0.25\%$. Obtained results were low compared to the result by the other researchers but the method was new.

Table 2: Comparison of parameters of ITO/p-Si cells with different thick film printing techniques

Sl No.	Method	Voc(V)	Jsc(mA/cm ²)	FF	Efficiency(%)
1	Screen-Printing (Unannealed)	0.48	0.50	0.40	0.12
2	Screen-Printing (Annealed)	0.57	0.75	0.47	0.25
3	Sputtering	0.481	32.2	0.745	16.5
4	CVD	0.510	32.0		12

Simashkevich et al. SIS based solar cell with n+ ITO-SiO₂-n Si structure with inexpensive spray pyrolysis method. ITO is deposited with alcoholic solution of SnCl₄ and InCl₃ in different proportions with special developed installations. To obtain the SiO₂ tunneling layer, the wafers were immersed in HNO₃ for 15 seconds. ITO thickness of 350 nm and transparency of 87% is obtained with 90% of InCl₃ and 10% of SnCl₄ solution. SiO₂ thickness in between 30-60 Å is obtained by substrate temperature 450°C, deposition rate 100Å/s, spraying time 45 s. Cells with active area of 8.1cm² and 48.6cm² were fabricated with quantum efficiency reaches 0.97 at λ=550nm and with AM1.5 illumination conditions the efficiency is 9.567% for cells with area of 8.1cm² and 6.979% for cells with area 48.6cm².

Malik et al. developed ITO-SiO_x-n Si SIS solar cell with simple, cheap, low temperature and fast spraying method. This structure is identical to inversion p+-n junction in disparity to the Schottky barrier structures. They have got better result than the previous results at that time with efficiency of 10.8% and 12.2% with AM0 and AM2 illumination respectively. The paper concludes that, substrates having lower resistivity results lowering of conversion efficiency due to the formation of Schottky barriers forming higher dark saturation current than that presented by p+-n structures.

Maifi et al. had investigated a new structure of Schottky solar cell with Metal-Insulator-Semiconductor-Semiconductor (MISS) configuration. The configuration has ZnO/SiO₂/Si/SnO₂ structure. To sustain this structure a settlement between carrier concentration of silicon and tin oxide was done in a way that SnO₂/Si develops an ohmic contact although ZnO/SiO₂/Si a Schottky diode.

Brak et al. realized a new type of bifacial solar cell based on SIS structure. A structure of n+ ITO-SiO₂-n Si(CZ)-n+ was obtained with efficiency of 9.0% (front side illumination) and 3.6% (rear side illumination) while the efficiency of best monofacial cell was 9.6%. Front ITO layer was deposited on CZ n-Si wafer of 350 nm thickness by spray pyrolysis method with different proportions of SnCl₄ and InCl₃. Back side n+ layer was deposited by P diffusion followed by thermal oxidation with temperature of 850°C. Front and back contacts were formed by vacuum evaporation of copper. The parameters of best obtained result cell are, Voc 0.49 V, Jsc 27.48 mA/cm², FF 66.5%, efficiency 9%, Rse 2.79 Ω/cm², Rsh 6×10³ Ω/cm² for front side illumination and Voc 0.4 V, Jsc 13.23 mA/cm², FF 69.3%, efficiency 3.6%, Rse 3.41 Ω/cm², Rsh 1.26×10⁴ Ω/cm² respectively.

Liu et al. developed Schottky photovoltaic device with solution based spin coated intrinsic semiconductor nanocrystals having power conversion efficiency of 0.02%, FF of 0.26, Jsc of 0.148 mA/cm², and Voc of 0.51 V. The fabrication of Si NC Schottky junction devices is done by spin-casting of Si NC thin films onto indium tin oxide (ITO)-coated glass substrates at speed of 700 rpm in a glove box. A 100 nm layer of aluminum was deposited on the top of the film as the electrode with active area of the device 0.046 cm². The schematic diagram of the cell is given in the following figure. The paper concluded that devices show a clear photovoltaic response. The photovoltaic devices had poor performance, probably due to poor absorption of radiation and serious charge carrier recombination.

Figure 4: Schematic diagram of NC based SIS cell developed in

Li et al. developed the first Graphene (Gs) based Schottky solar cell at room temperature. n-Si(100) wafer with SiO₂ layer of 300 nm thickness were designed with photolithography and wet etching of oxides to develop square windows for the expose of n-Si. Front and back contacts were developed by sputtering Au and Ti/Pd/Ag on front and back side respectively. Then Gs sheet was moved on the top of the patterned wafer and dried naturally with the motive to have conformal coating with Au layer and n-Si. Gs acted as semitransparent upper electrode and ARC layer. The cell has achieved efficiency up to 1.5% [21]. The schematic structure of the cell is given in the following figure.

Figure 5: Schematic structure of Gr/Si cell

Due to high sheet resistance, raw single or multi layer Gr/Si cells have poor electrical property with efficiency up to 9%. Doping is used to enhance the efficiency from the raw Gr/Si cells. Feng et al. developed Gr/Si cell with chemical doping by HNO₃. Formation of Gr/Si substrate was moreover same as. Then HNO₃ was used for doping of Graphene by dipping the cell in HNO₃ vapor. The PEDOT-DOT film was formed by spin coating on top of the Graphene film at 4000 rpm for 1 min, and then heated on hot plate at 140 °C for 10 min. The brief advantage of using HNO₃ doping is given in the following table.

Table 3: Results of Gr/Si cell without and with HNO₃ doping

Samples	Voc(mV)	Jsc(mA/cm ²)	FF	Efficiency (%)
Without HNO ₃ doping	464.9	15.19	0.41	2.90
With HNO ₃ doping	495	17.22	0.51	4.35

Fuchsel et al. developed SIS based cell by two different TCO layers with nano-structured surface. ITO and AZO were deposited as TCO material on p type c-Si by dc magnetron sputtering. Nano-structured surface of the cell was obtained by inductively coupled plasma (ICP) etching process. The SiO_x interfacial layer was formed by thermal oxidation during sputtering process. Lower resistive ITO of 50 nm was used in nano-SIS cell. As a result of better light trapping greater Jsc was obtained for nano-SIS cell but due to increased defect density of the structured surface lower Voc was obtained than the normal SIS cell which had resulted almost same efficiency of around 7.7% for both the cells. It concludes that if the defect density can be lowered by some way then higher conversion efficiency can be obtained from nano-SIS cells.

Miao et al. developed Gr/n-Si shottky junction cell with doping of bis(trifluoromethanesulfonyl)- amide[(CF₃SO₂)₂NH)] (TFSA) and enhance the efficiency from 1.9% to 8.6% [24]. Structure of the cell without and with doping is given in the figure below.

Figure 6: a) Basic Gr/Si Cell structure b) With TFSA doping [24]

Table 4: Results of Gr/Si cells without and with TFSA doping.[24]

Samples	Voc(mV)	Jsc(mA/cm ²)	FF	Efficiency (%)
Without TFSA doping	430	14.2	0.32	1.9
With TFSA doping	540	25.3	0.63	8.6

Jia et al. developed nanowire based SIS solar cell with AZO-Al₂O₃-a-Si:H (p⁺ + i)- n Si structure presented in the figure below. Nanowire was developed by etching of AgNO₃/HF solution in ambient temperature on an n-type (100) Si wafer of 675 μ m thickness. Layer of a-Si:H with thickness 45 μ m was deposited over the wafer by PECVD and subsequently a 1.2 nm thick Al₂O₃ layer and 100 nm thick AZO layer was deposited above the a-Si:H layer by atomic layer deposition. A comparison had been made between the cells with and without 1.2 nm thick Al₂O₃ layer. The Al₂O₃ layered cell has better cell performance than the other with Voc 517 mV, Jsc 26.46 mA/cm² and efficiency of 10.04%. Increment of Voc and Jsc was due to increased passivation effect with the presence of Al₂O₃ layer while increased series resistance due to the presence of Al₂O₃ layer resulted lower FF than the cell where this ultra thin layer was absent. The structural details of this cell can be understood by the following figure.

Figure 7: Schematic of the nanowire based SIS cell described in [25]

Betge et al. investigated the performance of the SIS cells using different material as interfacial layer. Thin layer of Al₂O₃, ZrO₂, Y₂O₃ and La₂O₃ are used in between ZnO:Al (AZO) layer and p-type c-Si. The best result had come by using rare earth oxide La₂O₃ with Voc of 527 mV, FF 71.3% and efficiency of 8%. Surprisingly, Al₂O₃ showed drawback in performance. Due to insertion of defective states on band gap of oxide, a chemical instability induced by the diffusion of ZnO:Al layer lowers the effective barrier height. It was also concluded that higher reactivity of AZO caused the higher loss compared to other TCOs.

Liu et al. reported an effective method for the enhancement of Gr/Si cell performance. They have used co-doping by HNO₃ vapor along with Au nanoparticles. Both the doping method resulted in p-type doping and by combined effect graphene with high work function and electrical conductivity has achieved. Mono crystalline (100) wafer was taken and process steps used for pristine Gr/Si cell were taken. Then HNO₃ doping is done followed by Au NP formation over Gr layer [28]. The advantage of using co-doping is illustrated in the following table.

Table 5: Results of Gr/Si cells with different doping

Sample	Voc(mV)	Jsc(mA/cm ²)	FF	Efficiency (%)
Pristine	410	27.4	0.35	3.93
HNO ₃ doping	470	29.3	0.39	5.37
Au NPs doping	460	31.4	0.51	7.36
HNO ₃ + Au NP doping	510	32.8	0.61	10.20

Song et al. developed high efficiency Gr/Si solar cell with doped graphene and additional ARC. The high efficiency was obtained by optimizing the interfacial oxide layer. Optimization of oxide thickness is done by exposing the cell to air for different times before the transfer of graphene to the cell. Recombination current increases with the increase of oxide layer and

results S-shaped I-V curve with low FF. On the other reverse saturation current decreases with increase of oxide layer in between the thickness of 5-15 Å. By which they concluded the optimum thickness as 15 Å. With 15 Å oxide thickness, PCE increased to 12.4% from 10 % with 5 Å and Voc raised to 0.59 V from 0.51 V. Further they have deposited TiO₂ as an additional ARC layer using colloidal solution of nanoparticles by spin coating process resulting in efficiency of 15.6% which is the most efficient Gr/Si cell reported at that time (Song et al., 2015).

Du et al. developed ITO/SiO_x/n-Si SIS cell with different thickness of ITO layer. ITO layer which is a TCO must have optimized thickness. Different structures of the cell are described in the following figure. A thin layer causes reduction of open circuit voltage and a thick layer reduced light penetration through the cell and momentarily reduces short circuit current of the cell. Three different thicknesses of 80 nm, 150 nm and 250 nm had taken and best result came from 150 nm cell with Voc 0.50 mV, Jsc 25.5 mA/cm², FF 72.7 % and efficiency of 9.27 % respectively (Du et al., 2015). The device had no prior reduction in performance with passage of time. Further author have increased the efficiency by using BSF and surface texturing. BSF was implemented by using an n+ layer on the bottom surface of the cell and an increment of around 2%.

Figure 8: Different schemes of SIS cell used in

3. CONCLUSION

Schottky barrier solar cell fabrication is an uncomplicated, less expensive and low temperature process. Choosing proper materials requirement of ARC, heat treatment can be minimized. Due to conductive nature of the top degenerative layer front contacts are minimized resulting in less shadow loss. ITO, ZnO and AZO are promising materials for this purpose. The interfacial layer has the crucial role on cell performance. Width of the interfacial layer must be within 1-2 nm. Most of the Schottky cells are made with SiO_x as interfacial layer but different insulating materials such as Al₂O₃ can be implemented with beneficial outcomes [27]. Adding BSF and surface texturing of different kind more efficient result can be found. In case of Polycrystalline base material this process is effective because less number of dead layers is formed due to of low temperature. Graphene based solar cell is very popular topic on Schottky solar cell from last few years. PCE of Gr/Si cells is improved very rapidly by various researchers throughout the world. But the problem is its size. With the increment of the size, PCE of Gr based cell decreases which is constrain to develop commercial cell. Research is going on to increase the cell size without reducing the PCE.

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