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AN ANALYSIS OF LED DRIVER PERFORMANCE USING TRIAC AND DC LINK DIMMING

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Abstract

The most common dimming control for medium power LED systems is triac dimming, which constitutes the major problem of input current waveform being significantly distorted due to chopping and the resulting system having high total harmonic distortion (THD) values along with low driver efficiencies. The Electromagnetic Compatibility standard EN 61000-3-2-2014 defines THD limits for lighting equipment above 25 W. However, the standard does not specify a limit for systems below 25 W, making triac dimmers appealing for dimming low power LED systems even though the resulting THD, efficiency and power factor values are unsatisfactory. This study aims at evaluating the dimming properties of a flyback LED driver below 25 W, therefore not limited by the EMC standard. For this aim, dimming is separately performed through triac dimming, primary side DC link control with and without power factor correction and the results are analysed.

Keywords: LED Driver Systems, Dimming, Total Harmonic Distortion, Power Factor, Driver Efficiency, Flicker

1 Introduction

A light emitting diode (LED) driver is commonly utilized for receiving and regulating the alternating current (AC) from the electricity grid, rectifying it into direct current (DC) for the operation of LEDs, maintaining power factor correction (PFC) while keeping the total harmonic distortion (THD) as low as possible and finally delivering the DC current to the LED light source (Erdem Atılğan, et al., 2018). Dimming is an important approach for increasing both energy savings and lighting quality and there are numerous methods used to provide LED drivers with dimming capabilities. The most common dimming control for low and medium power LED systems is triac chopping. The biggest problem with triac dimming is that the input current waveform is significantly distorted due to chopping and thus the resulting system has high current THD values along with low driver efficiencies. Especially in high dimming levels, the input current waveform turns almost into alternating impulse waveforms. This situation results in THD values exceeding 100 %.

The Electromagnetic Compatibility (EMC) standard EN 61000-3-2-2014 defines the limits of THD for lighting equipment above 25 W (IEC, 2014). Medium and high power LED drivers must adhere to these limits, making it difficult to use triac dimmers as these dimming systems distort the grid energy quality in important amounts. However, the standard does not specify a limit for systems below 25 W, making triac dimmers appealing for dimming low power LED systems even though the resulting THD, efficiency and power factor (PF) values are unsatisfactory. For power factor values on the other hand, the EU Regulation 1194/2012 sets the following limits for lamps with integrated control gear: no power factor is specified for lamps below 2 W, for power values between 2 W and 5 W, 5 W and 25 W and above 25 W, the power factor values must be greater than 0,4, 0,5 and 0,9, respectively (European Commission, 2012). The regulation does not specify a power factor limit for external control gear.

In this study, a comparative analysis is conducted for three different dimming control methods: AC side triac control, flyback converter primary side DC link control and flyback converter primary side DC link control with PFC. The dimming performances are investigated through measurements of the input power factor, efficiency, current THD and flicker.

2 Method

For the study, a flyback LED driver of 12 W along with an LED luminaire of 12 W were utilized. The system was measured when dimming is separately performed through triac and primary side control with and without PFC. The rated values of the driver are 220-240 V input voltage, 50/60 Hz frequency, 0,2 A input current, 280 mA output current, 36-44 V output voltage, 10-12 W output power and a PF above 0,95. The driver was initially dimmed using a triac dimmer switch. The experiment was then repeated using primary side DC link control with and without PFC. Assuming a linear relationship between drive current and luminous output, the output current was reduced, starting from 100 % down to approximately 10 %. To analyse the dimming performance, input voltage, input current, input power, PF, driver efficiency, output voltage, output current, output power, THD, current ripple, flicker index, percent flicker, flicker frequency and stroboscopic effect visibility measure (SVM) values were measured for all cases.

3 Flyback Driver Topology

In LED driver applications, flyback converters are commonly preferred due to their extensive voltage regulation and isolation features. However, these converters lack some important requirements for LED illumination applications. LED luminaires are sensitive to current ripple which causes flicker. The most important drawback is the relatively low filtering capability of output current due to the lack of an output inductor, i.e. the current filter. Figure 1 shows the general electrical scheme for a flyback driver (Trzynadlowski, 2016).

Figure 1 – General Circuit Scheme for a Flyback Driver

In flyback converters, the primary side of a high frequency transformer is controlled by a switching device, i.e. Metal Oxide Semiconductor Field Effect Transistor (MOSFET) or Insulated Gate Bipolar Transistor (IGBT). The on-state operation of a transistor stores electrical energy as magnetic field energy in the transformer core. While the transistor is off, the previously stored energy is transferred to the secondary side. The voltage conversion ratio of a flyback converter for continuous current mode is given as:

$$\frac{V_o}{V_i} = \frac{N_2}{N_1} \cdot \frac{D}{1-D} \quad (1)$$

Here,

- D is the duty ratio;
- V_o is the output voltage;
- V_i is the input voltage;
- N_1 is the number of turns of the primary winding;
- N_2 is the number of turns of the secondary winding;

The input voltage V_i is approximately equal to the peak value of the AC mains voltage ($V_{\max}$) if a proper capacitor filtering is provided after the input rectifier. But for power factor correction circuits, capacitor filtering is not applied, so V_i simply becomes the absolute value of the AC mains voltage. The output voltage of the driver can be defined as follows:

$$V_o = n \cdot (V_{LED} + R_{LED} \cdot i) \quad (2)$$

Here,

- V_o is the output voltage;
- n is the number of series connected LED chips;
- V_{LED} is the threshold voltage of an individual LED;
- R_{LED} is the resistance of an individual LED;
- i is the output current of the driver.

Due to the relatively higher total threshold voltages of LEDs, dimming is implemented in a narrow output voltage range. The increase in the utilization of LED lighting brings along some important impacts on the AC network. Input power factors of drivers are quite low and terminal current THD is higher due to implementation of rectifiers and triac dimming circuits.

4 Measurements and Results

4.1 Triac Dimming

AC side triac control is the most common dimming method because of its simple application. Placing a triac control circuit between the AC mains and the LED driver is easy and cost-effective. In triac control, the control parameter is the phase delay angle of the triac (α) and this controls the value of RMS input voltage. In triac dimming, a potentiometer positioned on the switch at the input side provides phase control and establishes dimming. In order to analyse the change in the electrical properties of the driver, the output current of the driver has been manipulated using the triac dimmer and measurements have been made, keeping the input voltage 230 V at 50 Hz grid frequency. The resulting measurements are presented in Table 1. Here, and in the following tables, Table 2 and Table 3, I_{in} is the input current of the driver, P_{in} is the input power, or in other words the power consumed by the driver and the LED system, THD_c is the input current total harmonic distortion, $\cos\phi$ is the power factor on the grid side, η is the efficiency of the driver, V_{out} , I_{out} and P_{out} are the output voltage, current and power of the driver respectively, and SVM is the stroboscopic effect visibility measure.

Table 1 – Measurements for Triac Dimming

I_{in} [A]	P_{in} [W]	THD_c [%]	$\cos\phi$	η [%]	V_{out} [V]	I_{out} [A]	P_{out} [W]	Output Current Ripple [A]	Flicker Index	Percent Flicker [%]	SVM
0,062	12,75	34,8	0,896	76,9	0,272	0,272	9,81	0,005	0,04	12,79	0,45
0,067	12,09	69,7	0,783	73,9	0,251	0,251	8,93	0,006	0,04	13,08	0,48
0,073	10,32	116,1	0,617	67,6	0,200	0,200	6,98	0,008	0,04	13,38	0,51
0,074	8,33	154,4	0,491	62,1	0,151	0,151	5,17	0,009	0,04	12,96	0,48
0,071	6,14	196,8	0,376	54,6	0,100	0,100	3,35	0,010	0,04	11,75	0,44
0,056	3,43	233,5	0,266	47,5	0,050	0,050	1,63	0,007	0,03	10,73	0,39
0,043	2,01	265,1	0,203	41,3	0,026	0,026	0,83	0,005	0,03	9,47	0,33

As can be seen from the values given in the table, the electrical properties of input current, input power, output voltage, current and power all decrease in order to decrease the luminous output of the LED system through triac dimming. The main problem here is the alteration in the input current waveform which directly influences the power factor and the current total harmonic distortion of the system. This might also result in current ripple and flicker problems. Figures 2 and 3 show the voltage and current waveforms of the LED system when they're connected to the grid through the triac dimming switch. Figure 2 is when the system is at 100 % dimming while Figure 3 is when the system is at 10 % dimming. As can be seen from Figures, even for

the 100 % dimming situation, the waveform is distorted, losing its sinusoidality, which translates into deteriorations of both power factor and total harmonic distortion.

Figure 2 – Input Voltage and Current Waveforms at 100 % Triac Dimming

Figure 3 – Input Voltage and Current Waveforms at 10 % Triac Dimming

Looking at the values presented in Table 1, the current THDs reach very high values as the dimming level is increased, starting from 34,8 % and finally ending up at 265,1 % for 10 % dimming level. The resulting harmonic distributions for 100 % and 10 % triac dimming is given in Figures 4 and 5 respectively. Even though the European Standard does not define a current THD limit for drivers below 25 W, the resulting current THD imposes a significant problem on the power grid.

Figure 4 – Current Relative Harmonic Distribution at 100 % Triac Dimming

Figure 5 – Current Relative Harmonic Distribution at 10 % Triac Dimming

The values in Table 1 show that while the system power factor at 100 % dimming is equal to 0,896. While the EU regulation 1194/2012 does not set limits for external control gear, as the analysed driver can be easily integrated into an LED system, the values obtained for power factor measurements can be compared to the values specified by the Regulation for lamps with integrated control gear. The input power of the system in hand thus corresponds to a minimum power factor value of 0,5, therefore the measured value of 0,896 is an acceptable value for the EU Regulation (European Commission, 2012). However, the PF drops down to 0,203 at 10 % dimming, a very low value that would pose a threat to grid quality. As expected, the manipulated input waveform due to triac dimming results in the deterioration of both current THD and power factor values, especially in higher dimming levels.

Driver efficiency is a direct manipulator of the energy efficiency when utilizing LED systems. Recent developments in semiconductor technologies have facilitated the design and production of high efficiency LED drivers. The driver used in this study has a measured efficiency value of 76,9 % when connected to the grid through the triac dimmer at 100 % dimming. This efficiency value decreases down to a quite low level of 41,3 % for 10 % dimming, creating another undesirable effect on the overall performance of the LED system.

As the aforementioned electrical properties may also be influencers of the flicker problem in LED systems, flicker measurements have also been carried out in the study. For this aim the

flicker index, percent flicker and the stroboscopic effect visibility measure (SVM) have been recorded for each dimming level using the UPRTek MK350N Handheld Spectrometer. The values in Table 1 show that the flicker index is quite low for all levels of dimming with a maximum value of 0,04 at full load and decreasing only down to 0,03 for 10 % dimming, satisfying the IESNA “good lighting quality” levels (IESNA, 2000). The Percent Flicker and SVM values are also low, showing that with the chosen driver, even with low dimming values, flicker does not constitute a problem. It is important to note that both percent flicker and SVM increase in the first three dimming steps with a maximum flicker percentage of 13,38 % and maximum SVM of 0,51, and then start decreasing again for lower levels of dimming. Nonetheless, all dimming levels provide adequate flicker values according to the three common flicker quantifications.

4.2 DC Link Dimming with PFC

In the second method, the LED current is controlled by adjusting the on and off times of the primary side transistor, i.e. Pulse Width Modulation (PWM) and at the same time, the input current is forced to follow a sinusoidal waveform to adjust the output current for dimming. Here, adding an AC side filter capacitor at the terminal ports makes the input current properly sinusoidal. This effort will expose its positive effect on the input power factor. Table 2 gives the measurement results for DC link dimming with PFC.

Table 2 – Measurements for DC Link Dimming with PFC

I_{in} [A]	P_{in} [W]	THD_C [%]	$\cos \phi$	η [%]	V_{out} [V]	I_{out} [A]	P_{out} [W]	Output Current Ripple [A]	Flicker Index	Percent Flicker [%]	SVM
0,06	12,62	25,9	0,915	79,2	36	0,279	10	0,005	0,04	13,18	0,47
0,059	11,3	20,4	0,939	78,7	35,7	0,250	8,98	0,005	0,04	17,26	0,55
0,056	9,01	12,9	0,965	78,1	35,2	0,201	7,04	0,005	0,05	20,2	0,67
0,049	6,71	12,3	0,970	77,5	34,6	0,151	5,2	0,005	0,06	22,45	0,73
0,04	4,42	12,9	0,972	76,2	33,8	0,100	3,37	0,005	0,06	22,56	0,72
0,028	2,28	16,1	0,970	73,2	32,8	0,051	1,67	0,005	0,05	20,74	0,62
0,02	1,27	21,4	0,960	65,4	32,1	0,026	0,83	0,005	0,04	17,15	0,5

Figures 6 and 7 show the input voltage and current waveforms for DC link dimming with PFC for dimming levels of 100 % and 10 %, respectively. As can be seen from the figures, the sinusoidal form of the current signal does not deteriorate through the dimming process. This result translates into the current THD value to remain almost as high as it was at full load; the current THD value is 25,9 % for 100 % dimming; for the initial dimming steps, this value even drops down to lower values and rises back to 21,4 % for 10 % of dimming. Compared to triac dimming, this result shows that DC link dimming provides a much better alternative in terms of grid quality. The relative current harmonic distributions for 100 % and 10 % dimming levels presented in Figures 8 and 9 are also evidences of this finding.

Figure 6 – Input Voltage and Current Waveforms at 100 % DC Link Dimming with PFC

Figure 7 – Input Voltage and Current Waveforms at 10 % DC Link Dimming with PFC

Figure 8 – Current Relative Harmonic Distribution at 100 % DC Link Dimming with PFC

Figure 9 – Current Relative Harmonic Distribution at 10 % DC Link Dimming with PFC

A similar result is seen in the PF values. As the electrical circuitry of DC link dimming with PFC provides power factor correction, the power factor value remains approximately stable throughout the dimming process. All the power factor values in the table are acceptable for the EU regulation.

Looking at Table 2 for driver efficiency values, it can be seen that the efficiency value drops down from 79,2 % to 65,4 % from 100 % dimming to 10 % dimming levels. This result presents a superiority compared to the efficiency value of 41,3 % obtained at 10 % dimming level with triac dimming.

Similar to triac dimming, the values in Table 2 show that the flicker index is again quite low for all levels of dimming. Here, different than triac dimming, there's a small rise in the flicker index from 0,04 to 0,06 in middle dimming steps but the final value for 10 % dimming level is the same as the initial result of 0,04. The same inclination is seen with percent flicker and SVM values as well; percent flicker increases to a maximum value of 22,56 while the SVM reaches values of 0,73, both metrics staying below unwanted levels in terms of temporal results.

4.3 DC Link Dimming without PFC

In the third method of dimming, similar to the previous method, the LED current is controlled again through PWM but this time without a sinusoidal waveform manipulation. In this case, for the same output performance, the input power factor and current THD are expected to escalate when dimming is performed. The input power factor is expected to decrease due to distortion in the terminal current. Table 3 gives the measurement results for DC Link Dimming without PFC.

Table 3 – Measurements for DC Link Dimming without PFC

I_{in} [A]	P_{in} [W]	THD_c [%]	$\cos \phi$	η [%]	V_{out} [V]	I_{out} [A]	P_{out} [W]	Output Current Ripple [A]	Flicker Index	Percent Flicker [%]	SVM
0,059	12,76	18,0	0,930	79,3	36,1	0,283	10,17	0,005	0,05	16,1	0,58
0,053	11,3	20,8	0,912	77,9	35,7	0,248	8,78	0,005	0,05	14,92	0,57
0,044	9,18	24,7	0,886	75,3	35,2	0,195	6,87	0,005	0,04	13,45	0,51
0,035	6,9	30,9	0,845	75,4	34,6	0,150	5,19	0,005	0,04	12,03	0,44
0,026	4,9	36,9	0,810	68,4	33,8	0,099	3,35	0,005	0,03	12,47	0,40
0,018	2,91	55,0	0,674	56,6	32,8	0,050	1,66	0,005	0,01	4,56	0,16
0,015	2,17	67,1	0,610	36,6	32,0	0,024	0,79	0,005	0,01	4,88	0,12

Figures 10 and 11 show the input voltage and current waveforms for DC link dimming without PFC for dimming levels of 100 % and 10 %, respectively. As can be seen from the figures, the lack of PFC in the circuit results in a moderate deterioration of the sinusoidal form of current, however not as high as the triac dimming situation. Thus the current THD value rises from 18 % up to 67,1 % from 100 % to 10 % dimming levels. The relative current harmonic distributions for 100 % and 10 % dimming levels presented in Figures 12 and 13 also support this finding.

Figure 10 – Input Voltage and Current Waveforms at 100 % DC Link Dimming **Figure 11 – Input Voltage and Current at 10 % DC link dimming** **Figure 12 – Current Relative Harmonic Distribution at 100 % DC Link Dimming without PFC** **Figure 13 – Current Relative Harmonic Distribution at 10 % DC Link Dimming without PFC**

The values in Table 3 show that while the system power factor at 100 % dimming is equal to 0,930, as there's no PFC in the circuit, this value drops down to 0,610 for 10 % dimming. This drop is still providing the grid with a power factor value that is adequate in terms of the EU Regulation, even though there's no power factor correction in the circuit.

Looking at the driver efficiency values, it is possible to see a decrease from 79,3 % to 36,6 %, approximately half of the starting value at 100 % dimming level. This decrease is mainly due to the nature of switching power circuit operation, a lower efficiency whilst dimming is inevitable because of well-known switching losses of conventional power switches such as MOSFETs and IGBTs.

Finally, the temporal results show that the flicker index is again quite low for all levels of dimming. With the third type of control, all flicker metrics slowly decrease and finally make a larger dive at the final two steps of dimming. In general, it can be seen from all the results that flicker has not been a problem for this specific set of driver and LED luminaire with the three different methods of dimming.

5 Conclusion

In this study, three different methods of dimming control have been applied to a 12 W flyback LED driver and luminaire, namely triac dimming, DC link dimming with PFC and DC link dimming without PFC. For all three methods, the best driver efficiencies have been obtained with the primary side DC link control with PFC as expected. Making the input current more sinusoidal decreases the current THD and increases the driver efficiency as a result. But, as experienced with the circuit without PFC, switching power circuit operation results in a lower efficiency whilst dimming due to the switching losses of conventional power switches. The results show that, while AC side triac control is easy to implement, in terms of current THD, PF, and driver efficiency, this type of dimming provides poor results. On the other hand, primary side DC link control with PFC requires an intervention to the primary side transistor control, making the circuitry more difficult, but outperforms the other methods due to its higher power factor and lower THD.

Another finding is that neither triac dimming nor input DC link control dimming has had a significant effect on the regulation of the driver circuit output, i.e. current ripple and flicker. This is prominently due to the size of the output capacitor in the circuitry as well as the low power value of the driver and LED luminaire that has been used in the experiment and should not be an example for higher power LED systems.

Overall, input values such as PF, THD and driver efficiency show very important differences in the three different dimming topologies that have been analysed in this study. It should be noted here that while a single low power driver controlled by triac dimming may not be an important threat to the power system individually, when a substantial number of these drivers are employed simultaneously, the amount of distress placed on the grid will be at concerning levels. As the aforementioned attributes are important influencers of energy efficiency and grid quality, better design alternatives should also be developed for low power LED drivers, regardless of the lack of EMC limitations.

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