An Efficient High-Performance Vedic Multiplier: Review

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Abstract

Multipliers are the most essential block of any processor. Multiplication is one of the important operations in digital signal processors. The processing speed of a ALU is depends on its logic algorithm and complexity of hardware circuitry delay. Basically delay is depending on number of bits increases. For efficient processors, delay should minimum; to minimize delay optimized hardware architecture for process is required. Vedic Multipliers are able to deal with the above credential of minimum hardware architecture. In this review a comprehensive analysis of binary multiplication algorithm and Vedic multiplication algorithm has presented.

Keywords

Vedic multiplier, Urdhva-Tiryagbyham, Highspeed multiplier, binary multiplication algorithm.

I. INTRODUCTION

In Arithmetic operations contain several fundamental functions like Addition, Subtraction, Multiplication, and Division and so on. Multiplication is one of the essential and mostly used functions in arithmetic operations [1]. Arithmetic logical unit and multiply and Accumulate (MAC) are the basic blocks in Digital Signal Processing applications and in these operation multiplication is the basic function to be implemented [1]. In Convolution, Fast Fourier Transform (FFT) and microprocessors we implement DSP applications in their arithmetic and logic units [10]. We need high speed multipliers in DSP processors as these multiplication operations decide their execution time. Currently, the execution time of a digital signal processing chip still depends on the multiplication time.

The recent improvement of technologies in many digital and signal processing applications, the need of high speed processors increased. In many signal and computer applications, high output of the arithmetic operations is needed to achieve the required performance [12]. By reducing the time delay and the amount of power consumed we can meet the requirements of many applications [3]. This article highlights different multiplier architectures and there implementation using Vedic Mathematics. We need to optimize at all levels that involve the design to minimize

power consumption. The technologies and algorithms used to implement the digital circuits must includes this optimization, circuit design, topology used to implement the circuits and the level at which the algorithms are designed. Digital multipliers are the main components used in any digital architecture. To implement any operation we need fast, dependable and competent workings. In many DSP algorithms, the performance of digital signal processor algorithm depends on the multiplier that lies in the critical delay path. The speed and time delay of multiplication operation are important in DSP and also in the general processor. Previously a set of addition, subtraction and shift operations are used to implement the multiplications. Previously, there were a lot of algorithms described to perform multiplication operation, each offering different advantages based on the speed, circuit design, effective area, and time delay, power dissipation and consumption.

In computing system the major block is multiplier. The relation between the circuit design and constancy is, the amount of circuitry involved i.e. size of the device (n) is directly proportional to square of its constancy i.e. constancy is having n^2 gates. For all the multiplication algorithms that are used in DSP applications, the latency and execution time are the two major terms in the time delay perspectives [11].

II. VEDIC MATHEMATICS

The History and Background of Vedic Mathematics

Veda is a Sanskrit word. This word is taken from the source Vid, which means knowing something without boundary. The Veda is a depot of all information, invaluable, still educational as it is investigate deeper.

Former Jagadguru Sankaracharya of Puri (India) Swami Bharati Krishna Tirtha (1884-1960), gathers a set of 16 Sutras (aphorisms) and 13 Sub - Sutras (corollaries) from the ancient Atharva Veda. He proposed a methodology for enhancing the principles enclosed in the aphorisms and their corollaries known as Vedic Mathematics. He established that in the Veda-sakhas, there has been extensive fiction on Mathematics. About 25 centuries ago, the era of Patanjali Veda-sakhas was known to the versatile Vedic scholars, only about ten Veda-sakhas are presently available Vedic scholars in India. The Sutras mainly apply to cover almost every branch of pure and

applied Mathematics to solve complex problems also. The major application of those Sutras saves a lot of time as well as effort in comparison with other formal methods due to the Sutras are formed by logical and rational analysis. The computation techniques of the present computers are follows to underlying the Sutras. 16 Formulas [7] are listed in the Table 1.

Table 1: 16 formulas and its explanations

Formula	Explanations
Ekadhikina Purvena	By one more than the previous one
Nikhilam Navatashcaramam Dashatah	All from 9 and the last from 10
Urdhva-Tiryagbyham	Vertically and crosswise
Paraavartya Yojayet	Transpose and adjust
Shunyam Saamyasamuccaye	When the sum is the same that sum is zero.
Anurupye or Shunyamanyat	If one is in ratio, the other is zero
Sankalana-vyavakalanabhyam	By addition and by subtraction
Puranapuranabyham	By the completion or non-completion
Chalana-Kalanabyham	Differences and Similarities
Yaavadunam	Whatever the extent of its deficiency
Vyashstisamanstih	Part and Whole
Shesanyakena Charamena	The remainders by the last digit
Sopaantyadvayamantyam	The ultimate and twice the penultimate
Ekanyunena Purvena	By one less than the previous one
Gunitasamuchyah	The product of the sum is equal to the sum of the product
Gunakasamuchyah	The factors of the sum is equal to the sum of the factors

This book on Vedic Mathematics is present an easiest way to learning Mathematics by of observation and minimized the monotony of accepting different theories and calculation techniques. The explanations processes are clear to the beginners with the logical proof of the Sutras [7]. The application of the Sutras are also involves rational thinking which helps to create mathematical geniuses of the past and the present scholar of the India as Aryabhata, Bhaskaracharya, Srinivasa Ramanujan, etc.

Vedic Mathematics is carried out by Sri Bharati Krishna Tirthaji. It is filled with numerical expansion of 'Sixteen Simple Mathematical formulae from the Vedas'. Urdhva – tiryagbhyam is the common method appropriate for the division of a large number by another large number and also in all cases of multiplication, i.e. Multiplication of two 2 digit numbers. The processes are represented symbolically in the below table: These codes are worked from right to left.

III. PRIOR APPROACHES

There are many approaches are proposed to design a highspeed and high performance multiplier few recent approaches of high speed vedic multiplier are discussed as follows.

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Fig. 1. Symbolic representation of Urdhva-Tiryagbyham [7].

A. Design of High Performance 8-bit Vedic Multiplier.

Yogendra [1] has proposed a design of 8 bit high performance Vedic Multiplier a design of fast and low power 8-bit multiplier architecture which implements Urdhva-tiryakbyham sutra of Vedic method of multiplication. The multiplier is designed in 180nm technology using cadence EDA tool and simulated using spectre simulator and found to be working correctly and results have been compared for pre-layout and post-layout analysis. It is shown that implementation of multiplier using the Vedic sutra leads to a very compact layout leading to significantly smaller Silicon area and very small contribution of interconnections to the overall propagation delay of the multiplier. The performance of the proposed multiplier has been compared with those of other multipliers reported in literature. Fig. 2 demonstrates the RLT Schematic of 8 bit multiplier circuit.

Fig. 2. Schematic of 8 bit multiplier [1].

B. Vedic Algorithm for Reversible Multiplier.

H.P. Patil [2] Proposed Vedic algorithm for reversible Multiplier Digital Signal Processing and many other microcontroller based applications is essential condition is fast and very low power consumption from the systems. The performance those system depends on the multiplication operation due to it requires more iterations leads to long time. Hence to enhance it performance Vedic algorithm becomes an essential solution. The conventional algorithm “Booth Multiplier” is illustrate in the Fig. 3, where other is the Vedic method “Nikhilam Navatascaram Dasatah” (Fig. 4) is demonstrated in Fig. 5 using reversible logic gates implemented in FPGA environments.

Fig. 3. Flowchart of the Booth Multiplier [2].

C. Vedic Multiplier with Square Architectures

Recently Sharma [3] present a high speed multiplier along with squaring architectures depending on the ancient Indian Vedic sutras or formulas. The partial product terms in the existing Vedic multiplier may be calculated parallel process, latter it sum to the ultimate result. In their proposed method all partial products terms are required to adjust separately by using simple concatenation procedure with single carry followed by high speed multiplier architecture based on Vedic algorithm which is implemented using Xilinx Spartan-3E (Fig. 6). The proposed design methodology is able to achieved 28.72% and 38.59% propagation delay reduction for the equivalent 32-bit multiplier result with the existing multiplier.

Fig. 4. Flow chart of Flowchart of Nikhilam Multiplier [2].

Fig. 5. Block diagram of Nikhilam's reversible multiplier [2].

Fig. 6. Architecture of 2-bit Squaring Circuit [3].

D. Vedic Multiplier Using Barrel Shifter Approach

Using Barrel shifter approach an 8-bit Vedic multiplier with less propagation delay is reported in [4] may be enhanced performances in comparison with conventional multiplier like Braun multiplier, array multiplier, and Wallace tree multiplier or modified booth multiplier. 8-bit barrel shifter is able to shift 'n' times in each clock cycle. The proposed design verified on Xilinx Spartan-6 family and the propagation delay measured only 6.781ns. The schematic block diagram is shown in Fig. 7.

Fig. 7. Multiplier architecture [4].

E. Parallel pipelined Approach

The speed is very important consideration to design any digital system. Multipliers are the most essential part, particularly DSP, image processing, etc. The overall operation speed of the system depends on the multiplication operation. Multipliers based on Vedic mathematics are one of the high speed multipliers in comparison with Booth or Wallace. The major drawback is propagation delay due to longer input size [5]. By using pipelined architecture minimization of the propagation delay is possible. For DCT applications, an 8*11

bit pipelined Vedic multiplier may have a maximum 179.69 MHz clock speed with 225 slices is shown in Fig.8.

Fig. 8. Architecture of parallel pipeline approach [5].

F. Bit Reduction Binary Multiplication

M. E. Paramasivam [6] proposed a low power high speed multiplier based on this method for multiplying two binary numbers. It mainly focuses to increase speed up the operation. It mainly by reducing the bit numbers are required to be multiplied. The algorithm which was proposed fully Vedic based mathematical algorithms. By expansion and bit-shifting which is further optimized in his design. The proposed algorithm was implemented and tested using Verilog. The proposed 4 bit multiplier only dissipates 47.35 mW powers in 3.3 V supply power. The propagation time is 6.63 ns. Fig. 9 demonstrated the chip layout of bit reduction binary multiplier

Fig. 9. Chip Planner of the Bit Reduction Binary multiplier [6]

IV. CONCLUSION

Basically Vedic Multipliers are seems to be very efficient in teams of area power and delay in digital circuitry design as compared to traditional design methodologies. Most electronic signal try to maintain a high SNR i.e. signal to noise ratio all through their internal data paths, similarly maintain high levels of precision performance and integrity by enhancing circuit performance by increasing level of sustaining the signal content. The major efforts can be expensive and the ultimate designs due to single element's immoderate variance that are catastrophically intolerant. All the designs are discussed in this literature review it can be conclude that the Vedic multipliers are the best way of the designing future processor multipliers. Vedic multiplier with Urdhva Tiryabhayam sutra seems to be promising technique outperforms as compared rest of 15 sutras for binary multiplier designing and implementation. The Sutras provide not only methods of calculation, but also ways of thinking for high speed application.

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