Impacts of High Frequency, High di/dt , dv/dt Environment on Sensing Quality of GaN Based Converters and Their Mitigation

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Abstract—A systematic study on a gallium nitride (GaN) high-electron-mobility transistor (HEMT) based battery charger, consisting of a Vienna-type rectifier plus a dc-dc converter, reveals a common phenomenon. That is, the high switching frequency, and high di/dt and dv/dt noise inside GaN converters may induce a dc drift or low frequency distortion on sensing signals. The distortion mechanisms for different types of sensing errors are identified and practical minimization techniques are developed. Experimental results on the charger system have validated these mechanisms and corresponding approaches, showing an overall reduction of input current total harmonic distortion (THD) by up to 5 percentage points and improved dc-dc output voltage regulation accuracy. The knowledge helps engineers tackle the troublesome issues related to noise.

Index Terms—Charger, dc bias, gallium nitride (GaN), sensing, three-phase rectifier, wide bandgap.

I. INTRODUCTION

LOW on-resistance and high switching speed have driven the research, commercialization, and application of wide bandgap (WBG) power semiconductor devices, such as SiC and GaN devices, for a more efficient and compact converter design [1]–[3]. However, as WBG devices are applied in practice, more design issues arise, such as the need for optimal power loop layout and device package to reduce parasitics [4], [5], thermal management for low profile devices [6], gate driver noise immunity for fast switching [7]–[9]. And high di/dt and dv/dt are regarded as the main obstacles to electrical performance improvement of WBG converters. High di/dt induced ringing

and overvoltage in the switching commutation loop introduces high voltage stress, extra loss, and severe radio frequency (RF) emission and electromagnetic interference (EMI). High dv/dt noise often induces spurious gate voltage, resulting in cross-talk issue in bridge configurations. Besides, the high common mode (CM) voltage transient due to high dv/dt may cause the false trigger of gate drive ICs. Many works have been done in addressing these di/dt and dv/dt issues through gate driver design [7], [10]–[14] and power stage optimization [4], [5].

Meanwhile, as switching frequency and speed increase in SiC and GaN based converters, some control challenges have been observed recently in applications of high speed and high switching frequency devices, e.g., zero-crossing detection error occurs in peak current control due to EMI distortion in GaN based high frequency buck [15]; several sensing distortions and conditioning circuit arrangements in 500 kHz GaN full bridge converter are reported [16]; and device parasitics can impact on current harmonics in a high frequency three-level GaN rectifier [17], [18]. These previous studies have clearly shown the impacts of high frequency, high di/dt , dv/dt on sensing, conditioning, and control circuits. However, they were more specifically focused on one aspect of these complex issues and did not provide comprehensive relation between high dv/dt , di/dt , high frequency operation environment and sensing and control.

Particularly, signal sensing and processing in the feedback path become the vulnerable link, as signal integrity issues arise due to capacitive coupling from dv/dt and inductive coupling from di/dt . Although these are commonly perceived by engineers and some are well known in information electronics field, few work has been reported in power electronic field to explain some of the phenomena and effects that are specifically associated with high frequency noise and transients. In the work, it is observed experimentally that high frequency noises in GaN based power converters could surprisingly induce nonlinear dc or low frequency shift on the sensing signals through the sensing and conditioning circuitry and lead to deviation from the desired control track as well as voltage/current distortion, if without a proper design.

In this paper, to address the above challenges in WBG based high switching frequency converter design, a systematical study will be conducted in a proposed two-stage charger consisting of three-level/phase Vienna-type power factor correction (PFC) rectifier and three-level LLC dc-dc converter as shown in Fig. 1. Instead of further stressing the high frequency noise itself, the

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Fig. 1. Schematic of the proposed GaN based two-stage battery charger system including power stage and control structure.

focus will be on illustrating why and how these high frequency distortions produce dc and low frequency sensing error and impact the ac or dc feedback voltage/current control, and the way to mitigate these noises in different situations. Considering that feedback control has no rejection capability for disturbances in the feedback path, understanding and fixing these issues are crucially important.

This paper is organized as follow: Section II presents the overall system topology, the control architecture and sensing arrangement, and the power quality requirement. Section III first introduces several dc and low frequency sensing distortions related to high speed and high frequency WBG converters, and then analyzes the mechanisms of different sensing distortions and proposes the mitigation methods. Of which, one of the major dc bias phenomena and its mechanism and influencing factors presented in subsection A have never been investigated before. Section IV provides experimental results. And Section V concludes this paper.

II. SENSING AND CONTROL ARCHITECTURE IN A GAN BASED CHARGER

A. Control Functions and Sensing Arrangement

A proposed two-stage GaN based battery charger is applied as an example to study the sensing issues. As given in Fig. 1, the front end is a 650V enhancement-mode GaN based three-level Vienna-type rectifier operated at 450 kHz switching frequency [17], [18], and the back end is a three-level LLC resonant dc-dc converter which adopts 650 V GaN devices at the primary side and 100 V EPC devices at the secondary side [19]. The charger converts 115 V_{rms} or 235 V_{rms} ac voltage to a maximum 28 V_{dc} output for batteries in aircraft application.

To properly charge the batteries and efficiently operate the charger, LLC converter is operated in dc transformer mode (DCX) with switching frequency fixed at the resonant frequency. Its dc output voltage and current are regulated indirectly by varying the dc-link voltage of the front-end rectifier, where the dc output voltage and current are sensed as the feedback signals for the constant voltage (CV) and constant current (CC) controllers. The output of CC/CV controller is then used as the reference for PFC dc-link voltage controller, which further generates the inner current control reference for phase current regulation.

For the studied system, three current hall sensors are therefore placed at the ac side, and one hall sensor is placed at the dc output side. Meanwhile, the intermediate dc-link voltage as well as dc capacitor voltage is sensed through differential voltage divider pairs, then processed through an instrumentation amplifier, and finally converted to a single-ended signal, whereas the dc output voltage at the low voltage secondary side is sensed through a voltage divider and transmitted via an analog isolated amplifier before it is processed by conditioning circuit on the interface board.

B. Power Quality Requirement

For grid connected inverters or rectifiers, power quality including current harmonic and power factor limits are required by various standards, such as IEC 61000-3-2 [20], IEEE 519-2014 [21], and DO-160E [22]. For dc-dc converters interfacing with local load, such as POL or back end of a battery charger, the accurate regulation of voltage and current is also required [23], [24]. For this aircraft charger, DO-160E standard is followed in which the limit of each order harmonic up to 40th order is specified and the current total harmonic distortion (THD) should be less than 3%, meanwhile the leading power factor should be above 98%.

Although one may expect that good current quality and voltage regulation accuracy can be more easily obtained as a result of higher control bandwidth and lower switching ripple if pushing the converter to high switching frequency, e.g. exploiting WBG devices, it is not always true due to aforementioned challenges in Introduction. Understanding and mitigating the unique dc and low frequency distortions associated with high-speed high-frequency WBG devices are therefore presented in the following section.

III. SENSING ISSUES AND MITIGATION METHODS

To address these sensing issues in the noisy operation environment, the causes of dc and low frequency bias on sensing signals are firstly understood including two main distortion mechanisms. Mitigation schemes are then discussed for each case.

A. DC Bias from Analog Signal Isolation Amplifier and Mitigation

1) Observed DC Bias on Isolated Voltage Sensing

When isolation is mandatory, voltage or current sensing is often realized by isolation schemes shown in Fig. 2. An analog isolation amplifier (iso-amp) is the key device to achieve the isolation between control and power domains. At the high-power side of an iso-amp, the voltage will be sampled by a resistor divider in a single-ended form or by a divider pair in a differential form. The current will be sampled through a shunt resistor. Then, the isolated sensing signal is processed by downstream conditioning amplifiers and filters before being transmitted to ADC. However, operated in high dv/dt conditions, this scheme is observed to suffer severe distortion, i.e. a nonlinear dc shift, in the GaN based charger system.

Fig. 2. Iso-amp function block and formation of dc bias through CM noise penetration and demodulation.

Although LLC resonant converter has much lower EMI emission, the front-end PFC is operated at hard-switching mode with high dv/dt GaN devices, emitting high amount of noises either conductively or radiationally to its surrounding. Although it is understandable that certain high frequency noise might be coupled onto the sensing signal of LLC output voltage, it is surprising to observe a significant dc bias in the sensed dc voltage. As shown later in Fig. 4, the dc error could be 6 V more.

Because of the sensing voltage shift ΔV_{dc} , the actual voltage regulated by feedback closed loop control is different from the desired value as in (1). This dc error is even larger when the dc-link voltage increases as if a nonlinear voltage-dependent sampling gain exists. For high step-down dc-dc and low output voltage applications, this dc error would be unacceptable.

$$V_{actual} = V_{ref} - \Delta V_{dc} \quad (1)$$

2) Origin of DC Bias

The dc bias from analog signal isolation amplifier in this paper can be understood from the basic structure of an analog iso-amp in Fig. 2, where the analog input is modulated into digital format, e.g. via a sigma-delta ADC at the primary side, and the signal is reconstructed to analog output via a demodulator at the secondary side. An intermediate digital transmitting medium is implemented across the isolation barrier of the iso-amp. As a result, a high CM voltage exists due to the different grounding potential. Taking optical iso-amp as an example, when a rising $v_{CM,r}$ pulse is imposed onto an iso-amp, the internal coupling capacitance of iso-amp induces CM current pulses penetrating the barrier, and a positive differential voltage spike is generated at the output through the pull-up resistor. In addition, the turn-off pulse also induces a negative spike $v_{CM,f}$ at the output. These spikes may falsely toggle the logic level, jeopardize the signal quality of effective signal and finally demodulate analog spikes. Thus, a dc bias can consequently be generated after the downstream filter through the average of these positive and negative analog spikes. This relationship is shown in (2). It should be noticed that the polarity of the spikes could be reversed depending on internal logic of an iso-amp IC.

$$\begin{aligned} \Delta V_{dc,out} &= \int_0^{T_s} (v_{CM,r} - v_{CM,f}) dt / T_s \\ &= f_s \cdot \int_0^{T_s} (v_{CM,r} - v_{CM,f}) dt \end{aligned} \quad (2)$$

Fig. 3. LLC voltage sensing distortion: (a) 450 kHz PFC. (b) 450/4 kHz PFC. Black line outlines the profile of output signal. Dashed magenta line denotes the desired voltage.

3) Impact Factors of dv/dt Induced DC Bias

a) CM dv/dt in power converter

The magnitude of this CM isolation voltage is determined by the dc-link voltage and CM impedance distribution along the whole CM path including grounding parasitics, transformer inter-winding capacitance of dc-dc converter, isolation capacitance of the iso-amp, etc. The edge slopes of this voltage are related to dv/dt of device turn-on and turn-off, determined by specific gate driver, gate resistance, switching speed, and dc-link voltage. The turn-off dv/dt is also strongly impacted by load current level.

b) Asymmetric of dv/dt transient

If the turn-on and turn-off dv/dt are the same, it seems reasonable that a minimum dc bias might be induced per (1). However, in practice, the two dv/dt values might be different due to the junction capacitor charging effect, load current, and different gate drive on/off speed control. For GaN based application, this dv/dt disparity becomes larger. The turn-on transient of 650 V e-mode GaN device is usually less than 10 ns and dv/dt can be above 100 kV/ μ s, while its turn-off transient could last for hundreds of ns at ac current zero crossings [25], [18]. Thus, turn-on dv/dt becomes the primary contributor to the CM transient immunity (CMTI) issue instead of the turn-off dv/dt at low current level or zero crossing. This is further verified by LLC voltage sensing results in experiment with front-end PFC operating at two different switching frequencies. As shown in Fig. 3, the turn-on dv/dt induced negative spikes (below the desired voltage sensing level as marked in dashed magenta line) are almost the same in case (a) and (b), whereas no positive peaks show up except for some noises.

c) Transient speed of iso-amp

The above results also highlight another important distortion factor that was not considered previously, i.e. the output signal rise/fall time of an iso-amp IC. Ideally, the output spike due to dv/dt should only occur during the switching transient. However, it is noticed that at different switching frequencies, the profiles of the output ripples in Fig. 3(a) and (b) have rising ramps which increase linearly from the same negative valley. This is caused by the relatively slow rise time of the iso-amp ACPL-C87B output, roughly 4 μ s [26]. For example, in the 450 kHz switching frequency case, the dv/dt induced spike is reset by the

Fig. 4. Recorded experimental data of LLC output voltage sampling: (a) 450/4 kHz PFC. (b) 450 kHz PFC.

next switching event before it can reach the steady state level within its $2.2 \mu\text{s}$ cycle. Whereas in the 112.5 kHz case, the dv/dt related ripple can jump back to the desired dc voltage in one switching cycle.

d) Switching frequency

Switching frequency will not impact the peak spike of an iso-amp output, but it does impact the dc bias level. This is because: 1) the same noise spike pattern will be averaged over different switching periods, thus the bias is proportional to f_s , as shown in (2); 2) the noise spike of an iso-amp may not reach the correct sensing level if the switching cycle is too short as analyzed above. As a result, high frequency induces more dc sensing drift.

From the experimental results in Fig. 4 recorded by DSP controller, the sampling voltage of LLC output marked in red is compared with the actual voltage marked in blue predicted via the intermediate dc-link voltage and the LLC dc gain (matching the digital meter measurement), at two different frequencies. In the steady-state when the front-end PFC is activated after the soft-start and diode rectification, LLC output voltage sampling begins to suffer high dc shift, and it is clear that this dc shift becomes much higher when PFC is operated at 450 kHz compared to the case at $1/4$ of 450 kHz .

In sum, the speed of iso-amp, i.e. the rise/fall time, impacts the sensing output distortion induced by CM spikes. More instantaneous distortions and dc bias will be introduced when higher switching frequency, lower speed sensing iso-amp, and higher speed devices are adopted.

4) Mitigation Solutions

The above analysis has shown that the dc bias issue is not just by the switching noise propagation, but it is at the basis of the demodulation of the interference. With high CMTI and fast speed iso-amp, this effect could be suppressed. Unfortunately, the CMTI of the commercial analog iso-amp is relatively low in comparison with GaN device turn-on dv/dt . TABLE I lists the state-of-the-art commercial iso-amps. As it can be seen, the CMTI of some products is not precisely defined [26], [27]. Detailed information of iso-amp error levels vs. CM voltage or dv/dt is also unknown, which further increases the difficulty of sensing circuit design. The state-of-the-art commercial voltage

TABLE I
KEY PARAMETERS OF STATE-OF-THE-ART COMMERCIAL AVAILABLE ANALOG ISOLATION AMPLIFIERS

Amplifier names	Isolation techniques	Bandwidth (kHz)	CMTI (kV/ μs)	t_r and t_f (μs)
ACPL-C87B	Optical	100	^a 15 (typ), 10 (min)	2.7 (typ), 4.0 (max)
ACPL-790B/A/0	Optical	200	^a 15 (typ), 10 (min)	1.7 (typ)
Si8920A/B	CMOS	950	^b 75 (typ), 50 (min)	0.42 (typ)
AMC1311B	SiO ₂	275	^c 140 (typ), 75 (min)	1.3 (typ)
AMC1311	SiO ₂	220	^c 30 (typ), 15 (min)	1.3 (typ)

^aCMTI failure is defined as the output error of 200 mV deviation from the average output voltage persisting for at least $1 \mu\text{s}$, tested at $V_{CM} = 1 \text{ kV}$.

^bCMTI failure is defined as the output error of more than 100 mV persisting for at least $1 \mu\text{s}$, tested at $V_{CM} = 1.5 \text{ kV}$.

^cCMTI failure definition is not specified, tested at $V_{CM} = 1 \text{ kV}$.

sensing iso-amp was from Avago before year 2018, typical with $15 \text{ kV}/\mu\text{s}$ CMTI [26] using optocoupler isolation, and current sensing iso-amp has up to $75 \text{ kV}/\mu\text{s}$ CMTI [27] using CMOS isolation. Thus, CMOS based iso-amp is a better option currently, since it shows higher CMTI due to RF transmission. To be noted, recently an even higher CMTI voltage sensing iso-amp AMC1311B from Texas Instruments was released in early 2018 [28].

To obtain better voltage sampling quality in high dv/dt operation, the $75 \text{ kV}/\mu\text{s}$ CMTI current sensing iso-amp Si8920B from Silicon Lab is finally selected, considering its tight CMTI definition and higher CM testing voltage, as well as the fastest rise and fall time during the transient. In order to apply this amplifier for voltage sensing, reconfiguration is needed. Since the internal input resistance of this shunt-input iso-amp is much lower than the typical high impedance of the voltage sensing iso-amp, e.g. $37 \text{ k}\Omega$ only for Si8920B, the resistance of the voltage divider should be properly selected. Higher resistance will lead to the failure of impedance mismatching, while a lower value will introduce additional power loss. The trade-off between the sensing accuracy in terms of voltage divider load dependence and the extra loss introduced by sensing resistors is thus required for a set of given system parameters. For 28 V sampling using Si8920B, as the allowable input voltage is within 0.25 V , the voltage divider ratio is determined as 175. The sensed lower side resistor is chosen as 110Ω and the upper resistor is $19.1 \text{ k}\Omega$, giving a total 40 mW loss at 28 V . Both have 0.1% high accuracy. Impedance mismatch ratio between 110Ω and $37 \text{ k}\Omega$ is 0.3% , ensuring enough accuracy for this current sensing iso-amp.

Optionally, common mode filters may be possible to use at the high side of the iso-amp to limit the CM voltage across the iso-amp. This will be similar to the approach for CMTI enhancement of the gate driver [29]. However, the power supply lines should also be in series with the CM filter to avoid

Fig. 5. Experimental waveforms of ac current sampling: (a) 450 kHz PFC. (b) 450/4 kHz PFC. (Ch1: sampled signal, Ch3: current probe result)

Fig. 6. Experimental waveforms of ac current sensor output with 450 kHz PFC. (a) Higher line current instant. (b) Lower line current instant. (Due to 25 MHz low bandwidth voltage probe used in the test, only the noise envelop is captured where the higher frequency oscillations are not accurate.)

high CM voltage stress across the high side pins of the iso-amp.

B. DC Bias From RF Interference Rectification in Op-amp and Mitigation

For silicon device switching at tens of kHz, a moderate filter implemented in the conditioning circuitry is sufficient to guarantee the integrity of sensed signals. However, when using the similar design principles in GaN based converters, the experimental results reveal that the voltage and current sensing signals along the conditioning circuitry could see a pronounced dc offset or low frequency distortion, which further grows as dc bus voltage or switching frequency increases. An example of ac current sensing at 450 kHz and 112.5 kHz switching frequencies in a GaN based Vienna-type rectifier is provided in Fig. 5, where the sampling signal outputted by digital-to-analog converter (DAC) is much different from the Keysight current probe result. At higher switching frequency, this low frequency or dc shift becomes larger. It should be mentioned the poor quality of the ac current is due to several distortions including the sensing distortion, sampling distortion [30], [31] and the PWM voltage loss during the current zero crossings [18].

1) Identification of Observed Sensing Noise Pattern

To identify the cause of this distortion, the output signal of the hall sensor is checked. High switching transient noises are observed in the sensor output as shown in Fig. 6. Since the onboard sensor is placed close to the main power loop, the noise is found induced by high di/dt of switching transients. And noise at turn-on seems more pronounced than that at turn-off, which can be explained from the fact that at turn-off,

Fig. 7. Comparison between onboard sensor output (blue) and current probe result (magenta) at different current levels with 450 kHz PFC in switching cycle scale. (a) Current instant at the positive line cycle. (b) Current instant at the negative line cycle.

commutation from off-device to on-device is largely determined by load current charging.

The sensor output, ADC sampling, and probe measurement are further compared. From results in Fig. 7, both the sensor output and final ADC sampling have dc shift distortion in switching period scale and low frequency distortion in line period scale. Although the coupled noise and dc shift patterns may be different at different operation points, making the analysis intricate, some key observations are captured: 1) due to the asymmetric nature of the coupled HF noise as mentioned in Section III-A, the mean value of sensor output over a switching period can be shifted from the original level and falsely conveyed to the downstream conditioning amplifier; 2) this dc shift is thus influenced by switching frequency; 3) the fact that an offset also exists between the envelopes of the sensor output and probe result, indicates the sensor itself is also affected by the HF noise.

2) Origin of DC Bias and Low Frequency Distortion

Eventually it is found that this dc severe distortion is determined by the amount of high di/dt induced noise picked up by signal-ground traces between sensor output and conditioning amplifier input. And the cause of this dc bias is the radio frequency interference (RFI) rectification effect on operational amplifiers (op-amp) [32]–[39], a phenomenon seldom considered in power converter field. According to it, when an op-amp sees high frequency out-of-band noises at its input, its output can induce an instantaneous dc shift due to the nonlinear I-V characteristics of differential transistor pairs at its input stage. And the strength and envelop of the time-domain bias are dependent on the amplitude, frequency and continuity of the input coupled out-of-band noise. Furthermore, noise coupled at the output of an op-amp can also contribute to the input noise via its feedback path. This explains why dc shift at current sensor output was observed, as an internal op-amp exists at the output stage of the current sensor to provide desired quiescent bias [41], [42].

To help understand this rectification effect for power engineers, a brief introduction is provided. RFI rectification was firstly observed in naval research on the susceptibility of transistors to microwave energy [32], [33]. Since then, the effects and mechanisms of RFI distortion on analog and digital ICs have been investigated experimentally and theoretically, in both time domain and frequency domain [32]–[39]. Analog

electronics, in particular, the amplifiers are most susceptible to the EMI noise. Technical notes from industry have attributed the dc bias effect on op-amp to the nonlinear transfer characteristics of its input transistors, e.g., emitter-coupled BJT has exponential I-V curve and source-coupled JFET or CMOS have quadratic I-V curve [34], [35]. Although this theory can confirm the observation that BJT-based amplifiers typically suffer higher RFI distortion than other types, it fails to explain why this effect only occurs at out-of-band frequencies and why the dc offset varies with frequencies. The frequency-dependent nonlinearity and dc bias level was later analytically modeled in [36] for a CMOS op-amp, indicating that the parasitic capacitances C_{gs} of input differential pairs and their total source-to-ground capacitance are the determinants. The mechanism of negative feedback on dc bias was also revealed in [36], [37] for CMOS op-amp. It is noticed that some models are only valid at low level RF input, i.e. two transistors of the input differential pairs are both in saturation region [37], while other models may be feasible for both saturation region and subthreshold region where large signal noise switches the transistor on and off [36].

The susceptibility of an amplifier to RFI EMI can be evaluated by a rejection ratio (EMIRR) [38], from which the corresponding dc bias can be estimated as (3). However, this is only valid at low amplitude EMI/RF [39].

$$\Delta V_{dc} = \frac{1}{10^{\left(\frac{EMIRR_{dc}(dB)}{20}\right)}} \left(\frac{V_{RF_peak}}{100mV} \right)^2 \quad (3)$$

To further verify the RFI offset issue identified in this work and evaluate EMIRR of the adopted op-amp OPA2227 in cascaded inverting configuration for feedback current conditioning, offline characterization of the OPA2227 is carried out, whose test setup is provided in Fig. 8, using a signal generator to mimic the output of the hall sensor with varying HF noise and injecting the EMI source via a 50 Ω BNC cable.

From results in Fig. 8(b), as RFI amplitude increases, the dc shift becomes larger and occurs earlier. This dc offset also presents nonlinear frequency characteristics. It grows larger as frequency increases from 500 kHz to 2 MHz and then drops back to almost zero around 10 MHz. Testing at even higher frequency is not performed, due to measurement complexities involving reflection effects of input cable, PCB traces and op-amp pins.

3) Mitigation Approaches

A straightforward approach to mitigate the RFI effect is to attenuate EMI noise before the input pins of an op-amp. RC-based CM and DM filters have been built in some commercial amplifiers [35]. However, the filter corner frequency is usually set above tens of MHz to serve general purposes, beyond interested frequency range of the state-of-the-art GaN based power converters. Therefore, a set of external EMI filter should be provided for converter sensing design, as shown in Fig. 9.

For single-ended signals, RC or LC filter can be applied whose bandwidth should be selected between the current control bandwidth frequency and the high switching frequency,

Fig. 8. EMIRR characterization of op-amp OPA2227 in current conditioning circuit. (a) EMIRR measurement setup. (b) Measured RFI induced dc offset on OPA2227 with cascaded inverting configuration.

Fig. 9. Recommended filter approaches to mitigate amplifier RFI issue. (Upper for general op-amp and lower for differential amplifier).

e.g. in the middle range, without impacting obvious delay to the feedback control. For differential sensing signals, both CM and DM filters should be adopted following similar design consideration, where the DM filter corner frequency is determined by (4) and the CM filter corner frequency decided by (5) can be slower as it does not affect the feedback control.

$$f_{DM} = \frac{1}{2\pi R_y (2C_x + C_y)} \quad (4)$$

$$f_{CM} = \frac{1}{2\pi R_y C_y} \quad (5)$$

However, unlike signal processing, power conversion deals with high voltage and current. Particularly, in GaN based converter, high di/dt , dv/dt and high frequency could likely

induce strong noise coupling. Relying purely on filter itself is not effective enough to eliminate RFI noise without sacrificing sensing bandwidth. In fact, as earlier work reported in [16], the pre-filtered voltage sensing circuit can still be distorted once active power control is activated, leading to the design compromise by moving the local sensing circuit of the power board far away and placing onto another board. This prevents further degrees of power function integration, especially for intelligent power module design.

Differently, this paper will show that the direct control of the noise source and associated coupling path is more effective and straightforward. Taking current sensing distortion as an example, if tracing back to the source of the hall sensor noise, it is actually induced by high di/dt current circulated in the switching loop and then coupled onto the signal side of the sensor through space magnetic coupling. Given the fixed di/dt , smaller power loop means less diffusing magnetic field generation, thus reduces the magnetic coupling. However, less loop inductance can adversely induce higher di/dt and dv/dt [40]. Since power loop layout has been well studied in literature, details are not covered here. Instead, this paper emphasizes the importance of signal loop layout for sensing design. In high power density converter design, surface-mount hall sensor chip is preferred due to its low profile and weight. When it is placed on the power board close to converter terminals, longer traces of control power supply nets and output nets are needed to interface with the control board, thus prone to taking in the high di/dt induced voltage noise. Therefore, an effective solution is to layout the sensor circuit and the conditioning circuit with the lowest loop area, in addition to the front-end filters. The basic concept is shown in Fig. 10, where three traces including control ground, control power line, and sensing signal should all be tightly placed on both the power board and the control board.

To implement this scheme, a vertical trace arrangement is proposed to minimize the area of two types of signal loops. In addition, the hall sensor interface loop and power supply loops should be paralleled to the flux orientation and orthogonal to the switching loop, so that the coupling could also be reduced.

Two layout designs are developed for the three-phase ac current sensing. The three-phase sensors are placed next to the switching nodes of the rectifier, and their low side signals have to go across three power traces to the interface connector on the left side where the control interface board is stacked. Compared to the design in Fig. 11(a) with large VCC-GND loop and signal-GND loop on phase B and C, the improved current sensor layout for phase B and C is proposed in Fig. 11(b). The first improvement is that multi-radial power lines are applied for all three sensor chips instead of the central power lines. This decouples possible noises among three-phases and ensures good power quality for each sensor. VCC lines for three sensors directly connect to the main VCC plane, and GND lines also start directly from the GND plane. In addition, all signals are embedded in the mid-layers and overlaid with power lines, to form vertical loops with minimized coupling area. And next to each sensor, reasonable size ground plane is also designed to provide a stable ground potential to each chip.

Finite element analysis (FEA) has been conducted to study

Fig. 10. RFI noise suppression approach through PCB layout for op-amp based sensing circuit. EMI filter can be optional.

Fig. 11. Comparison of current sensor layouts on main power board. (a) Large VCC-GND (upper) and signal-GND (lower) loops in the first version design. (b) Small VCC-signal-GND vertical loops with radial power distribution of the improved layout. Top view (upper), bottom view (lower).

the impact of layout approaches to the loop inductance as shown in Fig. 12. The final measured loop inductance includes the series inductance from the PCB traces formed by the internal trace-self-inductance and external trace-self-inductance, and the negative mutual-partial inductance from the loop which is inversely proportional to the distance between loop segments [43]. As the loop area is shrunk, the negative mutual-partial inductance is maximized and thus effectively cancels or counteracts the external trace-self-inductance that will link/couple with the power switching loop nearby. From Fig. 12, the improved layout has only 17.2 nH loop inductance, reducing 2/3 of that in the original layout.

4) Discussion of Other Noises and Mitigation

Since the magnetic strength is inversely proportional to

Fig. 12. Selective FEA results of current sensor layouts on main power board. (a) Large loop in the first version design. (b) Small vertical loops with radial power distribution in the improved design.

the distance, another conservative but effective approach is to move hall sensors far away from the power loop, which is also experimentally verified but at the cost of larger board space.

Apart from di/dt inductive coupling noise, other noises also exist for hall sensors. For example, dv/dt capacitive coupling from high voltage side to signal side of the hall sensor IC could also superpose significant noise onto the low-level sensor output via the isolation capacitance [41], [42]. Recommendations are: 1) placing hall sensors at non- dv/dt nodes, such as after filter inductors which absorb voltage dv/dt in the first place [16]; 2) choosing hall sensor chips with internal capacitive shielding can also avoid this type of distortion [42], and is applied in this design; 3) adding proper filter for this HF noise is also suggested [41]. However, that alone may be ineffective, since a dc offset can still be produced if dv/dt patterns at turn-on and off are not symmetric, following the mechanism disclosed in Section III-A.

C. DC Bias due to RFI Rectification in In-amp and Mitigation

Aside from op-amp, instrumentation amplifier (in-amp) is typically used for high voltage sensing where strong CM signals can be eliminated by the differential structure. However, the typical common mode rejection ratio (CMRR) of in-amps rolls off at 200 Hz, only remaining 20~30 dB at 100 kHz, and the in-amp has only up to 20 kHz bandwidth [35]. If a strong RFI noise is coupled at the input and is not

Fig. 13. Combined RFI noise suppression approach through PCB layout and EMI filter for in-amp based sensing circuit.

effectively suppressed, the dc rectification effect happens as well [34], similar to the RFI issue in the above op-amp case. Choosing an in-amp with higher EMI robustness is always the first design choice, however, decent immunity at low voltage signal level can barely cover the high noise strength in power conversion systems.

More practical mitigation in power electronics applications should be again to reduce the noise from its source. The first typical solution is inserting external EMI filter pairs at inputs of the in-amp, with both CM and DM filters implemented by RC filters, chokes, or X2Y capacitors, as shown in Fig. 13.

To be noted, the divider impedance network should also be considered for the input EMI filter design, otherwise improper filter characteristics may affect the control bandwidth of the voltage regulator due to the enlarged phase delay of the filter. Based on the Thevenin theory, the equivalent source impedance from the sensing voltage side is $R_H // R_L$, thus corner frequencies for CM and DM filters are respectively

$$f_{CM} = \frac{1}{2\pi (R_H // R_L + R_Y) C_Y} \quad (6)$$

$$f_{DM} = \frac{1}{2\pi (R_H // R_L + R_Y) (2C_X + C_Y)} \quad (7)$$

Clearly, neglecting the divider impedance $R_H // R_L$ in the filter will lead to selection of higher R_Y and cause underestimated phase delay and much slower voltage controller dynamics than one would expect. Similarly, failure to model it in the control transfer function should also be prohibited. In the case of RC filter, since $R_H // R_L$ is often above tens of k Ω , R_Y and C_X could be removed to simplify the conditioning circuit. If LC filters are used, a second-order RLC circuit analysis would be needed to properly determine the cut-off frequency and damping factors.

Another solution is to minimize the signal coupling loop. Different from the single-ended signal, the differential sensing circuit shown above contains two types of signal trace loops between the sensing divider and the in-amp: the differential-mode signal loop and the common-mode signal-GND loop. When it comes to PCB trace layout for the differential signal, the CM ground loop is often overlooked. In fact, it is as important as the DM loop. Since the high di/dt can induce significantly high CM and DM noise voltage on the control interface circuit, the CM noise voltage will also be imposed on the in-amp pins. High stress of such CM noise not only causes clamped 0-volt output of the in-amp (since

its allowable input CM voltage is limited within its power supply voltage and decreases as its DM voltage increases), but also introduces heavier RFI effect as the RFI rectification involves CM and DM noises simultaneously [36], [37]. Reducing both noises and minimizing both types of trace loops is a must. This requires delicate layout on the power board to minimize not only the gap between the differential signal pairs as short as possible but also the gap between signal pairs and the signal ground, where the ground wire can be vertically placed through the multi-layer PCB design. The signal connection from the power board to the control interface board should also be short and compact until the three signal traces safely land onto the controller ground plane. On the interface board, the differential pair should continue to follow the best practice as mentioned to reduce the possible coupling noise.

IV. EXPERIMENTAL VERIFICATION

The above sensing issues have been observed and mitigated in the charger design, whose prototype information can be found in [18], [19]. Through this paper, two major mechanisms have been revealed in power electronic field applications. The mitigation performance is now examined in this section.

A. CM dv/dt Impact and Mitigation

Because of the high CM dv/dt of GaN devices, especially the hard-switching action of the front-end PFC, the LLC dc output voltage sensing signal has suffered from the dc bias noise, as already shown in Fig. 3 and Fig. 4, when the voltage sensing is through a widely adopted voltage sensing iso-amp ACPL-C87 which has been successfully applied in many commercial Si device based converter products for many years. Owing to the significantly high dv/dt in GaN based converter, the CM dv/dt noise immunity becomes a new issue as studied in this paper. To reduce the noise, a current sensing iso-amp Si8920B is configured to sample the LLC output voltage, to replace the prior voltage sensing iso-amp ACPL-C87. Thanks to the high CMTI up to 75 kV/ μ s of Si8920B and its high speed (rise/fall time is 0.42 μ s), the dc bias on the desired dc sensing signal is effectively suppressed over the whole operation range of the two-stage charger. In addition, RFI rectification dc bias from its downstream in-amp and op-amp is also eliminated after minimizing all sensing circuit ground loops and the output differential pair loop as well as adding RC based EMI filters. The final voltage sampling result is accurately controlled at the given reference value 27 V with 650 V dc-link bus voltage, as shown in Fig. 14. Compared to the prior result in Fig. 4, significant improvement on dc bias mitigation has been achieved.

B. RFI Impact and Mitigation

To illustrate this di/dt effect and improvement through the new layout approach, sensing waveforms tested under 300 V_{dc} and 450 kHz switching frequency without any control compensation are compared.

Fig. 14. Eliminated dc sensing shift and accurate dc regulation with the proposed sensing solution.

Fig. 15. Photo of ac/dc PFC prototype with revised input current sensor layout (top-overlaid gate driver board is removed).

Fig. 16. Current sensing waveforms. (a) Current sensing distortion based on the old layout. Ch1: sampled signal via DAC output; Ch3: current probe output; Ch4: conditioning output signal. (b) No sensing distortion based on the improved layout. Ch1 and Ch2: outputs of hall sensors, Ch3 and Ch4: outputs of current probes.

Fig. 15 provides the prototype of the ac-dc PFC stage with the improved layout for the current sensing circuit, highlighting the power switching loops and the hall sensors. Fig. 16(a) gives the output of the conditioning circuit in green, sampling result from DSP in blue, and current probe result in magenta, with the first version layout. Disruptive distortion on the output of current sensor was observed, compared to the result of current probe. After adopting the new layout, all sensor outputs became clean, matching the actual shape of current waveforms obtained from current probes, as given in Fig. 16(b). This lays a solid basis for

Fig. 17. Reduced current THD with proposed current sensor layout 2 avoiding high di/dt noise coupled from power switching loops.

current quality control.

The impact of current sensor distortion on current harmonic distribution is also provided in Fig. 17. Compared to the case with distorted current sensors, tested at 115 V_{rms} input, 600 V_{dc} output, and 450 kHz, the proposed layout improves sensing signal quality and thus reduces phase current THD from 14.3 to 9.3 percentage points, before involving any further compensation [18] or sampling scheme [30], [31].

V. CONCLUSION

In this paper, different sensing distortions observed when adopting GaN devices in high frequency application are reported and their mechanisms investigated. The corresponding mitigation methods from noise source, propagation path, and noise receptor are studied and experimentally verified. Three types of sensing distortions are found strongly impacted by di/dt , dv/dt and switching frequency, all related to undesired high frequency behaviors of different amplifiers. Mitigation solutions are proven effective in improving the sensing quality and minimizing the influences on feedback control and finally help reduce the ac input current THD by 5 percentage points and eliminate the dc output voltage drift from 6-volts to almost 0-volt in a 28 V_{max} battery charger. It is expected that the discussed noise issues, associated mechanisms, and noise mitigation solutions can be applied to other WBG converters and the results can facilitate converter control design.

REFERENCES

- [1] E. A. Jones, F. Wang, and D. Costinett, "Review of commercial GaN power devices and GaN-based converter design challenges," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 3, pp. 707–719, Sept. 2016.
- [2] H. Li, X. Zhang, Z. Zhang, C. Yao, F. Qi, B. Hu, *et al.*, "Design of a 10 kW GaN-based high power density three-phase inverter," in *Proc. IEEE Energy Conv. Congr. Expo.*, 2016.
- [3] C. Zhao, B. Trento, L. Jiang, E. Jones, B. Liu, Z. Zhang, *et al.*, "Design and implementation of a GaN-based, 100-kHz, 102-W/in³ single-phase inverter," *IEEE J. Emerg. sel. Topics Power Electron.*, vol. 4, no. 3, pp. 824–840, Sept. 2016.
- [4] X. Zhang, Z. Shen, N. Haryani, D. Boroyevich, and R. Burgos, "Ultra-low inductance vertical phase leg design with EMI noise propagation control for enhancement mode GaN transistors," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2016, pp. 1561–1568.
- [5] Z. Liu, X. Huang, F. C. Lee, and Q. Li, "Package parasitic inductance extraction and simulation model development for the high-voltage cascode GaN HEMT," *IEEE Trans. Power Electron.*, vol. 29, no. 4, pp. 1977–1985, Apr. 2014.
- [6] GaN Systems, "GN005_PCB thermal design guide for GaN enhancement mode power transistors," [Online]. Available: <http://www.gansystems.com/whitepapers.php>.
- [7] Z. Zhang, F. Wang, L. M. Tolbert, and B. J. Blalock, "Active gate driver for crosstalk suppression of SiC devices in a phase-leg configuration," *IEEE Trans. Power Electron.*, vol. 29, no. 4, pp. 1986–1997, Apr. 2014.
- [8] E. A. Jones, F. Wang, D. Costinett, Z. Zhang, and B. Guo, "Cross conduction analysis for enhancement-mode 650-V GaN HFETs in a phase-leg topology," in *Proc. Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, 2015, pp. 98–103.
- [9] R. Xie, H. Wang, G. Tang, X. Yang, and K. J. Chen, "An analytical model for false turn-on evaluation of high-voltage enhancement-mode GaN transistor in bridge-leg configuration," *IEEE Trans. Power Electron.*, vol. 32, no. 8, pp. 6416–6433, Aug. 2017.
- [10] Z. Zhang, F. Wang, L. M. Tolbert, B. J. Blalock, and D. J. Costinett, "Active gate driver for fast switching and cross-talk suppression of SiC devices in a phase-leg configuration," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2015.
- [11] Z. Zhang, J. Dix, F. Wang, B. Blalock, D. Costinett, and L. Tolbert, "Intelligent gate drive for fast switching and cross-talk suppression of SiC devices," *IEEE Trans. Power Electron.*, vol. 32, no. 12, pp. 9319–9332, Dec. 2017.
- [12] Semisouth. AN-SS1, Silicon carbide enhancement-mode junction field effect transistor and recommendations for use. [Online]. Available: <http://www.semisouth.com>.
- [13] Avago Technologies, Active Miller clamp. [Online]. Available: <http://www.avagotech.com>.
- [14] Silicon lab, Si827x Data Sheet. [Online]. Available: <https://www.silabs.com/documents/public/data-sheets/Si827x.pdf>.
- [15] M. Biglarbegan, S. J. Nibir, H. Jafarian, J. Enslin, and B. Parkhideh, "Layout study of contactless magnetoresistor current sensor for high frequency converters," in *Proc. IEEE Energy Conv. Congr. Expo.*, 2016.
- [16] L. Xue, D. Boroyevich, and P. Mattavelli, "Driving and sensing design of an enhancement-mode-GaN phase leg as a building block," in *Proc. IEEE 3rd Workshop Wide Bandgap Power Devices Appl. (WiPDA)*, Nov. 2015, pp. 34–40.
- [17] B. Liu, R. Ren, Z. E. A. Jones, F. Wang, D. Costinett, and Z. Zhang, "A compensation scheme to reduce input current distortion in GaN based 450 kHz three-phase Vienna type PFC," in *Proc. IEEE Energy Conv. Congr. Expo.*, 2016.
- [18] B. Liu, R. Ren, E. Jones, F. Wang, D. Costinett, and Z. Zhang, "A modulation compensation scheme to reduce input current distortion in GaN based high switching frequency three-phase three-level Vienna type rectifiers," *IEEE Trans. Power Electron.*, vol. 33, no. 1, pp. 283–298, Jan. 2018.
- [19] R. Ren, B. Liu, E. A. Jones, F. Wang, Z. Zhang, and D. Costinett, "Capacitor-clamped, three-level GaN-based dc-dc converter with dual voltage outputs for battery charger applications," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 3, pp. 841–853, Sept. 2016.
- [20] Int. Standard IEC 61000-3-2, "Limits for harmonic current emissions (equipment input current ≤ 16 A per phase)," May 2014.
- [21] IEEE 519–2014, IEEE Standards Association, 2014. [Online]. Available: <http://standards.ieee.org>.
- [22] RTCA DO-160E, "Environmental conditions and test procedures for airborne equipment," Dec. 2004.
- [23] Intel, Voltage regulator-down (VRD) 11.1 processor power delivery design guidelines.
- [24] XP Power, Power Supply Technical Guide 2010/11, Technical Notes.
- [25] E. Jones, F. Wang, and Z. Zhang, "Analysis of the dv/dt transient of enhancement-mode GaN FETs," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Mar. 2017.
- [26] Broadcom, Precision optically isolated voltage sensor. [Online]. Available: <https://www.broadcom.com/products/optocouplers/industrial-plastic/isolation-amplifiers-modulators/isolation-amplifiers/acpl-c87b>.
- [27] Silicon labs, Isolated amplifier for current shunt measurement. [Online]. Available: <https://www.silabs.com/documents/public/data-sheets/si8920-datasheet.pdf>.

- [28] Texas Instruments, AMC1311x High-Impedance, 2-V Input, Reinforced Isolated Amplifiers. [Online]. Available: <http://www.ti.com/lit/ds/symlink/amc1311.pdf>.
- [29] P. Karutz, S. D. Round, M. L. Heldwein, and J. W. Kolar, "Ultra compact three-phase PWM rectifier," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2007, pp. 816–822.
- [30] B. Liu, R. Ren, Z. Zhang, F. Wang, and D. Costinett, "A sampling scheme for three-phase high switching frequency and speed converter," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2018, pp. 3031–3035.
- [31] F. Wang and B. Liu, (2018) GaN in AC/DC Power Converters. In: Meneghesso G., Meneghini M., Zanoni E. (eds) Gallium Nitride-enabled High Frequency and High Efficiency Power Conversion. Integrated Circuits and Systems. Springer, Cham. http://doi.org/10.1007/978-3-319-77994-2_7.
- [32] R. A. Amadori, V. G. Puglielli, and R. E. Richardson, "Prediction methods for the susceptibility of solid state devices to interference and degradation from microwave energy," in *Proc. 1973 Int. Symp. Electromagn. Compat.*, 1973, pp. 1–17.
- [33] R. E. Richardson, V. G. Puglielli, and R. A. Amadori, "Microwave interference effect in bipolar transistor," *IEEE Trans. Electromagn. Compat.*, vol. EMC-17, pp. 216–219, Nov. 1975.
- [34] W. Kester, System applications guide, Analog Devices Inc., 1993.
- [35] C. Kitchin and L. Counts, A designer's guide to instrumentation amplifiers, 3rd ed., Analog Devices Inc., 2006.
- [36] F. Fiori and P. S. Crovetto, "Prediction of high-power EMI effects in CMOS operational amplifiers," *IEEE Trans. Electromagn. Compat.*, vol. 48, no. 1, pp. 153–160, Feb. 2006.
- [37] F. Fiori, "A new nonlinear model of EMI-induced distortion phenomena in feedback CMOS operational amplifier," *IEEE Trans. Electromagn. Compat.*, vol. 44, no. 4, pp. 495–502, Nov. 2002.
- [38] Texas Instruments, EMI rejection ratio of operational amplifiers, application report, SBOA128, 2011.
- [39] M. B. Aimonetto and F. Fiori, "On the effectiveness of EMIRR to qualify opAmps," in *Proc. 2015 Int. Symp. Electromagn. Compat.*, Dresden, 2015, pp. 40–44.
- [40] Z. Zhang, "Characterization and realization of high switching-speed capability of SiC power devices in voltage source converter," Ph.D. dissertation, the University of Tennessee, Knoxville, 2014.
- [41] LEM, LTSR: ASIC based closed-loop transducers from 6 A up to 25 A nominal with reference access. [Online]. Available: http://www.lem.com/images/stories/files/Products/P1_5_1_industry/E_CH23103.pdf.
- [42] Allegro, ACS710: 120 kHz bandwidth, high-voltage isolation current sensor IC with integrated overcurrent detection. [Online]. Available: <http://www.allegromicro.com/en/Products/Current-Sensor-ICs/Zero-To-Fifty-Amp-Integrated-Conductor-Sensor-ICs/ACS710.aspx>.
- [43] B. Liu, R. Ren, E. Jones, H. Gui, Z. Zhang, R. Chen, F. Wang, and D. Costinett, "Effects of junction capacitances and commutation loops associated with line-frequency devices in three-level ac/dc converters," *IEEE Trans. Power Electron.*, Oct. 2018 (Early access). doi: 10.1109/TPEL.2018.2876610.

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