Control of Neutral-Point Voltage in Three-Phase Four-Wire Three-Level NPC Inverter Based on the Disassembly of Zero Level

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Abstract—It is important to maintain the neutral-point (NP) voltage balanced for the three-phase four-wire three-level neutral-point clamped (NPC) inverter. In this paper, after detailed discussion, a mathematical model of the neutral-point voltage are derived. Then a novel control strategy is proposed based on the disassembly of zero level (O Level) to maintain the neutral-point potential. A variable named neutral-point control margin (NPCM) is defined to represent the disassembly margin of each phase. The zero level of one of the three phase is disassembled quantitatively after calculation. Furthermore, the neutral-point voltage can keep balanced while the average output voltage remains unchanged. The proposed control strategy is verified by simulation and experiments.

Index Terms—Neutral-point control margin, neutral-point voltage balance, three-level NPC converters, three-phase four-wire.

I. INTRODUCTION

THREE-PHASE four-wire inverter is widely adopted in industrial applications, such as active power filter (APF), distribution static compensator (DSTATCOM) and uninterrupted power source (UPS). This is mainly because it can generate and control zero-sequence component independently [1]–[3].

Among all the three-phase four-wire inverters, the three-level neutral-point-clamped (NPC) inverter is one of the most popular type because of less switching stress, switching loss and lower EMI [4]. In three-phase four-wire applications, there are mainly two ways to provide the neutral line: one is to use the three-level four-leg NPC topology [5]–[7]; and the other is to connect the neutral-point of the DC bus to the midpoint of the three-phase load. This is called three-leg split capacitor NPC inverter [8]. Although it is easier to control the zero-sequence component in the four-leg topology, it needs more switching components, diodes, pulse-triggered terminals and drives, which increase the cost and complexity of implementation. The three-leg split capacitor NPC inverter is a more economical solution, and is easier to control. Hence, the three-level three-leg NPC inverter, as shown in Fig. 1, is researched in this paper.

Due to the structural characteristics, the NP voltage must be maintained balanced to ensure the normal operation of

three-level NPC inverter. Many strategies have been proposed to balance the NP voltage, which can be mainly divided into the two categories. The first one is based on space vector modulation (SVPWM). There are 27 vectors of 19 kinds in a three-level NPC converter. As a result, the balance of NP voltage can be achieved by modifying the appropriate redundant small vectors and adjusting the dwell time [9]–[10]. The other one is based on carrier pulse width modulation. The balance of NP voltage can be realized by injecting zero-sequence voltage into the modulation voltages [11]–[13]. However, those strategies cannot fully eliminate the low-frequency fluctuation of NP voltage. To solve this problem, a strategy named two modified modulation algorithm has been proposed in [14]–[15]. Low-frequency fluctuation can be fully eliminated while it will also increase the switching frequency and harmonic component.

The strategies introduced above cannot be used in three-phase four-wire system because of the additional fourth wire. There are also some solutions proposed to control the NP voltage of three-phase four-wire NPC inverter. In [16]–[18], the zero-sequence voltage/current injection method based on carrier-based modulation is proposed to control the NP voltage. Although it can balance the NP voltage, it cannot reduce the amplitude of NP voltage fluctuation, and what's worse, it changes the output voltage of each phase. In [19]–[21], the control methods based on vectors selection in α - β - o coordinates and a - b - c coordinates are proposed. However, this method is complex and not easy for the digital implementation.

In this paper, based on the fluctuation mechanism of NP voltage in three-phase four-wire three-level NPC inverter, a new control strategy based on the disassembly of zero level is proposed. The validity of the strategy is verified through the simulation and experiments.

II. PRINCIPLE ANALYSIS OF THE NEUTRAL-POINT VOLTAGE FLUCTUATION

The three-phase four-wire three-level NPC inverter is presented in Fig. 1, where V_{dc} is the DC-bus voltage. Phase j ($j = a, b, c$) outputs P level when T_{j1} and T_{j2} are on and T_{j3} and T_{j4} are off, O level when T_{j2} and T_{j3} are on and T_{j1} and T_{j4} are off, and N level when T_{j3} and T_{j4} are on and T_{j1} and T_{j2} are off.

$V_{dc}/2$ is chosen as the base value to calculate the Per-Unit value of the three-phase output voltages, which are defined as follows:

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Fig. 1. Three-phase four-wire three-level NPC inverter.

$$\begin{cases} v_{ao} = M \cos(\theta) \\ v_{bo} = M \cos(\theta - 2\pi/3) \\ v_{co} = M \cos(\theta + 2\pi/3) \end{cases} \quad (1)$$

Where M is the modulation ratio ($0 \leq M \leq 1$).

Different from the three-wire topology, the neutral wire in four-wire structure is connected directly to the neutral-point of the DC bus. As a result, the three-phase four-wire three-level NPC inverter can be regarded as the combination of three single-phase inverters. It can be analyzed that when phase j outputs O level, the phase current i_j will flow through D_{j5} and T_{j2} or T_{j3} and D_{j6} , and return to or from the neutral point of the DC-bus capacitors through the neutral wire. The NP current i_o will not be influenced in this case. When phase j outputs P level, i_j will flow through the neutral wire and DC-bus capacitors. Thus, it will have an influence on i_o . Similarly, when phase j outputs N level, i_j will change i_o . Thus, it can be drawn that when one of the three phases outputs P or N level, i_o will be changed and lead to the drift of NP voltage. For convenience, define the variable S_{jo} that indicate the state of inverter output as follows:

$$S_{jo} = \begin{cases} 1, & \text{when outputs } O \text{ level} \\ 0, & \text{when outputs } P \text{ or } N \text{ level} \end{cases} \quad (2)$$

And then, the instantaneous value of the neutral current i_o shown in Fig. 1 can be achieved:

$$i_o = S_{ao} \cdot i_a + S_{bo} \cdot i_b + S_{co} \cdot i_c - (i_a + i_b + i_c) \quad (3)$$

When the switching frequency is high enough, it can be regarded that the current remains unchanged during every switching period. The average current can be given according to Fig. 1. according to the Kirchhoff's law:

$$\begin{aligned} \bar{i}_o &= d_{ao} \cdot i_a + d_{bo} \cdot i_b + d_{co} \cdot i_c - i_a - i_b - i_c \\ &= -i_a \cdot |v_{ao}| - i_b \cdot |v_{bo}| - i_c \cdot |v_{co}| \\ &= - \sum_{j=a,b,c} i_j \cdot |v_{jo}| \end{aligned} \quad (4)$$

Where d_{jo} is the duty ratio of O level in one switching period.

i_j is the phase current. The relationship between d_{jo} and v_{jo} is as follows [22]:

$$d_{jo} = 1 - |v_{jo}| \quad (5)$$

It can be found that the three-wire and four-wire topology share the same average neutral-point current expression, as is shown in (4) [11]. However, the principles of NP voltage imbalance between these two structures are different.

Based on the discussion above, the control of NP voltage can be converted to the control of NP current i_o . Thus, as long as the NP current i_o can be kept to zero through a certain control strategy, the NP voltage can keep balanced.

III. THE NEUTRAL-POINT VOLTAGE CONTROL STRATEGY BASED ON THE DISASSEMBLY OF ZERO LEVEL

The purpose of NP voltage control is to compensate the voltage offset between the upper and lower capacitors. This voltage offset consists of two parts, one is the voltage offset at the beginning of each switching period, and the other is the voltage offset during this switching period, which needs to be predicted.

A. Principle of O Level Disassembly

It can be seen from (4) that the NP current i_o is related to the output voltage and current of each phase. In [14], the author proposes a strategy to balance the NP voltage for the three-wire NPC inverter. It keeps the average NP current to zero during each switching period. Consequently, the average voltage of the DC-bus capacitors can be maintained constant. Although this strategy can only be applied to the three-wire NPC inverter, its idea can be migrated to the four-wire NPC inverter.

In a three-phase four-wire three-level NPC system, the NP voltage will be affected by phase current i_j only when phase j outputs P or N level. As a result, if the duty ratio of O level is disassembled to P and N level according to the NP voltage offset, the average NP current will be changed. The fluctuation of the NP voltage can be decreased or even eliminated through this process.

This can be described by Fig. 2. The original modulation sig-

Fig. 2. Modulation based on disassembly of O level.

Fig. 3. Waveforms of modulation and carrier signals.

nal v_j is disassembled to v_{jp} and v_{jn} as follows:

$$v_j = v_{jp} + v_{jn} \quad (j = a, b, c) \quad (6)$$

The modulation principle is shown in (7):

$$V_j = \begin{cases} P, & v_{jp} > v_{carrier}^p \text{ \& \& } v_{jn} > v_{carrier}^n \\ O, & v_{jp} < v_{carrier}^p \text{ \& \& } v_{jn} > v_{carrier}^n \\ N, & v_{jp} < v_{carrier}^p \text{ \& \& } v_{jn} < v_{carrier}^n \end{cases} \quad (7)$$

As is shown in Fig. 2, the output pulse ① is transferred to ② in this method. The O level has been disassembled to P and N level, so that the disassembly of O level can be achieved.

Actually, the phase disposition (PD) SPWM in [23] can be regarded as a kind of two modified modulation signals to some extent. In Fig. 3, the modulation signal of the PD-SPWM can be divided into the red (upper) and blue (lower) signals. Define the upper and lower signals as v_{jp} and v_{jn} . It can be found that they follow the rule given in (7), and also satisfy $v_{jp} \geq 0$, $v_{jn} \leq 0$ and $v_{jn} + 1 \geq v_{jp}$.

B. The Proposed Neutral-Point Control Strategy

Define V_{C1_mea} , V_{C2_mea} as the initial voltage of the upper and lower capacitors. Assume $\bar{i}_{C1}$, $\bar{i}_{C2}$ are the average currents that flow through the upper and lower capacitors respectively during one switching period. The NP voltage offset between the upper and lower capacitors during one switching period can be ex-

pressed as follows:

$$\begin{aligned} \Delta V_{dc_pre} &= \frac{T_s}{C} (\bar{i}_{C1} - \bar{i}_{C2}) = \frac{T_s}{C} \bar{i}_o \\ &= -\frac{T_s}{C} (i_a |v_a| + i_b |v_b| + i_c |v_c|) \end{aligned} \quad (8)$$

Where C is the capacitance value of each DC capacitor. The total offset value of the NP voltage difference is:

$$\Delta V_{dc} = \Delta V_{dc_pre} + V_{C1_mea} - V_{C2_mea} \quad (9)$$

So, the NP voltage offset needed to compensate will be:

$$\Delta V_{dc_com} = -\Delta V_{dc} \quad (10)$$

In order to minimize the switching loss, only one phase will be selected to disassemble its O level. The time needed to be disassembled is obtained as:

$$\Delta t_{dis_j} = -C \cdot \Delta V_{dc_com} / i_j \quad (j = a, b, c) \quad (11)$$

Δt_{dis_j} is theoretical disassembly time of phase j . It can be positive or negative. Only a phase with positive Δt_{dis_j} can be chosen to disassemble its O level. Also, only when Δt_{dis_j} is smaller than the O level time of phase j , the NP voltage offset can be fully compensated. As a result, proper phase should be chosen to compensate the NP voltage offset.

According to the analysis above, a variable indicating the neutral-point control margin ($NPCM$) is defined as follows:

$$NPCM_j = -\text{sign}(\Delta V_{dc_com}) \cdot [1 - |v_j|] \cdot i_j \quad (j = a, b, c) \quad (12)$$

$NPCM$ is related to the phase current, initial duty ratio of O level and the polarity of the compensation voltage. It represents the ability to compensate the offset. If $NPCM_j$ is positive, the NP voltage offset can be suppressed through disassembling O level of phase j . Moreover, the greater the $NPCM_j$ is, the more voltage offset it can be compensated. In order to select the proposer phase to compensate the NP voltage offset, the following cases are discussed:

- 1) If $NPCM$ of all the three phases are smaller than zero. The NP voltage offset cannot be compensated and no phases need to be disassembled in this case.
- 2) If any of the three $NPCM$ are greater than zero, phase with the largest $NPCM$ will be selected to disassemble the O level.

Assume phase j is selected, then the practical disassembling time $\Delta t'_{dis_j}$ can be obtained by the following discussion:

- 1) If the theoretical disassembling time Δt_{dis_j} is smaller than the O level time of phase j , the practical disassembling time is equal to the theoretical disassembling time:

$$\Delta t'_{dis_j} = \Delta t_{dis_j} \quad \left(\Delta t_{dis_j} < (1 - |v_j|) \cdot T_s \right) \quad (13)$$

- 2) If the theoretical disassembling time Δt_{dis_j} is larger than the O level time of phase j , all the O level needs to be dis-

TABLE I
SIMULATION AND EXPERIMENT PARAMETERS

Item	Parameter	Item	Parameter
DC-bus voltage	$V_{dc} = 540 \text{ V}$	Symmetrical reference voltages	$\begin{cases} v_a = 0.5 \sin \theta \\ v_b = 0.5 \sin(\theta - 2\pi/3) \\ v_c = 0.5 \sin(\theta + 2\pi/3) \end{cases}$
Upper/lower capacitor	$C_1 = C_2 = 1000 \mu\text{F}$	Asymmetrical reference voltages	$\begin{cases} v_a = 0.5 \sin \theta \\ v_b = 0.5 \sin(\theta - 2\pi/3) \\ v_c = 1.0 \sin(\theta + 2\pi/3) \end{cases}$
Output frequency	50 Hz	Balanced load:	$R_a = R_b = R_c = 12 \Omega$
Switching frequency	4 kHz	Unbalanced load:	$R_a = R_b = 12 \Omega, R_c = 24 \Omega$
LC filter	$L = 5 \text{ mH}, C = 20 \mu\text{F}$	Resistive load

Fig. 6. Example of output waveforms by 3-D SVM strategy.

the sub-space needs to be extended along the direction of axis a . As a result, the sub-space is extended to the cuboid A~L, and V_{ref} is located in the tetrahedron ABDJ. The pulse sequence is as shown in Fig. 6(b). Similarly, other axis can be analyzed from the way mentioned above.

It can be seen from Fig. 6 that the duty ratio of O level is fully and equally disassembled to P and N level for the phase selected for sub-space extension. Actually, it can be considered that 3D-SVM is a special case of the proposed method. However, the O level can only be fully disassembled to P and N level in the 3-D SVM method, and it cannot be quantitative. What's more, under some conditions, 3-D SVM would disassemble two phases in one switching period to balance the DC side. This would increase the switching loss a lot. The control strategy proposed in this paper solves the defect of 3-D SVM: it can compensate the offset of NP voltage accurately and what's more, quantitatively.

V. SIMULATION AND EXPERIMENTAL RESULTS

To validate the proposed NP voltage control strategy and compare its NP voltage control performance with the 3-D SVM method, simulation and experiments are carried out in this section. The system parameters are shown in TABLE I. Fig. 7 and Fig. 8 present the simulation and experimental results respectively under the balanced load and symmetrical three-phase reference voltages. Fig. 9 and Fig. 10 present the simulation and experimental results respectively under the unbalanced load and symmetrical three-phase reference voltages. Fig. 11 and Fig. 12 present the simulation and experimental results respectively under the unbalanced load and asymmetrical three-phase reference voltages. It can be seen that the NP voltage fluctuation is suppressed under all the three conditions. Moreover, the proposed strategy has a better control performance over the 3-D SVM method.

The FFT analysis for current of phase a under the three conditions are shown in Fig. 13. It can be seen that the THD is a little worse when adopting the proposed strategy. It is mainly because the switching frequency is higher than before and there are more low-order harmonics in the output current.

In practical applications, the nominal capacitance of capacitor is different from its actual value. Usually, for a capacitor with accuracy of "K", there will be a $\pm 10\%$ error. In order to find out the impact of accuracy of capacitor value on the proposed control performance, simulation is taken below under all the three conditions mentioned in TABLE I. For each figure, the capacitance is 900 μF in the upper one and 1100 μF in the lower one.

Compared Fig. 14 with Fig. 7(c), Fig. 9(c), Fig. 11(c), it can be found that the accuracy of capacitors do not have an obvious impact on the proposed strategy. The offset of NP voltage is compensated and the ripple is eliminated to a certain extent. However, when the actual capacitance is bigger than its nominal value, the control effect is a little better than the other condition.

What's more, the dynamic performance of the proposed strategy has been verified under sudden change of phase currents. Simulations have been carried out under two circumstances: (a) initially, $R_a = R_b = R_c = 12 \Omega$, and changes to $R_a = R_b = R_c =$

Fig. 7. Simulation results under the balanced load and symmetrical three-phase reference voltages.

Fig. 8. Experimental results under the balanced load and symmetrical three-phase reference voltages.

Fig. 9. Simulation results under the unbalanced load and symmetrical three-phase reference voltages.

Fig. 10. Experimental results under the unbalanced load and symmetrical three-phase reference voltages.

Fig. 11. Simulation results under the unbalanced load and asymmetrical three-phase reference voltages.

Fig. 12. Experimental results under the unbalanced load and asymmetrical three-phase reference voltages.

Fig. 13. FFT analysis results of output current of phase a: (a) and (d) are under the balanced load and symmetrical three-phase reference voltages. (b) and (e) are under the unbalanced load and symmetrical three-phase reference voltages. (c) and (f) are under the unbalanced load and asymmetrical three-phase reference voltages. (a), (b) and (c) show the results without NP voltage control. (d), (e) and (f) show the results with proposed control strategy.

Fig. 14. Simulation results for testing the impact of capacitor accuracy on proposed control strategy: (a) Balanced load and symmetrical reference voltage. (b) Unbalanced load and symmetrical reference voltage. (c) Unbalanced load and asymmetrical reference voltage.

24 Ω when $t = 0.98$ s; (b) initially, $R_a = 24 \Omega$, $R_b = R_c = 12 \Omega$, and changes to $R_a = R_b = R_c = 12 \Omega$ when $t = 0.98$ s. The simulation results are shown in Fig.15. The images from top to bottom is v_{ao} , i_{abc} , and ΔV_{dc} . It can be seen that the transitional process of NP voltage is very short, and the NP voltage ripple is well controlled under the new steady state. The proposed strategy has a good dynamic performance.

The power losses of the proposed strategy are analyzed in the following part. Power device used in this study is the F3L75R07W2E3_B11 from INFINEON, rated at 650 V, 75 A. The power losses of the converter can be classified into two parts: conduction and switching losses from the IGBT and its freewheeling diodes. Calculation method adopted in this paper is similar to the one adopted in [24]. The threshold voltage and on-state resistance of IGBT and diode are calculated based on

the V_{CE} versus I_C and V_F versus I_F figures provided in the technical information book of the IGBT modules. Results are given in TABLE II. In this analysis, the gate voltage is assumed to be 15 V which is a typical one and the junction temperature is 150 $^{\circ}\text{C}$ which is the worst case.

Then the conduction losses of the power devices can be approximated as:

$$P_{T_conduct} = \frac{1}{T} \int_0^T (V_T + i_F R_T) i_F dt \quad (19)$$

$$P_{D_conduct} = \frac{1}{T} \int_0^T (V_D + i_F R_D) i_F dt \quad (20)$$

where $P_{T_conduct}$ and $P_{D_conduct}$ is the conduction losses of transistor

Fig. 15. Simulation results for testing the dynamic performance of the proposed control strategy: (a) $R_a = R_b = R_c = 12 \Omega$, changes to $R_a = R_b = R_c = 24 \Omega$. (b) $R_a = 24 \Omega$, $R_b = R_c = 12 \Omega$, changes to $R_a = R_b = R_c = 12 \Omega$.

TABLE II

PARAMETERS OF THE IGBT FOR CALCULATION OF CONDUCTION LOSSES

Parameters	Value
V_T IGBT threshold voltage	0.42 V
R_T IGBT on-state resistance	15.3 mΩ
V_D Diode threshold voltage	1.45 V
R_D Diode on-state resistance	8.53 mΩ

and diode, respectively. T is the period of fundamental frequency.

To calculate the switching losses, Matlab curve fitting tool is adopted to obtain the Energy curves provided in the datasheet. E_{on} and E_{off} are the energies dissipation during the turn-on and turn-off process of the transistor. E_{rec} is the energy dissipation during the turn-off process of the diode. The energy dissipation in the diode during the turn-on process is very small and is neglected. The estimated curves are shown in TABLE III.

Thus, the switching losses can be calculated as:

$$P_{T_switching} = \frac{1}{T} \sum_{j=1}^n [E_{on}(i_F, v) + E_{off}(i_F, v)] \quad (21)$$

$$P_{D_switching} = \frac{1}{T} \sum_{j=1}^n [E_{rec}(i_F, v)] \quad (22)$$

After calculation, the total losses of the converter are shown in TABLE IV. It can be seen that the proposed algorithm will increase the switching losses, but not too much. Meanwhile, the conduction loss has decreased.

VI. ANALYSIS OF NEUTRAL-POINT VOLTAGE FLUCTUATION

It can be seen from the simulation and experimental re-

TABLE III
ENERGY DISSIPATION CURVES

Energy	Expression
E_{on} (mJ)	$\frac{V_{CE}}{300} (0.0075 I_C + 0.1625)$
E_{off} (mJ)	$\frac{V_{CE}}{300} (0.0275 I_C + 0.3375)$
E_{rec} (mJ)	$\frac{V_{CE}}{300} \left(5.686 \times 10^{-7} I_C^3 - 0.0001681 I_C^2 + \right)$ $0.02486 I_C + 0.5779$

TABLE IV
SIMULATION OF POWER LOSSES UNDER DIFFERENT CONDITIONS

Test Condition	Proposed Method (Conduction/Switching)	Without NP Control (Conduction/Switching)
Balanced load, Symmetrical voltage	15.2025/0.6258 W	18.2217/0.1128 W
Unbalanced load, Symmetrical voltage	16.6818/0.6045 W	18.4419/0.1128 W
Unbalanced load, Asymmetrical voltage	15.1383/0.6249 W	17.8656/0.1131 W

sults that there are some uncontrollable regions of NP voltage when the inverter connects to an unbalanced load. Actually, the proposed strategy suppresses the offset of NP voltage by controlling the NP current to zero. NP current i_o is given in (4) when none of the three phases are disassembled. When phase a , b and c are selected separately to fully disassemble its O level, the NP current can be obtained in (23).

In a three-phase four-wire three-level NPC system, the offset of NP voltage can be fully compensated only when the NP current can keep to zero in a switching period. If the polarities of i_o and $i_{o(j)}$ are opposite, NP current can keep to zero by disassembling O level of phase j , that is to say, the offset of NP voltage can be fully compensated.

$$\begin{aligned} i_{o(a)} &= -i_a - i_b \cdot |v_b| - i_c \cdot |v_c| \\ i_{o(b)} &= -i_b - i_a \cdot |v_a| - i_c \cdot |v_c| \\ i_{o(c)} &= -i_c - i_a \cdot |v_a| - i_b \cdot |v_b| \end{aligned} \quad (23)$$

Consequently, in order to fully compensated the NP voltage, it is required that there exists at least one phase, which satisfies:

$$i_{o(j)} \cdot i_o < 0 \quad (24)$$

Fig. 16 shows the NP current $i_{o(j)}$, i_o and the NP voltage differential under the three operation conditions. It can be seen from the Fig. 16(a) that (20) is satisfied when the inverter is under the condition of balanced load and symmetrical three-phase reference voltages. Thus, it does not have the uncontrollable region. While in Fig. 16(b) and Fig. 16(c), Fig. (20) is not established in the shadow region, where the NP current cannot be

Fig. 16. Analysis of NP current and voltage fluctuation. (a) is under the balanced load and symmetrical three-phase reference voltages. (b) is under the unbalanced load and symmetrical three-phase reference voltages. (c) is under the unbalanced load and asymmetrical three-phase reference voltages.

controlled to zero. The uncontrollable region is larger when the inverter is under the unbalanced load and asymmetrical three-phase reference voltages.

VII. CONCLUSION

A novel neutral-point voltage control strategy for a three-phase four-wire three-level NPC inverter is proposed in this paper. Proper phase is selected to disassemble the zero level and suppress the offset of NP voltage. Compared with the 3-D SVM, it can disassemble the zero level quantitatively and compensate the drift of NP voltage accurately. The offset of NP voltage cannot be fully compensated. However, it improves the stability of NP voltage without increasing too much switching frequency. The validity of this strategy is verified by simulation and experiments.

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