MODEL REDUCTION OF CFD SIMULATION OF INTEGRATED CIRCUIT COOLING OF AN ELECTRONICS PACKAGING VIA KRYLOV SUBSPACE SYSTEM

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ABSTRACT

The computational modeling and analysis of dense electronic circuits involve the numerical solution of large-scale or very large scale or sparse, in general leads to a nonlinear system of differential-algebraic equations. Frequently, the size of these systems can be reduced model, considerably by replacing the equations corresponding to linear subcircuits by approximate models of much smaller state-space dimension. In this paper, we describe the use of Krylov-subspace methods for generating such reduced-order models of linear subcircuits.

KEYWORDS: Dense Electronic Circuits, Smaller State & Linear Sub Circuits

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INTRODUCTION

The increasing complexity and size of today's integrated circuit (IC) designs and the constant development of processing technologies led to an increase in the fabrication costs and development and modeling time of such designs. In order to minimize the growing costs and improve the accuracy and reliability verification of each project before fabrication becomes imperative, so that fabricated circuits function correctly on "first silicon". As circuits become more complex and large, design techniques happen to be more elaborate and innovative in order to fully exploit the available space. Also, the continuing trend for increasing speeds of operation makes it impossible to discount previously ignored the effects of the interaction between circuits and their surrounding environment. Therefore, it becomes necessary that accurate circuit simulation methods be applied instead of other more intuitive, but less detailed approaches to verification, such as timing simulation or functional simulation. Parent and periinen [1] studied in the novel model-order reduction (MOR) in order to create fast-running, nonlinear, multiphysics models. From the study, it was concluded that a multi-physics reference model not only simplifies the creation of the ROM, but also helps the user to make educated choices if and how a particular nonlinearity needs to be included. Benion and Chen [2] investigated on the model order reduction (MOR) techniques that are used in coupling with finite element methods in order to generate computationally efficient methods for multiphysics MEMS simulation problems. Tamara *et al* [3] presented a methodology to apply the mathematical models for model order reduction (MOR) to electro-thermal MEMS models. The mainly focused to estimate the error between the original and the reduced models. For that, they suggested three heuristic

strategies for error estimation and concluded that the convergence of relative error and sequential model order reduction can be recommended for practical use. David Binion and Xiaolin Chen [4] investigated on the Arnoldi Model Order Reduction to develop the computational efficiency for using the MEMS simulations. Using this Arnoldi, a Krylov subspace was extracted in order to reduce the model size. Binion and Chen [5] investigated on Model order reduction (MOR) study to diminish the problem size for a multifaceted dynamic system. For the comparison sake, the results of the full-scale model were also performed using FEA program ANSYS. It was concluded that the computational time of MOR was drastically reduced when compared to the full-scale solution time, with only a minute relative error ranging from 1.1% to 4.5% for all the positions. Bianet *al* [6] investigated on the model order reduction (MOR) techniques based on Structure Preserving Reduced-order Interconnect Macro modeling (SPRIM) method, in order to generate the computationally competent solutions for multi-phase MEMS simulation. It was observed that the SPRIM efficiency development was slower than PRIM model, but this model experiences a less relative error of 2.2%. Guan *et al* [7] investigated an effective increment-dimensional precise integration method (PIM) along with the MOR technique. Krylov subspace is used to solve the large-scale nonlinear problems. Lastly, the precise integration method is used to solve the fast transient response of compact order model. Bianet *al* [8] investigated on the stochastic model reduction method with indiscriminate input conditions in order to smooth the progress of fast time and regularly domain analyses; this method mostly makes use of polynomial chaos expansions for the arbitrary input variables of a finite element model and then it uses its transformation matrix to reduce the model; this method is totally independent of the MOR algorithm.

Conventional circuit simulators, developed during the 1990's are capable of simulating virtually any circuit given enough resources in terms of time and computational power. However, full verification of the functionality of a system must not only be reliable, but also fast enough to provide results in an acceptable time interval. This implies that the computational resources that must be allocated for the simulation task also increase dramatically and in some cases, the amount of resources needed becomes inadmissibly expensive.

One way to address this problem is through the usage of faster computer hardware. While this may be as simple as using a faster mainframe computer or a new generation workstation, it can also be viewed in the context of parallel computation. Parallel circuit simulation has been successfully applied to specific classes of circuits with very encouraging results. With some degree of confidence, it is believed that this is true whenever the sheer size of the circuit or the nature of the computation it performs make it amenable to parallel simulation. However, it is also recognized that for the most part, the circuit simulation paradigm does not contain enough structure for efficient parallelization. In fact, in many cases the nature of the difficulty may not be related to the size of the circuit itself, but merely to the length of the simulation interval, or to the complexity of the models of the elements involved. In such cases, it is believed that improving the efficiency of the simulation process can only be accomplished by devising specific algorithms that exploit the characteristic features of the particular problem to be solved.

Transient circuit simulation involves forming the system of nonlinear ordinary differential equations (ODE) that describes the dynamics of a circuit, and solving them numerically. The typical approach is to first discretize the set of ODE's in time with an integration method. As stiff ODE systems require the use of implicit integration schemes, the time discretization generates a sequence of nonlinear algebraic problems which are solved with an iterative method. The sequence of linear algebraic systems generated at each iteration of the nonlinear solution method, then solved by means of Gaussian elimination or possibly some iterative linear solution algorithm.

Two possible computational bottlenecks are usually identified in standard circuit simulation. One is the function evaluations necessary to compute the components of the Jacobian and right hand side vector used for iteration. These function evaluations correspond to the computation of the device's constitutive relations and their derivatives. If the circuit is very large, then eventually the linear solution task will dominate the total complexity. On the other-hand, if the circuit is small or only moderately large, then the device evaluation task will in general dominates. Nevertheless, one should be very careful when weighing the costs associated with the circuit simulation process using complexity issues alone as this can sometimes lead to erroneous conclusions. In fact, even assuming the number of circuit nodes to be small, the real cost of each Newton iteration might still be extremely large if the evaluation of some or all of the devices is computationally very expensive.

A simple example of this situation is the case of clocked analog circuits such as power converters or phase-locked loops. It seems, therefore hopeless to expect that standard circuit simulation algorithms be able to handle every conceivable scenario with acceptable efficiency. For these reasons, a pertinent question is whether it is possible to achieve efficient simulation of certain classes of circuits by using algorithms or techniques specifically tuned to exploit the characteristic features of the particular problem to be solved and make them more tractable.

Model Order Reduction is one possible answer to our problem. Model order reduction is a process by which, given a complex dynamic system, one obtains a simpler model that approximates the full system in some adequate way. The main reasons for obtaining lower-order models are twofold: to facilitate an understanding of the system, or to reduce computational efforts in the simulation process. We will study some theoretical and practical aspects of model order reduction techniques for use in the context of circuit simulation. Two different types of approaches will be considered. One is to look at the model order reduction technique as a way to simplify the complexity of the computations in an otherwise computationally expensive problem.

The other approach taken is to consider model order reduction as a macro-modeling technique applied in this case to the modeling of frequency-dependent interconnect and packaging structures.

METHODOLOGY

A measurement-based reduced-order model of transient air temperature is developed with time as the independent variable and spatial location as the parametric variable. The functional form of the temperature response surface is: $T = f(t; x, y, z)$

The measurement-based reduced-order air temperature model is developed via a KSS based statistical algorithm. Figure 1 shows the proposed Krylov-based algorithm.

Figure 1: Krylov Based Algorithm

Governing Equations and Numerical Scheme

The governing equations for this project are the three-dimensional continuity, Navier-Stokes for momentum, energy, and scalar transport equations for steady-state flow, and can be written (generally) as follows:

Continuity Equation

$$\frac{\partial(\rho u_i)}{\partial x_i} = 0. \quad (1)$$

Momentum Equation

$$\frac{\partial}{\partial x_i}(\rho u_i u_j) = \frac{\partial}{\partial x_i} \left(\mu \frac{\partial u_j}{\partial x_i} \right) - \frac{\partial p}{\partial x_j}. \quad (2)$$

Energy Equation

$$\frac{\partial}{\partial x_i}(\rho u_i T) = \frac{\partial}{\partial x_i} \left(\frac{k}{C_p} \frac{\partial u_j}{\partial x_i} \right). \quad (3)$$

General Transport Equation (For Scalars)

$$\frac{\partial(\rho u_i \phi)}{\partial x_i} = \frac{\partial}{\partial x_i} \left[\Gamma_\phi \frac{\partial \phi}{\partial x_i} \right] + S_\phi \quad (4)$$

It is solved on a staggered grid using solvers for laminar and turbulent flow, with the latter solution solved using the Reynolds Averaged Navier-Stokes equations (RANS) with both k-epsilon and SST k-omega turbulence models. To ensure coupling between velocity and pressure, the SIMPLE algorithm is used.

CFD Simulation

The ANSYS Icepack software among various CFD tool specifically tailored for use in the electronic industry to perform the board and system level thermal analysis. In icepack, a variety of thermal limitation source elements are available, including heat dissipation, fixed temperature sources or heat flux sources. Typically controllers in the vehicle are housed in a sealed case, and rely solely on free convection and radiation for cooling. The heat flow path in the controller is

a series of conduction, convection and radiation path. Much of the generated in an integrated circuit chip is first conducted into a printed circuit board. From here, heat is transported through the case wall and finally removed to the environment by free convection. Figure 2 shows the detail model of ECU with different component on the PCB. Figure 3 shows the whole solution domain with open faces.

Figure 2: ECU of Different Components

Figure 3: Thermal Models for ECU

RESULTS AND DISCUSSIONS

A three-dimensional model is developed to investigate flow and conjugate heat transfer in the microchannel based heat sink for electronic packaging applications. A series of numerical calculations have been conducted by FLUENT and the results are presented in order to show the effects of temperature distribution, heat flux distribution as well as the average heat transfer coefficient in the microchannel heat sinks.

The average of the area of microchannel has been taken for plotting the different graphs, i.e average of the total number of nodes along the perimeter of the inner wall. To better understand the fluid flow and heat transfer characteristics in silicon-based microchannel heat sinks designed for applications in electronic cooling. These non-circular channels and silicon base, microchannel heat sinks combine the attributes of high material compatibility, high surface area per unit volume ratios and large potential heat transfer performance, with highly sophisticated and economic fabrication processes. These advantages make this silicon based microchannel heat sinks extremely attractive for a wide variety of commercial applications. Figure 4 shows the iterations of the CFD models.

Graph 1: Different CFD Values for 150 Iterations

Figure 5 and 6 shows the heat transfer coefficient and temperature distribution on the board respectively. The highest temperature is obtained at the channel outlet in case of 10 kPa at constant heat flux of 90 W/cm^2 , because of the low velocity of fluid flow. At heat flux $q'' = 150 \text{ W/cm}^2$ the highest temperature is obtained at the channel outlet at a constant pressure drop of 50 kPa. As the heat flux increases, the outlet temperature goes on increasing because the fluid gets heated up more and more due to convective heat transfer. The maximum temperature of fluid rises in case of 10 kPa due to low liquid velocity and Minimum temperature raises in case of 50 kPa due to high liquid velocity inside the microchannel at a constant inlet temperature 20°C .

Figure 4: Heat Transfer Coefficient of the Board

The theoretical analysis performed, provides a fundamental understanding of the combined flow and conjugate convection-conduction heat transfer in the three-dimensional microchannel heat sink. The model formulation is general and only a few simplifying assumptions are made. Therefore, the results of the analysis, as well as the conclusions, can be considered as quite general and applicable to any three-dimensional conjugate heat transfer problem.

The maximum temperature is located at a heated base surface of the heat sink, below the channel outlet. This is due to the low velocity of the fluid flow and resulting the high concentration of heat flux.

Figure 5: Temperature Distribution of the Board at Different Locations

Table 1: Temperature Difference of the Board at Different Dimensions

Chip dimension	Correlation Coefficient	Temperature Difference
(450,1250,220)	0.9968	1.89
(350,1250,220)	0.9862	1.23
(250,1250,220)	0.9972	1.65
(450,1050,220)	0.9825	1.03
(450,950,220)	0.9902	1.06
(450,750,220)	0.9802	1.23
(450,1250,220)	0.9817	1.42
(450,1250,180)	0.9924	1.24
(450,1250,150)	0.9943	1.16

Table.1 shows the temperature difference and its correlation coefficient of the board at different chip dimensions. A three-dimensional rectangular microchannel model consists of a 10 mm long silicon substrate with 57 μm wide and 180 μm deep developed using incompressible laminar Navier-Stokes equations of motion are capable of predicting correctly the flow and conjugate heat transfer in the microchannel heat sink. It has been validated using numerical data reported in the literature and a good agreement has been found between the model prediction and measurements.

CONCLUSIONS

The comparison of computational results obtained by the CFD method without model reduction and after implementing the model order reduction has been presented above. From the comparison, we can observe that the computational time by the CFD method of solving without implementing model order reduction has been much larger and more over the CPU utilization of the solution strategy has been significantly reduced with the implementation of order reduction technique. The computational recourse has been minimized to as minimum as of 54.6% to 8.2%. The minimum and maximum error percentage has been kept in the limits at 0.5% to 1% of the experimental values. The computational time has significantly been reduced to the minimum of 1.4% to a maximum of 30.5%.

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