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It also consists of two word lines namely word line (WL) and word line bar (WLB). It has bit lines namely bit line (B) and bit bar line (BB). B, BB, WL, WLB lines act as input to the circuit. The output is observed at Q and QB. The design specifications are shown in table 1.

Parameter	WL	WLB	B	BB
voltage 1 (volts)	0	1.8	0	1.8
voltage 2 (volts)	1.8	0	1.8	0
Period	90ns	90ns	100ns	100ns
Pulse Width	30ns	30ns	50ns	50ns

Table 1: Design Specifications of TG8T SRAM.

The schematic view of TG8T SRAM with above specifications is designed as shown in fig 2 in virtuoso.

Fig 2: Schematic view of TG8T SRAM using virtuoso.

B. Working of tg8t sram cell

The working of TG8T SRAM cell consists of two operations i.e. write and read operation. When we perform a write operation, both the bit lines are at opposite voltages which represent if bit line BL is at high then BLB is at low and vice versa (BL=1 and BLB=0 or BL=0 and BLB=1). When WL becomes high and also WLB=0 which enables NMOS and PMOS transistors M5 and M6 then data writes on the output nodes Q and QB of back-to-back connected inverters.

When the read operation is performed which is just opposite to the write operation, both the bit lines are at high voltages also behave as an output and WL is raised to high and WLB at 0. Since one of the output nodes (Q and QB) is at low then one of pre-charged bit lines start discharging and at that instant data is going to be read.

III. SIMULATION RESULTS

A. Output Graphs

The figure 3, 4 and 5 show the simulation graph of TG8T SRAM, delay and power. WL, WLB, B and BB are the input lines which mean word line, word line bar, bit line and bit line bar respectively. Q and QB are the output lines.

Fig 3: Simulation Result of TG8T SRAM.

Fig 4: Delay of TG8T SRAM Cell.

Fig 5: Power of TG8T SRAM Cell.

B. Comparative Analysis

Here the delay and power outputs of 6T SRAM, 8T SRAM and TG8T SRAM are compared and tabulated as shown in table 2.

SRAM	DELAY(sec)	POWER (W)
6T SRAM	99.88 E-9	2.616 E-6
8T SRAM	-62.99 E-12	2.54 E-6
TG8T SRAM	-27.21 E-12	3.474 E-6

Table 2: Comparative Analysis.

The table 2 shows the comparison of 6T SRAM and 8T SRAM with TG8T SRAM. It is crystal clear that the delay of TG8T SRAM is very less compared to existing SRAMs which implies speed of proposed design is faster than others. The bit line leakage problems are also less.

The power of proposed designed is slightly higher than standard 6T SRAM which is the major drawback of this project. Since there is a possibility of changing threshold voltage of CMOS transistors, we can overcome the above drawback using SYNOPSIS tool.

IV. CONCLUSION

An 8T SRAM cell is designed using Transmission gate in 180nm CMOS technology and its parameters are compared with the existing SRAM cells. The proposed design has improved parameters with the benefit of high speed operation as delay is decreased by $9.99\text{E-}8$ leading to reduced leakage parameters. The results show major enhancement in the design parameters over standard 6T SRAM cell and 8T SRAM cell signifying its strength and functionality.

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