Design of Digital Filters for Multi-standard Transceivers

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Abstract: This paper addresses on three different architectures of digital decimation filter design of a multi-standard RF transceivers. Instead of using single stage decimation filter network, the filters are implemented in multiple stages using FPGA to optimize the area, delay and dynamic power consumption. The proposed decimation filter architectures reflect the considerable reduction in area and dynamic power consumption without degradation of performance. The filter coefficients are derived from MATLAB, the filter architectures are implemented and tested using Xilinx SPARTAN FPGA. First, the types of decimation filter architectures are tested and implemented using conventional binary number system. Then the two different encoding schemes i.e. Canonic Signed Digit (CSD) and Minimum Signed Digit (MSD) are used for filter coefficients and then the architecture performances are tested. The results of CSD and MSD based architectures show a considerable reduction in the area and power against the conventional number system based filter design implementation. The implementation results reflect that considerable reduction in area of 47.89% and dynamic power reduction of 28.64% are achieved using hybrid architecture.

Keywords: Digital Filter, Multi-rate Decimation Filter, FPGA, Hardware Reduction, Low Power Design.

1. Introduction

Radio Frequency (RF) communication transceivers emphasizes both higher integration to meet consumer demand of low-cost, low-power, less area personal communication devices and the ability to adapt to Multiple Communication Standards. Receiver architecture that performs channel select filtering based on-chip at baseband allows for the programmability necessary to adapt to Multiple Communication Standards[1]. In audio applications of wireless transceivers, the use of oversampling Sigma Delta Analog to Digital ($\Sigma\Delta$ -ADC) converter has become popular because of its improved performances [2]. The $\Sigma\Delta$ -ADC converter samples the input signal with rate much greater than Nyquist rate $2f_s$. The oversampling ratio of the $\Sigma\Delta$ -ADC is defined as $M = f_s/2f_s$, where f_s is the sampling rate of $\Sigma\Delta$ -ADC converter. Typical audio application consists of an oversampled $\Sigma\Delta$ -ADC followed by a decimation filter. The digital filter is used to perform filtering operation and sampling rate down conversion so as to extract the original signal bandwidth. A programmable low-pass decimation filter of a RF transceiver can select a desired channel in the presence of both strong adjacent channel interference and quantization noise from the digitizing process.

Several literatures deal with the design issues of decimation filters for wireless communication transceivers. In this paper, a cascade CIC-HB filter implementation of the decimation filter using Conventional and CSD based multipliers are addressed in detail. This paper is organized as follows: Section 2 describes the digital receiver architecture suitable for multi-standard operation. Section 3 deals with the concepts of decimation process. Section 4 presents the three different multistage decimation filter architectures and types of filters used for implementation of each stage. In Section 5 Canonical Signed Digit (CSD) and Minimum

Signed Digit (MSD) representation are explained in detail[3]. Section 6 provides the simulation results of the various types of decimation filter architectures. Finally Section 7 describes the conclusion.

2. Digital Receiver Architecture

This section deals with the digital receiver architecture, which emphasizes high integration and multi-standard capability. High integration can be achieved by utilizing a receiver architecture that performs base band channel select filtering on-chip. This enhances the programmability to different dynamic range, linearity and signal bandwidth so as to meet the requirements of multiple RF standards. Typical block diagram of a digital transceiver is shown in Figure 1. An overview of a digital receiver will readily confirm that its main task is to take a signal sampled at a high rate, down convert it and filter it-through low-pass filter and then decimate it and finally format it into one or more of several forms. After demodulation, this signal is converted back to analogy form and then applied to power amplifier and loudspeaker.

Figure 1. Architecture of Digital Transceiver

The input analogy signal is converted to digital form with the aid of the analogy to digital converter. A wide band, high dynamic range sigma-delta modulator can be used to digitize both the desired signal and potentially stronger adjacent channel interferences. Next, this signal is applied to a digital Mixer-the signal is applied to two Mixers driven by digital In-phase (I) and Quadrature (Q) components of a local oscillator signal which in turn is provided by a digital frequency synthesizer. In essence, the input signal is multiplied with the sine and also with the cosine output of the local oscillator. The output of the Mixer consists of sum and difference frequencies extending the way up in the sampled data spectrum. To remove the higher order components and to recover only the baseband signal, the signal is passed through a decimating low pass filter. This digital filter has the property of reducing the sample rate of the input signal by some factor (decimation factor), which can be programmed to be as low as 1 or as high as 16,384. As far as the demodulator function is concerned, it is best performed digitally in a DSP processor outside the digital receiver chip. Demodulator is followed by a D/A converter and speaker to complete the analogy between the analogy and digital receivers.

3. Decimation Process

To reconstruct a signal from its sample values, a band-limited signal only need to be sampled at a rate in excess of the Nyquist rate. Speech or low bandwidth signals may be sampled well above their Nyquist rate to bypass problems associated with the low rate analogy to digital(A/D) conversion noises.This is achieved using Sigma Delta A/D converter($\Sigma\Delta$ -ADCs) in the digital receivers. One of the key features of Sigma Delta A/D converter is that the modulator is over sampled compared to the expected output sample rate. A higher order decimation filter is used to convert the over sampled signal into usable baseband signal. The decimation process simply reduces the output sample rate while retaining the necessary information. It transforms the digitally modulated signal from short words occurring at high sampling rate to longer words at Nyquist rate. To extract the signal information, the signal must be first down-converted to base band. A multi-stage decimation filter is used to perform this function.

Due to over sampled $\Sigma\Delta$ - ADCs, only small fraction of the total noise power falls in the frequency band. The noise power outside the signal band can be greatly attenuated with a digital low pass Decimation filter following the $\Sigma\Delta$ - ADC. Decimation is often performed in several stages instead of a single stage. This leads to higher decimation factor in the first filter stage as compared with decimation filters of similar input and output data word lengths in the consecutive stages. However, the word length differs between the consecutive stages. This is especially important for $\Sigma\Delta$ ADCs, as the input to the decimator may be only one bit while the output precision can be, say, 16 bits or more. Multistage decimation filter architecture reduces the overall complexity in terms of area and power at each stage of filter design.

4. Multistage Decimation Filter Architectures

The sampling rate is down converted from the oversampled rate of sigma-delta modulator to a data rate that can be conveniently processed by existing DSP processors using decimation filters. The purpose of decimation filter is to remove all the out-of-band signals and noise and to reduce the sampling rate from oversampled frequency of the $\Sigma\Delta$ -ADC to Nyquist rate of the channel[5]. The decimation filter consists of a low-pass filter and a down-sampler. It is possible to perform noise removal and down conversion with a single FIR filter stage. The filter order N of FIR low-pass filter is given by eqn. (1), where D_∞ is a function of the required ripples δ_p and δ_s in the pass-band and stop-band respectively, F_s is the sampling frequency and Δf is the width of transition band.

$$N \approx D_\infty(\delta_p, \delta_s) (F_s / \Delta f) \quad (1)$$

As the $\Sigma\Delta$ - ADCs are oversampled, the transition band is small relative to the sampling frequency leading to excessively large filter orders and this leads to a lot of multiplication operations. The power consumption of the filter depends on the number of taps as well as the rate at which it operates. So computational complexity is high for single stage implementation of decimation filter and consumes more power. Implementing decimation filter in several stages reduces the total number of filter coefficients. This will result in less area and low power consumption. A multistage decimation filter system consists of a cascaded structure of several single stage decimation filter systems. The ' i^{th} ' stage of multistage system performs decimation by a factor of ' R_i ' such that the overall decimation factor ' R ' is given by the eqn. (2)

$$R = \prod_{i=1}^P R_i, \quad (2)$$

where ' P ' is the total number of stages of multistage decimation filters. The individual filter of each stage is designed within the frequency band of interest in order to prevent aliasing in the overall decimation process. The performance of a decimation filter depends on the filter architecture and the order of each stage of a multistage decimator. FIR filters are widely used in decimators because of its linear phase characteristics. Multistage decimation reduces the overall complexity of system by decomposing the decimation factor into several sub factors. Thus, each stage requires lower order filters.

FIR filter are used in down converters because some modulation schemes requires linear phase. In wireless communication devices, the battery life must be maximized. Therefore, high performance blocks with low power consumption and small area are required. The implementation of decimation filter for multiple standards on a single device is very demanding in terms of area and power. With an efficient decomposition of decimation factor considering common blocks between different communication standards, it is possible to have an efficient design. Thus, few different blocks could be implemented in a configurable fashion. Three different filter architectures used in this paper are described in the following sections in detail.

A. Architecture I

Decimation Filter with Conventional MAC Unit

In this architecture, decimation filter is implemented using two filter stages with overall decimation factor of 32. The decimation filter architecture consists of first stage representing High Order Decimation Filter (HDF) and second stage representing Corrector Finite Impulse Response (FIR) filter and implemented using conventional binary number system with conventional MAC unit as shown in figure 2.

Figure 2. Two Stage Decimation Filter with Conventional MAC Unit

A.1 Cascaded Integrator Comb(CIC) Filter

The first filter section is called the HDF and it is normally optimized to perform decimation by large factors. It implements a low pass filter function using only adders and delay elements instead of a large number of multiplier/accumulators that would be required using a standard FIR filter. An efficient architecture of HDF stage belongs to a class of multi-rate multiplier-less systems referred to as Cascade of Integrators-Comb (CIC) filters[4]. In fact, in its recursive form, the CIC filter is multiplier less and presents low complexity properties. The fifth order CIC filter structure is constructed using only integrators and differentiators as shown in figure 3. Blocks I represent the integrators, R represents the decimator and Represent the differentiators (comb). The CIC filter design approach consists of 5 stages of Integrator section followed by a 5 stages of differentiators. The cascaded structure of integrators and combs provides a better solution for low power CIC filters.

Figure 3. CIC Filter Structure

The integrator (I) and the comb filter (D) operations are performed using registers and adders only. Figure 4 shows the equivalent digital circuit representation of the integrator stages. Each accumulator is implemented as an adder followed by a register in the feed forward path. The integrator is clocked by the sample clock, CK_IN. The output of the Integrator section is latched on to the decimation register by CK_DEC. The output of the decimation register is passed to the Comb Filter Section. The Comb section consists of five cascaded comb filters. Each Comb filter calculates the difference between the current and previous integrator output. Each comb filter consists of a register which is clocked by CK_DEC followed by an subtracter where the subtracter calculates the difference between the input and output of the register. Figure 5 describes the equivalent digital circuit representation of the 5-stage comb filter.

Figure 4. Digital Circuit Implementation of 5-Stage Integrator

Figure 5. Digital Circuit Implementation Comb Filter Section

Figure 6. Corrector FIR Filter structure

A.2 Characteristics of CIC filter

The integrator section of CIC filter consists of N ideal digital integrator stages operating at high sampling rate, f_s . Each stage is implemented as a one-pole filter with a unity feedback coefficient. The system function for a single integrator is given by eqn. (3).

$$H_I(z) = 1/(1-z^{-1}) \quad (3)$$

The comb section operates at the low sampling rate f_s/R , where R is the integer rate change factor. This section consists of N comb stages with a differential delay of M samples per stage. The differential delay is a filter design parameter used to control the filter's frequency response. In practice, the differential delay is usually held at $M = 1$ or 2 . The system function for a single comb stage referenced to high sampling rate is denoted by eqn. (4).

$$H_C(z) = (1-z^{-RM}) \quad (4)$$

Where R - Decimation ratio

M - Differential delay

N - No. of stages

It follows from eqn. 3 and eqn. 4 that the system function for the composite N th order CIC filter referenced to the high sampling rate, f_s is denoted by eqn. 5 as

$$H(z) = H_I^N(z) * H_C^N(z) = (1 - z^{-RM})^N / (1 - z^{-1})^N \\ = \left[\sum z^{-k} \right]^N \quad (5)$$

where k ranges from 0 to $RM-1$

It is implicit from the last form of the system function that the CIC -HDF filter is functionally equivalent to a cascade of N uniform FIR filter stages[8].

A.3 Corrector FIR Filter

The second filter stage in the top level block diagram of architecture I is a corrector Finite Impulse Response (FIR) filter which performs the final shaping of the signal spectrum and suppresses the aliasing components in the transition band of the HDF. This enables the Decimation filter to implement filters with narrow pass bands and sharp transition bands. The Corrector FIR filter structure used for architecture I is shown in figure.6. The FIR is implemented in a transversal structure using a single multiplier/accumulator (MAC) and RAM for storage of data and filter coefficients. The corrector FIR is designed with the decimation factor of two. The 16-bit output of the HDF output register is written into the data RAM on the rising edge of CK_DEC . The Coefficient RAM stores the coefficients for the current FIR filter being implemented. The coefficients are loaded into the Coefficient RAM over the control bus.

B. Architecture II

Cascaded Multi-standard Decimation Chain

The decimation filter is a block that reduces the data rate from IF to base band domain. Different communication standards require large factor of decimation resulting in large orders of filter networks. Multistage decimation reduces the overall complexity of system, by decomposing the decimation factor in to several sub factors. FIR filter are used in down converters because some modulation schemes requires linear phase[10]. In wireless communication transceivers, the battery life must be maximized. Therefore, high performance blocks with low power consumption and small area are required. The implementation of decimation filter for each standard on a single device is very demanding in terms of overall area and power dissipation. However, with an efficient decomposition of decimation factor and considering common blocks between different communication standards, it is possible to have an efficient design of multi-standard transceivers. Thus, few different blocks could be implemented in a configurable fashion to meet the multi-standard filter circuits requirement.

B.1 Decimation Chain Structure

Figure 7 shows the Cascaded Multi-standard Decimation Chain architecture for two different standards with the decimation factors of 8 and 32. The aim of this architecture is to reduce multiplication operations. To reach this goal, multiplier-less comb filters are used for the first stage similar to architecture I[7]. On simulations, the last two stages of each standard cannot be comb filters, because they don't remove the in band noise level sufficiently. It was decided to use half band filters for the last two stages. They exhibited good results and excellent out-of-band signal attenuation. The proposed architecture II supports three comb filter stages and 4 stages of half band filters to meet multi-standard requirements. Since the first comb filter stage is used commonly for both the standards, this architecture considerably reduces the area and power of the multi-standard transceiver.

Figure 7. Cascaded Multi-standard Decimation Chain Architecture

B.2 CIC Filter Structure

The fifth order CIC filter structure resembles as that of figure 3 shown in architecture I but the implementation of CIC filter integrators and differentiators stages of architecture II differs from architecture I. Figure 8 shows the basic integrator stage of CIC filter used in this architecture in its Z transform and its equivalent digital circuit in HDL. Thus the single accumulator (Integrator) unit is implemented in HDL using 14-bit adder and a register by avoiding complex multiplexer stages, when compared with architecture I. In a similar fashion, the differentiator (Comb filter) stage of CIC filter in Z domain and its digital equivalent circuit are represented as shown in figure 9. Thus the comb stage is designed in HDL using a subtraction and a register networks. This architecture results in a considerable reduction in area and power, when compared to the first architecture. Simulation environment states that further reduction in area and power can be achieved by changing the encoding scheme of filter coefficients from conventional binary number system to Canonic Signed Digit (CSD) and Minimum Signed Digit (MSD) Number systems.

Figure 8. Accumulator in Z-transform and its Digital Circuit Implementation

Figure 9. Differentiator in Z-transform and its Digital Circuit Implementation

B.3 Half Band FIR Filter

The CIC filter is followed by an half band FIR filter for further down-sampling. The half band FIR filter is used instead of another CIC due to the fact that the pass band of CIC consists of distortions and the half band FIR can be designed in such way that its frequency response compensates for the distortions created by CIC stages. Since the down-sampling rate of half band filter is chosen to be 2, special type of symmetric coefficients type FIR filter can be used for the architecture II meaning that the coefficients of an odd N tap ($N-1$ order) half band FIR can be represented by $\text{Ceil} [(N-1)/4] + 1$ numbers[9]. The half band filter significantly reduces the hardware resources needed. The order of the half band filter used in this design is 14(15 taps) with the filter coefficients quantized for 8-bit precision.

C. Architecture III Hybrid Architecture

The cascaded decimation chain architecture supports multi-standard applications. One of the drawback of decimation chain architecture- Nevertheless, it turns out that this architecture doesn't take into consideration of the selected standard to be treated. If the transceiver is intended to receive one particular standard's signal, all filter networks involved in the architecture of second standard are active irrespective of chosen one. i.e. when a standard is being processed even those filters, which are not necessary for the channel selection of the standard are active. Therefore, to overcome this problem, it is proposed to add a power consumption controller that well-manages and supervises filters operations depending on the selected standard as shown in figure 10. Furthermore, in order to have a multi-standard architecture with a unique cascade of filters for the two standards, this architecture is realized by exploiting the similarities between the half-band filters. This process produces a multi-standard design capability to handle mutually different exclusive filters with efficient resource sharing. Thus the hybrid architecture guarantees the re-configurability of RF transceivers and further reduction in power consumption and in area of the receiver.

Figure 10. Hybrid Architecture

5. Co-efficient Realization using CSD and MSD Representations

The CSD representation is a radix-2 signed digit system with the digit set $(1, 0, _1)$. For any binary number, the CSD representation is unique and it satisfies the following two properties: first property is that the number of non zero digits are minimal and the second property is that

adjacent two digits can never be nonzero digits i.e. the product of adjacent two digits will always be zero. This representation is widely used in multiplier less implementations of filter design with respect to filter coefficients because it reduces the hardware requirements due to the minimum number of non-zero digits. On an average, the number of non-zero digits in CSD is reduced by 33%, when compared with the conventional binary number system. To obtain the CSD representation of a number, start processing its binary representation from the least significant digit to the most significant digit and replace repeatedly all the sequences found as 01...1 by a sequence 10...01 with same number of digits [6]. The conversion table shown in Table 5.1 is used to obtain the CSD number of a given binary number.

Table 5. CSD Conversion Table

Inputs			Outputs	
State	b_{i+1}	b_i	c_i	Next State
0	0	0	0	0
0	0	1	1	0
0	1	0	0	0
0	1	1	-1	1
1	0	0	1	0
1	0	1	0	1
1	1	0	-1	1
1	0	1	0	1

If the second property of CSD is relaxed, then it leads to MSD representation. In general, the MSD representation providing multiple representations yielding the same value is more flexible than the CSD representation. This redundancy can result in smaller hardware units than those generated from the CSD representation provided appropriate MSD representation is selected for each constant. Thus the MSD representation is a superset of CSD number system and it provides a number of forms. The MSD number system is appropriate in finding common sub expressions of multiple constants, in case proper MSD representation is selected for each constant to be synthesized. Since the MSD number system has an effect on the number of additions in the decomposed multiplication block and the number of common sub-expressions that can be eliminated, it has significant bearing on the reduction of area and power consumption. The advantage of using the MSD representation for a coefficient results from increasing the possibilities of sharing partial terms between coefficients.

6. Simulation Results

The decimation filter design specification is shown in Table 6.1. The input signal frequency is chosen as 64 MHz and the decimation factors are chosen to be 8 and 32 respectively for the multi-standard structures. The pass band of the filter circuit with the decimation factors of 8 and 32 will be 8 MHz and 2 MHz respectively. The pass band ripple and the stop attenuation are taken to be 0.001 and -60 dB. The filter circuit performance has been tested first using Matlab and the filter co-efficients are derived as per the given specifications of Table 6.1. For the implementation of decimation filter architectures in Spartan FPGA, the filter coefficients derived from Matlab are encoded in conventional binary number system, CSD and MSD representations. In all the architectures, the overall multistage filter networks are implemented on Xilinx Spartan FPGA. The area in terms of total gate count is analyzed for the architectures and the power analysis is carried out using the power estimating tool Xilinx Xpower Analyzer. Figure 11-12 describes the MATLAB outputs of a conventional decimation filter network. The coefficients derived from MATLAB are converted to CSD and MSD form and the performance of the decimation filter architectures are tested, implemented using SPARTAN FPGA. Table 6.2 shows the comparison results of decimation filter architectures in terms of total gate count, Number of slices, LUTs, IOBs, flip-flops and dynamic power consumption with respect to conventional, CSD and MSD number systems. Table 6.3 shows

the comparison results of delay and power delay products of all the three decimation filter architectures.

Table 6. Decimation Filter Specification

Specification Parameters	Architecture I	Architecture II
Decimation Factor	8	32
Pass Band	0 to 8MHz	0 to 2MHz
Pass Band Ripple	0.001	0.001
Cut Off Frequency	8.4 MHz	2.4 MHz
Stop Band Attenuation	-60 dB	-60 dB
Output Word Length	16 bits	16 bits

Figure 11. Frequency Response of Decimation Filter

Figure 12. Filter Coefficients of Decimation Filter

Figure 13. Simulation Result of Half-band Filter using CSD Representation

Figure 14. Simulation Result of Half-band Filter using MSD Representation

Figure 15. Simulation Result of Decimation Filter for Architecture I

Figure 16. Simulation Result of Decimation Filter for Architecture II

Table 7. Area and Power Comparison of Decimation Filter Architectures

S.No.	Architecture Type	Number System	Total Gate Count	No. of Slices	No. of FF	No. of LUT	Logic	IOB	Total Power (mW)
1.	A.Two Stage Decimation Filter	Conventional Number System	17624	545	492	882	770	207	1278
2.	B.Cascaded Multi-standard Chain	Conventional Number System	4279	467	392	442	278	36	57.45
3.		Canonic Signed Digit (CSD)	3986	235	279	337	278	36	50.11
4.		Minimum Signed Digit (MSD)	3172	154	92	163	138	27	42.77
5.	C.Hybrid Architecture	Conventional Number System	3182	421	333	425	276	24	56.0
6.		Canonic Signed Digit (CSD)	2762	235	183	325	278	24	48
7.		Minimum Signed Digit (MSD)	2230	135	77	155	138	19	41

Table 8. Delay Comparison of Three Decimation Filter Architectures

S.No.	Architecture Type	Number System Representation	Delay (ns)	Power Delay Product
1	Two Stage Decimation Filter	Conventional Number System	27.801	23047.029
2	Cascaded Multi-Standard Decimation Chain	Conventional Number System	18.387	1056.333
3		Canonic Signed Digit (CSD)	13.784	690.716
4		Minimum Signed Digit (MSD)	6.104	274.68
5	Hybrid Filter	Conventional Number System	24.946	1396.976
6		Canonic Signed Digit (CSD)	17.293	830.064
7		Minimum Signed Digit (MSD)	10.345	424.145

7. Conclusion

All the three decimation filter architectures use the sinc type of CIC filter (Comb) network. Simulation results reveals that the total gate count of the decimation filter with MAC unit (two stage decimator) , Cascaded Multi-standard Decimation Chain and Hybrid architectures are found to be 17624 ,4279 and 3182 respectively using conventional number system. Further reduction in gate count can be achieved by using CSD and MSD representations for half band filter coefficients and it is identified to be 3986 and 3172 for cascaded chain architecture. For

the hybrid structure the gate count reduces further to 2762 and 2230 respectively using CSD and MSD representations. The dynamic power dissipation of the two stage decimator, Multi-standard Cascaded Chain and Hybrid architectures using two's complement arithmetic are found to be 1278 mW, 57.45mW and 56mW respectively. Using CSD and MSD representation for half band filters show considerable reduction in power dissipation of Cascaded Multistage Decimation Chain architecture and it is found to be 50.11mW and 42.77 mW respectively.

Using CSD and MSD representation for half band filter implementation of hybrid architecture show further reduction in power dissipation and it is found to be 48 mW and 41 mW respectively. From the implementation results, it is reflected that 47.89% of area reduction and 28.64% of dynamic power reduction are achieved using hybrid architecture. From Table 6.3, it is evident that delay is reduced for cascaded decimation chain architecture, when compared to hybrid structure. The delay is more in hybrid structure due to the controller section activities. In applications where area and power reduction are needed, hybrid decimation filter architecture can be used. For speedy decimation filtering operations, cascaded decimation chain architecture will be the better solution. Future work focuses on implementation of decimation filter architecture based on polyphase CIC structures.

8. References

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