PERFORMANCE EVALUATION ON UNIPOLAR PWM STRATEGIES FOR THREE PHASE DIODE CLAMPED MULTILEVEL INVERTER

C.R.Balamurugan¹ S.P.Natarajan² R.Bensraj³ and T.S.Anandhi⁴

¹Department of EEE, Arunai Engineering College, Tiruvannamalai
^{2,3,4} Annamalai University, Chidambaram, Tamilnadu

ABSTRACT

This paper proposes different types of modulation methods for the Diode Clamped Multi Level Inverter (DCMLI). In this paper, a DCMLI is controlled with Sinusoidal PWM technique (SPWM), Third Harmonic Injection PWM technique, Sixty degree PWM technique and Stepped wave technique with Sub harmonic (SHPWM), Carrier Overlapping (CO), Phase shift (PS), Variable frequency (VF) and the variation of Total Harmonic Distortion (THD) in their outputs are observed and also chosen inverter is controlled by SPWM technique, THIPWM technique, Sixty degree PWM and Stepped wave technique by varying the modulation index. Simulation are performed using MATLAB-SIMULINK. It is observed that SHPWM strategy provide output with relatively low distortion. It is observed that COPWM strategy provides higher V_{rms} compared to other modulation strategies.

KEYWORDS

THD, Stepped, THIPWM, 60 degree PWM, unipolar.

1.INTRODUCTION

MLIs easily produce high-power, high-voltage output with the multilevel structure because of the way the device voltage stresses are controlled in the structure. Babaei et al [1] proposed a inverter contained of a series connection of the proposed basic unit and is able to only generate positive levels at the output. Selvamuthukumaran et al[2] also proposed a H-MCPWM strategy ensures low leakage current in the transformer less PV inverter system with simplicity in implementation of the modulation strategy using lesser number of carriers. Edpuganti et al [3] suggested to operate a multilevel inverter for motor drive using SOP strategy. Kai-Ming Tsang et al [4] proposed a topology approach enables multilevel output to be realized by a few cascaded H-bridges and a three-leg inverter using lower number of power switches. Babaei et al [5] suggested a topology which requires lesser number of power switches and dc voltage sources. Odeh et al [6] developed a multicarrier, phase disposition PWM technique is applied to generate the gating signals for the power switches. Young et al. [7] discusses a combination of batteries can be controlled according to the batteries' voltages to implement the battery-balancing function. Gupta et al [8] made a synthesis of multilevel waveform using minimum number of power switches as compared to the classical topologies. Cougo et al [9] suggest pulse width modulation technique based on carriers' disposition and on zero sequence injection is analyzed for parallel multilevel inverters. Zixin et al. [10] discusses level of the output voltage is only half of the dc-link voltage in all conditions, leading to much reduced dv/dt. Palanivel et al [11] observed this topologies of multilevel inverter have several advantages such as high output voltage, lower

electromagnetic interference, lower THD. Khoucha et al [12] developed a symmetrical and asymmetrical arrangements of five- and seven-level H-bridge inverters are compared in order to determine optimum arrangement with lower switching losses and optimized output voltage quality. Jing zhao et al [13] suggested minimum number of devices switching on or off within broad modulation index range, accordingly reducing switching losses and reduce the amplitude of lower harmonics. Naumanem et al [14] proposed pulsed inverter voltage and the impedance mismatch between the cable and the motor cause an oscillating overvoltage in the motor terminals.

2. MULTILEVEL INVERTER

The MLIs synthesize a near sinusoidal voltage from several DC voltage sources. A diode clamped multilevel (m-level) inverter typically consists of (m-1) capacitors on the bus and produces m levels on the phase voltage. Fig.1 shows three phase five level diode clamped multilevel inverter. The numbering order of the switches for R-phase is S_{a1} , S_{a2} , S_{a3} , S_{a4} , S_{a1}' , S_{a2}' , S_{a3}' and S_{a4}' .

Figure. 1 Power Circuit for 3Φ DCMLI

The gate signals for chosen five level diode clamped inverter are simulated using MATLAB-SIMULINK. The control gate signals are developed and checked. Fig. 2 shows a sample SIMULINK model.

Figure. 2 Sample control signal generation SIMULINK

3. UNIPOLAR MULTICARRIER PWM STRATEGIES

This paper presents four types of unipolar PWM strategies.

3.1. Unipolar Sub Harmonic PWM Strategies

The principle of the USHPWM strategy is similar to bipolar PDPWM strategy.

$$m_a = A_m / n * A_c$$

Figure. 3 Sample modulating and Carrier signal for USHPWM technique ($m_a=0.8$, $m_f=40$)

3.2. Unipolar Phase Shift (PSPWM) Strategy

The UPSPWM is same as bipolar PSPWM strategy.

$$m_a = A_m / A_c$$

Figure. 4 Sample modulating and Carrier signal for UPSPWM strategy ($m_a=0.8$, $m_f=40$)

3.3. Unipolar Carrier Overlapping (COPWM) Strategy

The UCOPWM is same as bipolar COPWM.

Figure. 5 Sample modulating and carrier signals for UCOPWM strategy ($m_a=0.8$, $m_f=40$)

3.4. Unipolar Variable Frequency (VFPWM) Strategy

The UVFPWM is same as bipolar VFPWM.

Figure. 6 Sample modulating and carrier signals for UVFPWM strategy ($m_a=0.8$, $m_f=40$)

4. THIRD HARMONIC INJECTION METHOD

The third-harmonic is a advanced modulation technique. By using this signal as reference the root mean square value of voltage will increase by 15.5 %. But the THD will be increased compared to sinusoidal signal. THIPWM technique is shown in Figs. 7 to 10.

Figure. 7 Modulating and Carrier signal for UTHIPWM strategy ($m_a=0.8$, $m_f=40$)

Figure. 8 Modulating and Carrier signal for UPSPWM strategy ($m_a=0.8$, $m_f=40$)

Figure. 9 Modulating and Carrier signal for UCOPWM strategy ($m_a=0.8$, $m_f=40$)

Figure. 10 Modulating and Carrier signal for UVFPWM strategy ($m_a=0.8$, $m_f=40$)

5. 60 DEGREE PWM METHOD

This method is a advanced modulation technique. This type of reference is also called as trapezoidal reference. This type of reference also increase the fundamental voltage. 60 degree PWM technique is shown in Figs. 11 to 14.

Figure. 11 Modulating and Carrier signal for USHPWM strategy ($m_a=0.8$, $m_f=40$)

Figure. 12 Modulating and Carrier signal for UPSPWM strategy ($m_a=0.8$, $m_f=40$)

Figure. 13 Modulating and Carrier signal for UCOPWM strategy ($m_a=0.8$, $m_f=40$)

Figure. 14 Modulating and Carrier signal for UVFPWM strategy ($m_a=0.8$, $m_f=40$)

6. STEPPED MODULATION

The stepped wave is a advanced modulation reference. This reference is used to increase the fundamental RMS voltage. Stepped wave PWM techniques is as shown in Figs. 15 to 18.

Figure. 15 Modulating and Carrier signal for USHPWM strategy ($m_a=0.8$, $m_f=40$)

Figure. 16 Modulating and Carrier signal for UPSPWM strategy ($m_a=0.8$, $m_f=40$)

Figure. 17 Modulating and Carrier signal for UCOPWM strategy ($m_a=0.8$, $m_f=40$)

Figure. 18 Modulating and Carrier signal for UVFPWM strategy ($m_a=0.8$, $m_f=40$)

7. SIMULATION RESULT

Switching signals for DCMLI are developed using unipolar PWM techniques discussed previously. Simulation and hardware results are taken for different values of m_a ranging from 0.6 – 1. The Hardware and simulation parameters are : $V_{DC} = 880V$, $m_f = 40$, $f_c = 2000Hz$, $f_m = 50Hz$ and R (load) = 100 ohms.

Figure. 19 Output voltage generated by USHPWM strategy for sine. Reference

Figure. 20 FFT plot for output voltage of USHPWM strategy for sine. reference

Figure. 21 Output voltage generated by UCOPWM strategy for sine. reference

Figure. 22 FFT plot for output voltage of UCOPWM strategy for sine. reference

Figure. 23 Output voltage generated by UPSPWM strategy for sine. reference

Figure. 24 FFT plot for output voltage of UPSPWM strategy for sine. reference

Figure. 25 Output voltage generated by UVFPWM strategy for sine. reference

Figure. 26 FFT plot for output voltage of UVFPWM strategy for sine. reference

Figure. 27 Output voltage generated by USHPWM strategy for THI reference

Figure. 28 FFT plot for output voltage of USHPWM strategy for THI reference

Figure. 29 Output voltage generated by UCOPWM strategy for THI reference

Figure. 30 FFT plot for output voltage of UCOPWM strategy for THI reference

Figure. 31 Output voltage generated by UPSPWM strategy for THI reference

Figure. 32 FFT plot for output voltage of UPSPWM strategy for THI reference

Figure. 33 Output voltage generated by UVFPWM strategy for THI reference

Figure. 34 FFT plot for output voltage of UVFPWM strategy for THI reference

Figure. 35 Output voltage generated by USHPWM strategy for 60 degree reference

Figure. 36 FFT plot for output voltage of USHPWM strategy for 60 degree reference

Figure. 37 Output voltage generated by UCOPWM strategy for 60 degree reference

Figure. 38 FFT plot for output voltage of UCOPWM strategy for 60 degree reference

Figure. 39 Output voltage generated by UPSPWM strategy for 60 degree reference

Figure. 40 FFT plot for output voltage of UPSPWM strategy for 60 degree reference

Figure. 41 Output voltage generated by UVFPWM strategy for 60 degree reference

Figure. 42 FFT plot for output voltage of UVFPWM strategy for 60 degree reference

Figure. 43 Output voltage generated by USHPWM strategy for stepped reference

Figure. 44 FFT plot for output voltage of USHPWM strategy for stepped reference

Figure. 45 Output voltage generated by UCOPWM strategy for stepped reference

Figure. 46 FFT plot for output voltage of UCOPWM strategy for stepped reference

Figure. 47 Output voltage generated by UPSPWM strategy for stepped reference

Figure. 48 FFT plot for output voltage of UPSPWM strategy for stepped reference

Figure. 49 Output voltage generated by UVFPWM strategy for stepped reference

Figure. 50 FFT plot for output voltage of UVFPWM strategy for stepped reference

Table 1. % THD for different modulation indices for sinusoidal reference

m_a	USHPWM	UCOPWM	UPSPWM	UVFPWM
1	28.08	39.08	34.34	28.19
0.9	35.35	46.58	44.24	35.33
0.8	40.46	56.48	52.60	40.48
0.7	44.28	71.91	58.48	44.63
0.6	46.10	88.32	60.22	45.89

Table.2 V_{RMS} (fundamental) for different modulation indices with sinusoidal reference

m_a	USHPWM	UCOPWM	UPSPWM	UVFPWM
1	305.3	315.9	291.2	305.4
0.9	272.4	290	252.4	272.3
0.8	240	258.4	212.9	239.8
0.7	206.2	218.4	176.1	206
0.6	173.8	181.6	141.6	246.8

Table.3 % THD for different modulation indices for THI PWM reference

m_a	USHPWM	UCOPWM	UPSPWM	UVFPWM
1	28.79	33.36	31.14	28.89
0.9	36.60	39.05	42.56	36.74
0.8	43.15	47.80	52.61	43.42
0.7	46.69	64.71	59.23	46.90
0.6	44.93	81.49	60.36	45.02

Table.4 V_{RMS} (fundamental) for different modulation indices with THI PWM reference

m_a	USHPWM	UCOPWM	UPSPWM	UVFPWM
1	357.2	364.3	349.4	357.1
0.9	319.3	337.9	305.4	319.4
0.8	281.3	306.3	259.5	281.4
0.7	242.4	260.6	215.1	242.6
0.6	203.5	217.1	168.2	203.6

Table.5 % THD for different modulation indices with 60 degree PWM reference

m_a	USHPWM	UCOPWM	UPSPWM	UVFPWM
1	24.72	30.99	24.94	37.31
0.9	34.13	37.41	38.88	34.22
0.8	41.38	42.30	49.60	41.55
0.7	46.24	61.03	58.34	46.44
0.6	46.10	78.05	61.86	46.04

Table.6 V_{RMS} (fundamental) for different modulation indices with 60 degree PWM reference

m_a	USHPWM	UCOPWM	UPSPWM	UVFPWM
1	372.6	374.8	369.6	373.1
0.9	332.4	345.9	321.8	332.5
0.8	292.9	319.7	274.6	293.1
0.7	253.3	271.5	227.4	253.1
0.6	212.5	226.3	180.1	212.5

Table.7 % THD for different modulation indices with Stepped wave reference

m_a	USHPWM	UCOPWM	UPSPWM	UVFPWM
1	26.22	38.38	31.09	26.01
0.9	34.84	46.35	42.77	34.69
0.8	40.58	55.94	51.94	41.22
0.7	43.66	72.29	58.16	44.92
0.6	48.84	88.16	61.42	48.32

Table.8 V_{RMS} (fundamental) for different modulation indices with Stepped wave reference

m_a	USHPWM	UCOPWM	UPSPWM	UVFPWM
1	305.4	318.9	295.5	304.9
0.9	273.7	286	256.1	272.9
0.8	244.5	257.7	219.2	242.6
0.7	215	218.3	182.3	212.4
0.6	180.6	182.3	145.2	179.6

Table.9 Crest Factor for different modulation indices with sinusoidal reference

m_a	USHPWM	UCOPWM	UPSPWM	UVFPWM
1	1.4140	1.4140	1.4144	1.4142
0.9	1.4141	1.4144	1.4144	1.4142
0.8	1.4142	1.4144	1.4142	1.4140
0.7	1.4146	1.4139	1.4145	1.4140
0.6	1.4143	1.4140	1.4145	1.4143

Table.10 Crest Factor for different modulation indices with THI PWM reference

m_a	USHPWM	UCOPWM	UPSPWM	UVFPWM
1	1.4140	1.4139	1.4141	1.4141
0.9	1.4140	1.4143	1.4142	1.4139
0.8	1.4141	1.4142	1.4142	1.4140
0.7	1.4141	1.4144	1.4142	1.4142
0.6	1.4147	1.4140	1.4137	1.4145

Table.11 Crest Factor for different modulation indices with 60 degree PWM reference

m_a	USHPWM	UCOPWM	UPSPWM	UVFPWM
1	1.4143	1.4143	1.4142	1.4143
0.9	1.4139	1.4142	1.4142	1.4141
0.8	1.4141	1.4141	1.4140	1.4141
0.7	1.4141	1.4143	1.4142	1.4144
0.6	1.4141	1.4140	1.4142	1.4145

Table.12 Crest Factor for different modulation indices with Stepped wave reference

m_a	USHPWM	UCOPWM	UPSPWM	UVFPWM
1	1.4142	1.4142	1.4142	1.4142
0.9	1.4143	1.4188	1.4139	1.4144
0.8	1.4143	1.4140	1.4142	1.4142
0.7	1.4139	1.4141	1.4141	1.4138
0.6	1.4141	1.4147	1.4146	1.4136

Table.13 Form Factor for different modulation indices with sinusoidal reference

m_a	USHPWM	UCOPWM	UPSPWM	UVFPWM
1	15265	15795	14560	15270
0.9	13620	14500	12620	13615
0.8	12000	12920	10645	11990
0.7	20620	10920	8805	10300
0.6	17380	9080	7080	17450

Table.14 Form Factor for different modulation indices with THI PWM reference

m_a	USHPWM	UCOPWM	UPSPWM	UVFPWM
1	17860	18215	17470	17855
0.9	15965	16895	15270	15970
0.8	14065	15315	12975	14070
0.7	12120	13030	10755	12130
0.6	10175	10855	8410	10180

Table.15 Form Factor for different modulation indices with 60 degree PWM reference

m_a	USHPWM	UCOPWM	UPSPWM	UVFPWM
1	18630	18740	18480	18655
0.9	16620	17295	16090	16625
0.8	14645	15985	13730	14655
0.7	12665	13575	11370	12655
0.6	10625	11315	9005	10625

Table.16 Form Factor for different modulation indices with Stepped wave reference

m_a	USHPWM	UCOPWM	UPSPWM	UVFPWM
1	15270	15945	14775	15245
0.9	13685	14300	12805	13645
0.8	12225	12885	10960	12130
0.7	10750	10915	9115	10620
0.6	18060	9115	7260	17960

Table.17 Distortion Factor for different modulation indices with Sinusoidal reference

m_a	USHPWM	UCOPWM	UPSPWM	UVFPWM
1	0.1906	0.2210	0.9087	0.174
0.9	0.1615	0.4138	0.9493	0.182
0.8	0.1627	0.692	0.8822	0.189
0.7	0.201	0.834	0.897	0.221
0.6	0.079	0.911	0.328	0.028

Table.18 Distortion Factor for different modulation indices with THI PWM reference

m_a	USHPWM	UCOPWM	UPSPWM	UVFPWM
1	2.226	2.308	1.944	2.2180
0.9	2.192	2.199	2.007	2.2
0.8	2.269	2.072	2.007	2.280
0.7	2.22	2.09	1.947	2.243
0.6	2.217	2.015	2.079	2.227

Table.19 Distortion Factor for different modulation indices with 60 degree PWM reference

m_a	USHPWM	UCOPWM	UPSPWM	UVFPWM
1	2.148	2.282	1.940	2.185
0.9	2.131	2.221	1.914	2.141
0.8	2.176	2.061	1.929	2.195
0.7	2.228	2.044	1.97	2.206
0.6	2.156	1.969	2.012	2.155

Table.20 Distortion Factor for different modulation indices with Stepped wave reference

m_a	USHPWM	UCOPWM	UPSPWM	UVFPWM
1	0.429	0.184	0.191	0.472
0.9	0.395	0.419	1.206	0.459
0.8	0.293	0.818	1.138	0.442
0.7	0.187	0.97	0.972	0.4
0.6	0.089	1.034	0.685	0.268

8. CONCLUSIONS

From the Tables-1, 3, 5 and 7 is shown that USHPWM method produce lesser total harmonic distortion compared to other strategies developed. UCOPWM with Sine, THI, 60 degree and Stepped wave reference found to perform better since it provides more V_{RMS} (Tables - 2, 4, 6 and 8). (Tables - 9, 10, 11 and 12) provide crest factor, (Tables - 13, 14, 15 and 16) provide FF for all modulating indices and (Tables 17,18,19 and 20) provide DF.

REFERENCES

- [1] Babaei, E. ; Laali, S. ; Bayat, Z. (2015). "A Single-Phase Cascaded Multilevel Inverter Based on a New Basic Unit With Reduced Number of Power Switches," IEEE Trans. Power Electron., vol.62, no. 3, pp. 922-929.
- [2] Selvamuthukumar, R. ; Garg, A. ; Gupta, R. (2015). "Hybrid Multicarrier Modulation to Reduce Leakage Current in a Transformerless Cascaded Multilevel Inverter for Photovoltaic Systems," IEEE Trans. Power Electron., vol. 30, no. 4, pp. 1779-1783.
- [3] Edpuganti, A. ; Rathore, A.K. (2015). "Optimal Low Switching Frequency Pulse width Modulation of Nine-Level Cascade Inverter," IEEE Trans. Power Electron., vol. 3, no. 1, pp. 482-495.
- [4] Kai-Ming Tsang ; Wai-Lok Chan, (2014). "Single DC source three-phase multilevel inverter using reduced number of switches," IET Power Electronics, vol. 7, no. 4, pp. 775-783.
- [5] Babaei, E. ; Alilu, S. ; Laali, S., (2014). "A New General Topology for Cascaded Multilevel Inverters With Reduced Number of Components Based on Developed H-Bridge," IEEE Trans. Ind. Electron., vol. 61, no. 8, pp. 3932-3939.
- [6] Odeh, C.I. ; Nnadi, D.B.N., (2013). "Single-phase 9-level hybridized cascaded multilevel inverter ," IET. Power Electron., vol. 6 , no. 3, pp. 468-477.
- [7] Chung-Ming Young ; Neng-Yi Chu ; Liang-Rui Chen ; Yu-Chih Hsiao ; Chia-Zer Li., (2013) "A Single-Phase Multilevel Inverter With Battery Balancing," IEEE Tran. Ind. Electron., vol. 60 , no. 5, pp. 1972-1978.
- [8] Gupta, K.K. ; Jain, S., (2013) " Multilevel inverter topology based on series connected switched sources," IET. Power Electron., vol. 6 , no. 1, pp. 164-174.
- [9] Cougo, B. ; Gateau, G. ; Meynard, T. ; Bobrowska-Rafal, M. ; Cousineau, M., (2012). " PD Modulation Scheme for Three-Phase Parallel Multilevel Inverters," IEEE Trans. Industrial Electron., vol. 59 , no. 2, pp. 690-700.
- [10] Zixin Li ; Ping Wang ; Yaohua Li ; Fanqiang Gao., (2012). "A Novel Single-Phase Five-Level Inverter With Coupled Inductors," IEEE Trans. Power Electron., vol. 27, no. 6, pp. 2716-2725.
- [11] Palanivel, P. ; Dash, S.S., (2011). "Analysis of THD and output voltage performance for cascaded multilevel inverter using carrier pulse width modulation techniques," IET Power Electron., vol. 4, no. 8, pp. 951-958.
- [12] Khoucha, F. ; Lagoun, M.S. ; Kheloui, A. ; El Hachemi Benbouzid, M., (2011). "A Comparison of Symmetrical and Asymmetrical Three-Phase H-Bridge Multilevel Inverter for DTC Induction Motor Drives," IEEE Trans. Energy Conversion, vol. 26 ,no. 1, pp. 64-72.
- [13] Jing Zhao ; Xiangning He ; Zhao, Rongxiang, (2010). "A Novel PWM Control Method for Hybrid-Clamped Multilevel Inverters," IEEE Trans. Ind. Electron., vol. 57, no. 7, pp. 2365-2373.
- [14] Naumanen, V. ; Korhonen, J. ; Silventoinen, P. ; Pyrhönen, J., (2010). "Mitigation of high dv/dt-originated motor overvoltages in multilevel inverter drives," IET Power Electron., vol. 3, no. 5, pp. 681-689.